E·XFL

Intel - 5AGXBB1D4F40C4N Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

2014110	
Product Status	Obsolete
Number of LABs/CLBs	14151
Number of Logic Elements/Cells	300000
Total RAM Bits	17358848
Number of I/O	704
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxbb1d4f40c4n

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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1-5

Symbol	Description	Condition	Minimum ⁽¹⁾	Typical	Maximum ⁽¹⁾	Unit
V	Coro voltago powor supply	-C4, -I5, -C5, -C6	1.07	1.1	1.13	V
V CC	Core voltage power suppry	-I3	1.12	1.15	1.18	V
V	Periphery circuitry, PCIe hard IP block,	-C4, -I5, -C5, -C6	1.07	1.1	1.13	V
V CCP	and transceiver PCS power supply	-I3	1.12	1.15	1.18	V
		3.3 V	3.135	3.3	3.465	V
V	Configuration pins power supply	3.0 V	2.85	3.0	3.15	V
V CCPGM		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
V _{CC_AUX}	Auxiliary supply	_	2.375	2.5	2.625	V
V _{CCBAT} ⁽²⁾	Battery back-up power supply	_	1.2	—	3.0	V
	(For design security volatile key register)					
		3.3 V	3.135	3.3	3.465	V
V _{CCPD} ⁽³⁾	I/O pre-driver power supply	3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V

⁽¹⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(2) If you do not use the design security feature in Arria V devices, connect V_{CCBAT} to a 1.5-V, 2.5-V, or 3.0-V power supply. Arria V power-on reset (POR) circuitry monitors V_{CCBAT}. Arria V devices do not exit POR if V_{CCBAT} is not powered up.



⁽³⁾ V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25, or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V. V_{CCPD} must be 3.3 V when V_{CCIO} is 3.3 V.

Figure 1-1: Equation for OCT Variation Without Recalibration

$$R_{OCT} = R_{SCAL} \left(1 + \left(\frac{dR}{dT} \times \Delta T \right) \pm \left(\frac{dR}{dV} \times \Delta V \right) \right)$$

The definitions for the equation are as follows:

- The R_{OCT} value calculated shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
- R_{SCAL} is the OCT resistance value at power-up.
- ΔT is the variation of temperature with respect to the temperature at power up.
- ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
- dR/dT is the percentage change of R_{SCAL} with temperature.
- dR/dV is the percentage change of R_{SCAL} with voltage.

OCT Variation after Power-Up Calibration

Table 1-10: OCT Variation after Power-Up Calibration for Arria V Devices

This table lists OCT variation with temperature and voltage after power-up calibration. The OCT variation is valid for a V_{CCIO} range of $\pm 5\%$ and a temperature range of 0°C to 85°C.

Symbol	Description	V _{CCIO} (V)	Value	Unit
		3.0	0.100	
		2.5	0.100	
	OCT variation with voltage without recalibration	1.8	0.100	
dR/dV		1.5	0.100	%/mV
		1.35	0.150	
		1.25	0.150	
		1.2	0.150	



1/O Standard	V _{CCIO} (V)			V _{SWI}	_{NG(DC)} (V)	V _{X(AC)} (V)		V _{SV}	_{WING(AC)} (V)	
	Min	Тур	Max	Min	Мах	Min	Тур	Max	Min	Max
SSTL-125	1.19	1.25	1.31	0.18	(15)	V _{CCIO} /2 – 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} – V _{REF})	$2(V_{IL(AC)} - V_{REF})$

Differential HSTL and HSUL I/O Standards

Table 1-18: Differential HSTL and HSUL I/O Standards for Arria V Devices

I/O Standard	,	V _{CCIO} (V))	V _{DI}	_{F(DC)} (V)		$V_{X(AC)}(V)$			$V_{CM(DC)}(V)$		V	_{DIF(AC)} (V)
	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Мах
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	_	0.78	_	1.12	0.78	_	1.12	0.4	_
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V _{CCIO} + 0.3	_	$0.5 imes V_{ m CCIO}$		$0.4 \times V_{ m CCIO}$	$0.5 imes V_{ m CCIO}$	$0.6 \times V_{ m CCIO}$	0.3	V _{CCIO} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	$\begin{array}{c} 0.5 \times \\ \mathrm{V}_{\mathrm{CCIO}} - \\ 0.12 \end{array}$	0.5 × V _{CCIO}	$\begin{array}{c} 0.5 \times \\ \mathrm{V}_{\mathrm{CCIO}} \\ + \ 0.12 \end{array}$	$0.4 \times V_{\rm CCIO}$	0.5 × V _{CCIO}	0.6 × V _{CCIO}	0.44	0.44

Differential I/O Standard Specifications

Table 1-19: Differential I/O Standard Specifications for Arria V Devices

Differential inputs are powered by V_{CCPD} which requires 2.5 V.



Symbol/Description	Condition	Tran	Unit		
Symbol Description	Condition	Min	Тур	Max	Onic
	10 Hz	_	—	-50	dBc/Hz
$T_{a} = \frac{1}{2} \left(\frac{1}{2} \right)^{2} \left(\frac{1}{2} \right$	100 Hz			-80	dBc/Hz
	1 KHz			-110	dBc/Hz
Hansmitter REPCLK phase hoise	10 KHz			-120	dBc/Hz
	100 KHz			-120	dBc/Hz
	≥1 MHz			-130	dBc/Hz
R _{REF}	_		2000 ±1%		Ω

Table 1-27: Transceiver Clocks Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Tran	Unit			
Symbol/Description	Condition	Min	Тур	Max	Onic	
fixedclk clock frequency	PCIe Receiver Detect	_	125		MHz	
Transceiver Reconfiguration Controller IP (mgmt_clk_clk) clock frequency	—	75	—	125	MHz	

Table 1-28: Receiver Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	T	Linit		
	Condition	Min	Тур	Мах	Onit
Supported I/O Standards		1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS			
Data rate (6-Gbps transceiver) ⁽⁴⁴⁾	_	611		6553.6	Mbps

⁽⁴³⁾ The transmitter REFCLK phase jitter is 30 ps p-p (5 ps RMS) with bit error rate (BER) 10⁻¹², equivalent to 14 sigma.



⁽⁴⁴⁾ To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain

Figure 1-3: CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices





Protocol	Sub-protocol	Data Rate (Mbps)
	SONET 155	155.52
SONET	SONET 622	622.08
	SONET 2488	2,488.32
	GPON 155	155.52
Gigabit-canable passive optical network (GPON)	GPON 622	622.08
Gigable-capable passive optical network (GI OIV)	GPON 1244	1,244.16
	GPON 2488	2,488.32
QSGMII	QSGMII 5000	5,000

Core Performance Specifications

Clock Tree Specifications

Table 1-35: Clock Tree Specifications for Arria V Devices

Parameter		Performance	Unit	
	-I3, -C4	–I5, –C5	-C6	omt
Global clock and Regional clock	625	625	525	MHz
Peripheral clock	450	400	350	MHz

PLL Specifications

Table 1-36: PLL Specifications for Arria V Devices

This table lists the Arria V PLL block specifications. Arria V PLL block does not include HPS PLL.



Symbol	Parameter	Condition	Min	Тур	Мах	Unit
t a	Period jitter for dedicated clock output	$F_{OUT} \ge 100 \text{ MHz}$			175	ps (p-p)
CASC_OUTPJ_DC	in cascaded PLLs	F _{OUT} < 100 MHz			17.5	mUI (p-p)
t _{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 μs	_			±10	%
dK _{BIT}	Bit number of Delta Sigma Modulator (DSM)	_	8	24	32	bits
k _{VALUE}	Numerator of fraction	_	128	8388608	2147483648	_
f _{RES}	Resolution of VCO frequency	$f_{INPFD} = 100 \text{ MHz}$	390625	5.96	0.023	Hz

Related Information

Memory Output Clock Jitter Specifications on page 1-57

Provides more information about the external memory interface clock output jitter specifications.

- Upstream PLL: 0.59 MHz ≤ Upstream PLL BW < 1 MHz
- Downstream PLL: Downstream PLL BW > 2 MHz



⁽⁷¹⁾ The cascaded PLL specification is only applicable with the following conditions:

HPS JTAG Timing Specifications

Symbol	Description	Min	Max	Unit
t _{JCP}	TCK clock period	30	_	ns
t _{JCH}	TCK clock high time	14		ns
t _{JCL}	TCK clock low time	14		ns
t _{JPSU (TDI)}	TDI JTAG port setup time	2		ns
t _{JPSU (TMS)}	TMS JTAG port setup time	3		ns
t _{JPH}	JTAG port hold time	5		ns
t _{JPCO}	JTAG port clock to output		12 ⁽⁹⁰⁾	ns
t _{JPZX}	JTAG port high impedance to valid output		14 ⁽⁹⁰⁾	ns
t _{JPXZ}	JTAG port valid output to high impedance		14 ⁽⁹⁰⁾	ns

Table 1-62: HPS JTAG Timing Parameters and Values for Arria V Devices

Configuration Specifications

This section provides configuration specifications and timing for Arria V devices.

POR Specifications

Table 1-63: Fast and Standard POR Delay Specification for Arria V Devices

POR Delay	Minimum	Maximum	Unit
Fast	4	12 ⁽⁹¹⁾	ms

⁽⁹⁰⁾ A 1-ns adder is required for each V_{CCIO_HPS} voltage step down from 3.0 V. For example, t_{JPCO} = 13 ns if V_{CCIO_HPS} of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

⁽⁹¹⁾ The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.



Initialization

Table 1-71: Initialization Clock Source Option and the Maximum Frequency for Arria V Devices

Initialization Clock Source	Configuration Scheme	Maximum Frequency (MHz)	Minimum Number of Clock Cycles	
Internal Oscillator	AS, PS, and FPP	12.5		
(107)	PS and FPP	125	Τ	
CLKOSK	AS	100	¹ init	
DCLK	PS and FPP	125		

Configuration Files

Table 1-72: Uncompressed .rbf Sizes for Arria V Devices

Use this table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (.hex) or tabular text file (.ttf) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Quartus Prime software. However, for a specific version of the Quartus Prime software, any design targeted for the same device has the same uncompressed configuration file size.

The IOCSR raw binary file (.rbf) size is specifically for the Configuration via Protocol (CvP) feature.

Arria V GX, GT, SX, and ST Device Datasheet



⁽¹⁰⁷⁾ To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus Prime software from the **General** panel of the **Device and Pin Options** dialog box.

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)
	A1	71,015,712	439,960
	A3	71,015,712	439,960
	A5	101,740,800	446,360
Arria V CY	A7	101,740,800	446,360
	B1	137,785,088	457,368
	B3	137,785,088	457,368
	B5	185,915,808	463,128
	B7	185,915,808	463,128
	C3	71,015,712	439,960
Arria V CT	C7	101,740,800	446,360
Allia v GI	D3	137,785,088	457,368
	D7	185,915,808	463,128
Arria V SV	B3	185,903,680	450,968
Allia V SA	B5	185,903,680	450,968
Arria V ST	D3	185,903,680	450,968
Allia v SI	D5	185,903,680	450,968

Minimum Configuration Time Estimation

Table 1-73: Minimum Configuration Time Estimation for Arria V Devices

The estimated values are based on the configuration .rbf sizes in Uncompressed .rbf Sizes for Arria V Devices table.







Date	Version	Changes
Date December 2015	Version 2015.12.16	 Updated Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices table. Updated F_{clk}, T_{dutycycle}, and T_{dssfrst} specifications. Added T_{qspi_clk}, T_{din_starb}, and T_{din_end} specifications. Removed T_{dinmax} specifications. Updated the minimum specification for T_{clk} to 16.67 ns and removed the maximum specification in SPI Master Timing Requirements for Arria V Devices table. Updated Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices table. Updated T_{clk} to T_{sdmmc_clk_out} symbol. Updated T_{sdmmc_clk_out} and T_d specifications. Added T_{sdmmc_clk}, T_{su}, and T_h specifications. Removed T_{dinmax} specifications. Updated the following diagrams: Quad SPI Flash Timing Diagram SD/MMC Timing Diagram
		 Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.



Symbol	Description	Condition	Minimum ⁽¹¹⁴⁾	Typical	Maximum ⁽¹¹⁴⁾	Unit
VI	DC input voltage	_	-0.5	_	3.6	V
Vo	Output voltage		0	_	V _{CCIO}	V
Т.	Operating junction temperature	Commercial	0		85	°C
IJ		Industrial	-40	_	100	°C
t	Power supply ramp time	Standard POR	200 µs	_	100 ms	
L RAMP		Fast POR	200 µs	—	4 ms	

Recommended Transceiver Power Supply Operating Conditions

Table 2-6: Recommended Transceiver Power Supply Operating Conditions for Arria V GZ Devices

Symbol	Description	Minimum ⁽¹¹⁸⁾	Typical	Maximum ⁽¹¹⁸⁾	Unit	
V _{CCA_GXBL}	Transcaiver channel DLL newer supply (left side)	2.85	3.0	3.15	V	
(119), (120)	Transceiver channel FLL power supply (left side)	2.375	2.5	2.625	V	
V _{CCA}	Transcaiver channel DLL never supply (right side)	2.85	3.0	3.15	W	
GXBR ⁽¹¹⁹⁾ , ⁽¹²⁰⁾	Transceiver channel FLL power supply (fight side)	2.375	2.5	2.625	V	
V _{CCHIP_L}	Transceiver hard IP power supply (left side)	0.82	0.85	0.88	V	
V _{CCHSSI_L}	Transceiver PCS power supply (left side)	0.82	0.85	0.88	V	
V _{CCHSSI_R}	Transceiver PCS power supply (right side)	0.82	0.85	0.88	V	

⁽¹¹⁴⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹¹⁸⁾ This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹²⁰⁾ When using ATX PLLs, the supply must be 3.0 V.



⁽¹¹⁹⁾ This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

Table 2-19: Differential SSTL I/O Standards for Arria V GZ Devices

I/O Standard	V _{CCIO} (V)			V _{SWING}	_{G(DC)} (V)		$V_{X(AC)}(V)$			V _{SWING(AC)} (V)
	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V _{CCIO} + 0.6	V _{CCIO} /2 - 0.2		V _{CCIO} /2 + 0.2	0.62	$V_{CCIO} + 0.6$
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V _{CCIO} + 0.6	V _{CCIO} /2 - 0.175	_	V _{CCIO} /2 + 0.175	0.5	$V_{CCIO} + 0.6$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(127)	V _{CCIO} /2 - 0.15		V _{CCIO} /2 + 0.15	0.35	_
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	(127)	V _{CCIO} /2 - 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	$2(V_{IL(AC)} - V_{REF})$
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(127)	V _{CCIO} /2 - 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	_
SSTL-12 Class I, II	1.14	1.2	1.26	0.18		V _{REF} -0.15	V _{CCIO} /2	V _{REF} + 0.15	-0.30	0.30

Table 2-20: Differential HSTL and HSUL I/O Standards for Arria V GZ Devices

I/O Standard		۷ _{ccio} (۱	/)	V _{DIF}	_(DC) (V)	V _{X(AC)} (V)			V _{CM(DC)} (V)			V _{DIF(AC)} (V)	
	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Мах
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	_	0.78		1.12	0.78	_	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	_	0.68		0.9	0.68		0.9	0.4	—



 $^{^{(127)}}$ The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

2-28	Transmitter
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Sumbol/Description	Conditions	Trans	ceiver Spee	d Grade 2	Transc	Unit		
Symbol/Description	Conditions	Min	Тур	Мах	Min	Тур	Max	Onit
	85- Ω setting	—	85 ± 20%	_	_	85 ± 20%	—	Ω
Differential on-chip termination	100- Ω setting		100 ± 20%			100 ± 20%	_	Ω
resistors	120- Ω setting	—	120 ± 20%			120 ± 20%	_	Ω
	150-Ω setting	_	150 ± 20%			150 ± 20%	_	Ω
V _{OCM} (AC coupled)	0.65-V setting	—	650			650	_	mV
V _{OCM} (DC coupled)	_	—	650			650	—	mV
Intra-differential pair skew	Tx V _{CM} = 0.5 V and slew rate of 15 ps	—		15	_	_	15	ps
Intra-transceiver block transmitterx6 PMA bonded modechannel-to-channel skew				120			120	ps
Inter-transceiver block transmitter channel-to-channel skew	xN PMA bonded mode			500			500	ps

Related Information

Arria V Device Overview

For more information about device ordering codes.



Typical VOD Settings

The tolerance is +/-20% for all VOD settings except for settings 2 and below.									
Symbol	V _{OD} Setting	V _{OD} Value (mV)	V _{OD} Setting	V _{OD} Value (mV)					
	0 (166)	0	32	640					
	1 ⁽¹⁶⁶⁾	20	33	660					
	2(166)	40	34	680					
	3(166)	60	35	700					
	4 ⁽¹⁶⁶⁾	80	36	720					
	5 ⁽¹⁶⁶⁾	100	37	740					
	6	120	38	760					
V_{OD} differential peak to peak typical	7	140	39	780					
	8	160	40	800					
	9	180	41	820					
	10	200	42	840					
	11	220	43	860					
	12	240	44	880					
	13	260	45	900					
	14	280	46	920					

⁽¹⁶⁶⁾ If TX termination resistance = 100 Ω , this VOD setting is illegal.





2-42 Memory Block Specifications

Mada	Performar	nce		Unit	
Mode	C3, I3L	C4 I4		Onit	
One sum of two 27×27	380	300	MHz		
One sum of two 36×18	380	30	MHz		
One complex 18×18	400	35	MHz		
One 36 × 36	380	30	MHz		
Modes using Three DSP Blocks					
One complex 18×25	340	275	265	MHz	
Modes using Four DSP Blocks					
One complex 27×27	350	31	MHz		

Memory Block Specifications

Table 2-36: Memory Block Performance Specifications for Arria V GZ Devices

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.

Memory	Mode	Resour	ces Used		Unit			
		ALUTs	Memory	C3	C4	I3L	14	
MLAB	Single port, all supported widths	0	1	400	315	400	315	MHz
	Simple dual-port, x32/x64 depth	0	1	400	315	400	315	MHz
	Simple dual-port, x16 depth (178)	0	1	533	400	533	400	MHz
	ROM, all supported widths	0	1	500	450	500	450	MHz

⁽¹⁷⁸⁾ The F_{MAX} specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.



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Symbol	Conditions	C3, I3L			C4, I4			Unit	
Symbol	Conditions	Min	Тур	Мах	Min	Тур	Max		
t _{x Jitter} - True Differential I/O	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—		160		—	160	ps	
Standards	Total Jitter for Data Rate < 600 Mbps	—		0.1		_	0.1	UI	
t _{x Jitter} - Emulated Differential I/O Standards with Three	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—		300		—	325	ps	
External Output Resistor Network	Total Jitter for Data Rate < 600 Mbps	—		0.2		—	0.25	UI	
t _{DUTY}	Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	%	
	True Differential I/O Standards	_		200		—	200	ps	
t _{RISE} & t _{FALL}	Emulated Differential I/O Standards with three external output resistor networks			250		_	300	ps	
	True Differential I/O Standards			150		—	150	ps	
TCCS	Emulated Differential I/O Standards	_	_	300		_	300	ps	

Receiver High-Speed I/O Specifications

Table 2-41: Receiver High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.



Symbol	Conditions		C4, I4			Unit		
Symbol		Min	Тур	Мах	Min	Тур	Max	
	SERDES factor J = 3 to 10 (192), (193), (194), (195), (196), (197)	150	_	1250	150	—	1050	Mbps
True Differential I/O Standards - f _{HSDRDPA} (data rate)	SERDES factor $J \ge 4$ LVDS RX with DPA (193), (195), (196), (197)	150	_	1600	150		1250	Mbps
(uata fate)	SERDES factor J = 2, uses DDR Registers	(198)	_	(199)	(198)		(199)	Mbps
	SERDES factor J = 1, uses SDR Register	(198)	_	(199)	(198)		(199)	Mbps
	SERDES factor $J = 3$ to 10	(198)	—	(200)	(198)	—	(200)	Mbps
f _{HSDR} (data rate)	SERDES factor J = 2, uses DDR Registers	(198)	—	(199)	(198)		(199)	Mbps
	SERDES factor J = 1, uses SDR Register	(198)	—	(199)	(198)	_	(199)	Mbps

 $^{(192)}$ The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

⁽¹⁹³⁾ Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.

⁽¹⁹⁴⁾ Arria V GZ LVDS serialization and de-serialization factor needs to be x4 and above.

⁽¹⁹⁵⁾ Requires package skew compensation with PCB trace length.

⁽¹⁹⁶⁾ Do not mix single-ended I/O buffer within LVDS I/O bank.

⁽¹⁹⁷⁾ Chip-to-chip communication only with a maximum load of 5 pF.

⁽¹⁹⁸⁾ The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

⁽¹⁹⁹⁾ The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.

⁽²⁰⁰⁾ You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.





