E·XFL

Intel - 5AGXBB1D4F40I5N Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Details	
Product Status	Obsolete
Number of LABs/CLBs	14151
Number of Logic Elements/Cells	300000
Total RAM Bits	17358848
Number of I/O	704
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxbb1d4f40i5n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Symbol	Description	Maximum	Unit
I _{XCVR-RX (DC)}	DC current per transceiver receiver (RX) pin	50	mA

Internal Weak Pull-Up Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up.

Table 1-13: Internal Weak Pull-Up Resistor Values for Arria V Devices

Symbol	Description	Condition (V) ⁽¹¹⁾	Value ⁽¹²⁾	Unit
		$V_{CCIO} = 3.3 \pm 5\%$	25	kΩ
	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	$V_{CCIO} = 3.0 \pm 5\%$	25	kΩ
		$V_{CCIO} = 2.5 \pm 5\%$	25	kΩ
D		$V_{CCIO} = 1.8 \pm 5\%$	25	kΩ
кру		$V_{CCIO} = 1.5 \pm 5\%$	25	kΩ
		$V_{CCIO} = 1.35 \pm 5\%$	25	kΩ
		$V_{CCIO} = 1.25 \pm 5\%$	25	kΩ
		$V_{CCIO} = 1.2 \pm 5\%$	25	kΩ

Related Information

Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines

Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.



⁽¹⁰⁾ The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

 $^{^{(11)}}$ Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

⁽¹²⁾ Valid with $\pm 10\%$ tolerances to cover changes over PVT.

1/O Standard	V _{IL(DC)} (V)		V _{IH(DC)} (V)		V _{IL(AC)} (V)	V _{IH(AC)} (V)	V _{OL} (V)	V _{OH} (V)	I _{OL} ⁽¹⁴⁾	I_{a} (mA)
	Min	Max	Min	Мах	Max	Min	Мах	Min	(mA)	
HSTL-15 Class II	—	V _{REF} – 0.1	$V_{REF} + 0.1$	_	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	V _{CCIO} – 0.4	16	-16
HSTL-12 Class I	-0.15	V _{REF} – 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	V _{REF} – 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	16	-16
HSUL-12	_	V _{REF} – 0.13	$V_{REF} + 0.13$	_	V _{REF} - 0.22	V _{REF} + 0.22	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	_	_

Differential SSTL I/O Standards

Table 1-17: Differential SSTL I/O Standards for Arria V Devices

V _{CCIO} (V)			V _{SWING(DC)} (V)		V _{X(AC)} (V)			V _{SWING(AC)} (V)		
	Min	Тур	Max	Min	Мах	Min	Тур	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V _{CCIO} + 0.6	V _{CCIO} /2 – 0.2	—	V _{CCIO} /2 + 0.2	0.62	$V_{CCIO} + 0.6$
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V _{CCIO} + 0.6	V _{CCIO} /2 – 0.175	—	V _{CCIO} /2 + 0.175	0.5	$V_{CCIO} + 0.6$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(15)	V _{CCIO} /2 – 0.15	—	V _{CCIO} /2 + 0.15	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$
SSTL-135	1.283	1.35	1.45	0.18	(15)	V _{CCIO} /2 – 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} – V _{REF})	$2(V_{IL(AC)} - V_{REF})$

⁽¹⁴⁾ To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.



 $^{^{(15)}}$ The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
		-3 speed grade	5	—	800 ⁽⁶¹⁾	MHz
f	Input clock fraguency	-4 speed grade	5		800 ⁽⁶¹⁾	MHz
IIN	input clock nequency	–5 speed grade	5	_	750 ⁽⁶¹⁾	MHz
		-6 speed grade	5		625(61)	MHz
f _{INPFD}	Integer input clock frequency to the phase frequency detector (PFD)	_	5	_	325	MHz
f _{fINPFD}	Fractional input clock frequency to the PFD		50	_	160	MHz
		-3 speed grade	600	—	1600	MHz
f (62)	PLL voltage-controlled oscillator (VCO) operating range	-4 speed grade	600	_	1600	MHz
IVCO		–5 speed grade	600		1600	MHz
		-6 speed grade	600		1300	MHz
t _{EINDUTY}	Input clock or external feedback clock input duty cycle	_	40		60	%
		-3 speed grade	_	_	500 ⁽⁶³⁾	MHz
f	Output frequency for internal global or	-4 speed grade	—	—	500 ⁽⁶³⁾	MHz
LOUT	regional clock	-5 speed grade	_	_	500 ⁽⁶³⁾	MHz
		-6 speed grade	_	_	400 ⁽⁶³⁾	MHz



⁽⁶¹⁾ This specification is limited in the Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

⁽⁶²⁾ The VCO frequency reported by the Quartus Prime software takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

⁽⁶³⁾ This specification is limited by the lower of the two: I/O f_{MAX} or F_{OUT} of the PLL.

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
		-3 speed grade			670 ⁽⁶³⁾	MHz
f	Output frequency for external clock	-4 speed grade	_	_	670 ⁽⁶³⁾	MHz
IOUT_EXT	output	–5 speed grade		_	622 ⁽⁶³⁾	MHz
		–6 speed grade			500(63)	MHz
t _{OUTDUTY}	Duty cycle for external clock output (when set to 50%)	_	45	50	55	%
t _{FCOMP}	External feedback clock compensation time	_	_		10	ns
t _{DYCONFIGCLK}	Dynamic configuration clock for mgmt_ clk and scanclk	_	_		100	MHz
t _{LOCK}	Time required to lock from end-of- device configuration or deassertion of areset	_	_	_	1	ms
t _{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	_			1	ms
		Low	_	0.3	_	MHz
f_{CLBW}	PLL closed-loop bandwidth	Medium	_	1.5	_	MHz
		High ⁽⁶⁴⁾		4		MHz
t _{PLL_PSERR}	Accuracy of PLL phase shift				±50	ps
t _{ARESET}	Minimum pulse width on the areset signal		10		_	ns
t(65)(66)	Input clock cycle_to_cycle iitter	$F_{REF} \ge 100 \text{ MHz}$			0.15	UI (p-p)
'INCCJ		$F_{REF} < 100 \text{ MHz}$			±750	ps (p-p)

⁽⁶⁴⁾ High bandwidth PLL settings are not supported in external feedback mode.



⁽⁶⁵⁾ A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

⁽⁶⁶⁾ F_{REF} is f_{IN}/N , specification applies when N = 1.

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
t a	Period jitter for dedicated clock output	$F_{OUT} \ge 100 \text{ MHz}$			175	ps (p-p)
CASC_OUTPJ_DC	in cascaded PLLs	F _{OUT} < 100 MHz			17.5	mUI (p-p)
t _{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 μs	_			±10	%
dK _{BIT}	Bit number of Delta Sigma Modulator (DSM)	_	8	24	32	bits
k _{VALUE}	Numerator of fraction	_	128	8388608	2147483648	_
f _{RES}	Resolution of VCO frequency	$f_{INPFD} = 100 \text{ MHz}$	390625	5.96	0.023	Hz

Related Information

Memory Output Clock Jitter Specifications on page 1-57

Provides more information about the external memory interface clock output jitter specifications.

- Upstream PLL: 0.59 MHz ≤ Upstream PLL BW < 1 MHz
- Downstream PLL: Downstream PLL BW > 2 MHz



⁽⁷¹⁾ The cascaded PLL specification is only applicable with the following conditions:

Figure 1-15: MDIO Timing Diagram



I²C Timing Characteristics

Table 1-59: I²C Timing Requirements for Arria V Devices

Symbol	Description	Standar	d Mode	Fast I	Mode	Unit	
Symbol	Description	Min	Max	Min	Max	Ont	
T _{clk}	Serial clock (SCL) clock period	10	—	2.5		μs	
T _{clkhigh}	SCL high time	4.7	—	0.6		μs	
T _{clklow}	SCL low time	4	—	1.3		μs	
T _s	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1		μs	
T _h	Hold time for SCL to SDA data	0	3.45	0	0.9	μs	
T _d	SCL to SDA output data delay	—	0.2		0.2	μs	
T _{su_start}	Setup time for a repeated start condition	4.7	_	0.6		μs	
T _{hd_start}	Hold time for a repeated start condition	4	_	0.6		μs	
T _{su_stop}	Setup time for a stop condition	4	_	0.6	_	μs	



Figure 1-16: I²C Timing Diagram



NAND Timing Characteristics

Table 1-60: NAND ONFI 1.0 Timing Requirements for Arria V Devices

The NAND controller supports Open NAND FLASH Interface (ONFI) 1.0 Mode 5 timing as well as legacy NAND devices. This table lists the requirements for ONFI 1.0 mode 5 timing. The HPS NAND controller can meet this timing by programming the c4 output of the main HPS PLL and timing registers provided in the NAND controller.

Symbol	Description	Min	Max	Unit
T _{wp} ⁽⁸⁹⁾	Write enable pulse width	10	—	ns
T _{wh} ⁽⁸⁹⁾	Write enable hold time	7		ns
T _{rp} ⁽⁸⁹⁾	Read enable pulse width	10		ns
T _{reh} ⁽⁸⁹⁾	Read enable hold time	7		ns
T _{clesu} ⁽⁸⁹⁾	Command latch enable to write enable setup time	10		ns
T _{cleh} ⁽⁸⁹⁾	Command latch enable to write enable hold time	5		ns
T _{cesu} ⁽⁸⁹⁾	Chip enable to write enable setup time	15		ns
T _{ceh} ⁽⁸⁹⁾	Chip enable to write enable hold time	5		ns
T _{alesu} ⁽⁸⁹⁾	Address latch enable to write enable setup time	10		ns
T _{aleh} ⁽⁸⁹⁾	Address latch enable to write enable hold time	5		ns
T _{dsu} ⁽⁸⁹⁾	Data to write enable setup time	10		ns

⁽⁸⁹⁾ Timing of the NAND interface is controlled through the NAND configuration registers.



Initialization

Table 1-71: Initialization Clock Source Option and the Maximum Frequency for Arria V Devices

Initialization Clock Source	Configuration Scheme	Maximum Frequency (MHz)	Minimum Number of Clock Cycles
Internal Oscillator	AS, PS, and FPP	12.5	
(107)	PS and FPP	125	Т
CLKOSK	AS	100	- ¹ init
DCLK	PS and FPP	125	

Configuration Files

Table 1-72: Uncompressed .rbf Sizes for Arria V Devices

Use this table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (.hex) or tabular text file (.ttf) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Quartus Prime software. However, for a specific version of the Quartus Prime software, any design targeted for the same device has the same uncompressed configuration file size.

The IOCSR raw binary file (.rbf) size is specifically for the Configuration via Protocol (CvP) feature.

Arria V GX, GT, SX, and ST Device Datasheet



⁽¹⁰⁷⁾ To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus Prime software from the **General** panel of the **Device and Pin Options** dialog box.

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)
	A1	71,015,712	439,960
	A3	71,015,712	439,960
	A5	101,740,800	446,360
Arria V GX	A7	101,740,800	446,360
	B1	137,785,088	457,368
	B3	137,785,088	457,368
	B5	185,915,808	463,128
	B7	185,915,808	463,128
	C3	71,015,712	439,960
Arria V CT	C7	101,740,800	446,360
Allia v GI	D3	137,785,088	457,368
	D7	185,915,808	463,128
Arria V SV	B3	185,903,680	450,968
Allia V SA	B5	185,903,680	450,968
Arria V ST	D3	185,903,680	450,968
Allia v SI	D5	185,903,680	450,968

Minimum Configuration Time Estimation

Table 1-73: Minimum Configuration Time Estimation for Arria V Devices

The estimated values are based on the configuration .rbf sizes in Uncompressed .rbf Sizes for Arria V Devices table.



			Active Seria	 (108)		Fast Passi	ve Parallel ⁽¹⁰⁹⁾
Variant	Member Code	Width	DCLK (MHz)	Minimum Configura- tion Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
	A1	4	100	178	16	125	36
	A3	4	100	178	16	125	36
	A5	4	100	255	16	125	51
Arria V CV	A7	4	100	255	16	125	51
Arria v GX	B1	4	100	344	16	125	69
	В3	4	100	344	16	125	69
	B5	4	100	465	16	125	93
	B7	4	100	465	16	125	93
	C3	4	100	178	16	125	36
Amia V CT	C7	4	100	255	16	125	51
Allia v GI	D3	4	100	344	16	125	69
	D7	4	100	465	16	125	93
Arria V SV	В3	4	100	465	16	125	93
AIIIa V SA	B5	4	100	465	16	125	93
Arria V ST	D3	4	100	465	16	125	93
AIIIa v SI	D5	4	100	465	Ition line (ms)I 612517816125178161252551612525516125344161253441612546516125178161253441612546516125465161254651612546516125465161254651612546516125465161254651612546516125465161254651612546516125465161254651612546516125465161254651612546516125	93	

Related Information Configuration Files on page 1-83

(108) DCLK frequency of 100 MHz using external CLKUSR.
 (109) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

1-100 Document Revision History

Date	Version	Changes
November 2012	3.0	 Updated Table 2, Table 4, Table 9, Table 14, Table 16, Table 17, Table 20, Table 21, Table 25, Table 29, Table 36, Table 56, Table 57, and Table 60. Removed table: Transceiver Block Jitter Specifications for Arria V Devices. Added HPS information: Added "HPS Specifications" section. Added Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, and Table 50. Added Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19. Updated Table 3 and Table 5.
October 2012	2.4	 Updated Arria V GX V_{CCR_GXBL/R}, V_{CCT_GXBL/R}, and V_{CCL_GXBL/R} minimum and maximum values, and data rate in Table 4. Added receiver V_{ICM} (AC coupled) and V_{ICM} (DC coupled) values, and transmitter V_{OCM} (AC coupled) and V_{OCM} (DC coupled) values in Table 20 and Table 21.
August 2012	2.3	Updated the SERDES factor condition in Table 30.
July 2012	2.2	 Updated the maximum voltage for V_I (DC input voltage) in Table 1. Updated Table 20 to include the Arria V GX -I3 speed grade. Updated the minimum value of the fixedclk clock frequency in Table 20 and Table 21. Updated the SERDES factor condition in Table 30. Updated Table 50 to include the IOE programmable delay settings for the Arria V GX -I3 speed grade.
June 2012	2.1	Updated V _{CCR_GXBL/R} , V _{CCT_GXBL/R} , and V _{CCL_GXBL/R} values in Table 4.



Bus Hold Specifications

Table 2-9: Bus Hold Parameters for Arria V GZ Devices

			V _{CCIO}										
Parameter	Symbol	Conditions	1.2 V		1.5	1.5 V		1.8 V		2.5 V		3.0 V	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I _{SUSL}	V _{IN} > V _{IL} (maximum)	22.5	_	25.0	_	30.0		50.0	_	70.0	_	μΑ
High sustaining current	I _{SUSH}	V _{IN} < V _{IH} (minimum)	-22.5	_	-25.0	_	-30.0	_	-50.0	_	-70.0	_	μΑ
Low overdrive current	I _{ODL}	$0V < V_{IN} < V_{CCIO}$	_	120	_	160	_	200	_	300	_	500	μΑ
High overdrive current	I _{ODH}	$0V < V_{IN} < V_{CCIO}$	—	-120	_	-160	_	-200		-300	_	-500	μΑ
Bus-hold trip point	V _{TRIP}		0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block.

Table 2-10: OCT Calibration Accuracy Specifications for Arria V GZ Devices

OCT calibration accuracy is valid at the time of calibration only.





Sumbol/Description	Conditions	Trans	ceiver Spee	d Grade 2	Transceiver Speed Grade 3			Unit
Symbol/Description	Conditions	Min	Тур	Max	Min	Тур	Max	
fixedclk clock frequency	PCIe Receiver Detect	_	100 or 125	_	_	100 or 125	_	MHz
Reconfiguration clock (mgmt_clk_ clk) frequency	—	100		125	100	_	125	MHz

Related Information

Arria V Device Overview

For more information about device ordering codes.

Receiver

Table 2-24: Receiver Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Trans	ceiver Spee	d Grade 2	Transceiver Speed Grade 3			Unit
Symbol Description	Conditions	Min	Тур	Max	Transceiver Speed Grade 3 Units Min Typ Max Units 600 — 8800 Min 600 — 10312.5 Min — — 1.2 Min — — — —	Onic		
Supported I/O Standards	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS							
Data rate (Standard PCS) (143), (144)	—	600		9900	600	_	8800	Mbps
Data rate (10G PCS) (143), (144)	_	600		12500	600	_	10312.5	Mbps
Absolute $\mathrm{V}_{\mathrm{MAX}}$ for a receiver pin $^{(145)}$	—			1.2			1.2	V
Absolute V_{MIN} for a receiver pin	_	-0.4	_		-0.4	_	_	V

⁽¹⁴³⁾ The line data rate may be limited by PCS-FPGA interface speed grade.

⁽¹⁴⁴⁾ To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.



⁽¹⁴⁵⁾ The device cannot tolerate prolonged operation at this absolute maximum.

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Symbol/Description	Conditions	Trans	ceiver Spee	d Grade 2	Transceiver Speed Grade 3			Unit
Symbol/Description	Conditions	Min	Тур	Max	Min	Тур	Max	Onit
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) before device configuration	—			1.6	—	_	1.6	V
Maximum peak-to-peak differential	$V_{CCR_GXB} = 1.0 V$ $(V_{ICM} = 0.75 V)$			1.8	—		1.8	V
device configuration ⁽¹⁴⁶⁾	$V_{CCR_GXB} = 0.85 V$ $(V_{ICM} = 0.6 V)$			2.4	—		2.4	V
Minimum differential eye opening at receiver serial input pins ⁽¹⁴⁷⁾⁽¹⁴⁸⁾	_	85		_	85	_	—	mV
	85– Ω setting		85 ± 30%	—	—	85 ± 30%	_	Ω
Differential on-chip termination	100– Ω setting		100 ± 30%	—	—	100 ± 30%	_	Ω
resistors	120– Ω setting		120 ± 30%	—	_	120 ± 30%		Ω
	150– Ω setting		150 ± 30%	_	_	150 ± 30%	_	Ω



⁽¹⁴⁶⁾ The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to 4 × (absolute V_{MAX} for receiver pin - V_{ICM}).

⁽¹⁴⁷⁾ The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

⁽¹⁴⁸⁾ Minimum eye opening of 85 mV is only for the unstressed input eye condition.

Table 2-26: CMU PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the Arria V Device Overview.

Symbol/Description	Conditions	Trans	ceiver Spee	d Grade 2	Transceiver Speed Grade 3			Unit
Symbol/Description	Conditions	Min	Тур	Max	Min	Тур	ed Grade 3 Max 10312.5 — 10	Onit
Supported data range	_	600	_	12500	600	_	10312.5	Mbps
t _{pll_powerdown} ⁽¹⁵³⁾	—	1			1	_		μs
t _{pll_lock} ⁽¹⁵⁴⁾	_			10			10	μs

Related Information

Arria V Device Overview

For more information about device ordering codes.

ATX PLL

Table 2-27: ATX PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the Arria V Device Overview.

Arria V GZ Device Datasheet

Altera Corporation



 $t_{pll_powerdown}$ is the PLL powerdown minimum pulse width. (153)

⁽¹⁵⁴⁾ $t_{\text{pll} \text{ lock}}$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

2-42 Memory Block Specifications

Mada	Performar	nce		Unit
Mode	C3, I3L	C4	14	Onit
One sum of two 27×27	380	300 290		MHz
One sum of two 36×18	380	30	MHz	
One complex 18×18	400	35	MHz	
One 36 × 36	380	30	MHz	
Modes using Three DSP Blocks				
One complex 18×25	340	275	265	MHz
Modes using Four DSP Blocks				
One complex 27×27	350	31	10	MHz

Memory Block Specifications

Table 2-36: Memory Block Performance Specifications for Arria V GZ Devices

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.

Memory	Mode	Resour	ces Used		Unit			
memory	moue	ALUTs	Memory	C3	C4	I3L	14	
	Single port, all supported widths	0	1	400	315	400	315	MHz
MLAB	Simple dual-port, x32/x64 depth	0	1	400	315	400	315	MHz
	Simple dual-port, x16 depth (178)	0	1	533	400	533	400	MHz
	ROM, all supported widths	0	1	500	450	500	450	MHz

⁽¹⁷⁸⁾ The F_{MAX} specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.



Symbol	Parameter	Minimum	Maximum	Unit
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times maximum$	—	_
		DCLK period		
t _{CD2UM} C	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (8576 × CLKUSR period) (209)		_

Related Information

- DCLK-to-DATA[] Ratio (r) for FPP Configuration on page 2-57 ٠
- Configuration, Design Security, and Remote System Upgrades in Arria V Devices

Arria V GZ Device Datasheet

Altera Corporation



⁽²⁰⁸⁾ The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

⁽²⁰⁹⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.

Table 2-60: PS Timing Parameters for Arria V GZ Devices

Symbol	Parameter	Minimum	Maximum	Unit
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	_	600	ns
t _{CFG}	nCONFIG low pulse width	2		μs
t _{STATUS}	nSTATUS low pulse width	268	1,506 (217)	μs
t _{CF2ST1}	nCONFIG high to nSTATUS high		1,506 (218)	μs
t _{CF2CK} (219)	nCONFIG high to first rising edge on DCLK	1,506	—	μs
t _{ST2CK} (219)	nSTATUS high to first rising edge of DCLK	2		μs
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5		ns
t _{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t _{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t _{CL}	DCLK low time	$0.45 imes 1/f_{ m MAX}$	—	S
t _{CLK}	DCLK period	1/f _{MAX}	—	s
f _{MAX}	DCLK frequency	_	125	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽²²⁰⁾	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK}$ period	_	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (8576 × CLKUSR period) (221)	_	

⁽²¹⁷⁾ This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.



⁽²¹⁸⁾ This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

⁽²¹⁹⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

⁽²²⁰⁾ The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

2-70 Remote System Upgrades Circuitry Timing Specification

Table 2-62: Uncompressed .rbf Sizes for Arria V GZ Devices

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ⁽²²³⁾
	E1	137,598,880	562,208
Arria V C7	E3	137,598,880	562,208
	E5	213,798,880	561,760
	E7	213,798,880	561,760

Table 2-63: Minimum Configuration Time Estimation for Arria V GZ Devices

Variant	Member Code	Active Serial ⁽²²⁴⁾			Fast Passive Parallel ⁽²²⁵⁾		
		Width	DCLK (MHz)	Min Config Time (ms)	Width	DCLK (MHz)	Min Config Time (ms)
Arria V GZ	E1	4	100	344	32	100	43
	E3	4	100	344	32	100	43
	E5	4	100	534	32	100	67
	E7	4	100	534	32	100	67

Remote System Upgrades Circuitry Timing Specification

Table 2-64: Remote System Upgrade Circuitry Timing Specifications

Parameter	Minimum	Maximum	Unit	
t _{RU_nCONFIG} ⁽²²⁶⁾	250	_	ns	
t _{RU_nRSTIMER} ⁽²²⁷⁾	250	_	ns	

⁽²²³⁾ The IOCSR **.rbf** size is specifically for the Configuration via Protocol (CvP) feature.

⁽²²⁴⁾ DCLK frequency of 100 MHz using external CLKUSR.

⁽²²⁵⁾ Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.



Date	Version	Changes
July 2014	3.8	 Updated Table 21. Updated Table 22 V_{OCM} (DC Coupled) condition. Updated the DCLK note to Figure 6, Figure 7, and Figure 9. Added note to Table 5 and Table 6. Added the DCLK specification to Table 50. Added note to Table 51. Updated the list of parameters in Table 53.
February 2014	3.7	Updated Table 28.
December 2013	3.6	 Updated Table 2, Table 13, Table 18, Table 19, Table 22, Table 30, Table 33, Table 37, Table 38, Table 45, Table 46, Table 47, Table 56, Table 49. Updated "PLL Specifications".
August 2013	3.5	Updated Table 28.
August 2013	3.4	 Removed Preliminary tags for Table 2, Table 4, Table 5, Table 14, Table 27, Table 28, Table 29, Table 31, Table 32, Table 43, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, and Table 54. Updated Table 2 and Table 28.
June 2013	3.3	Updated Table 23, Table 28, Table 51, and Table 55.
May 2013	3.2	 Added Table 23. Updated Table 5, Table 22, Table 26, and Table 57. Updated Figure 6, Figure 7, Figure 8, and Figure 9.
March 2013	3.1	 Updated Table 2, Table 6, Table 7, Table 8, Table 19, Table 22, Table 26, Table 29, Table 52. Updated "Maximum Allowed Overshoot and Undershoot Voltage".
December 2012	3.0	Initial release.

