Intel - 5AGXBB1D6F35C6N Datasheet





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Details

Product Status	Obsolete
Number of LABs/CLBs	14151
Number of Logic Elements/Cells	300000
Total RAM Bits	17358848
Number of I/O	544
Number of Gates	
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxbb1d6f35c6n

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Symbol/Description Condition		Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
Symbol/Description	Condition	Min	Тур	Max	Min	Тур	Max	Onic
Minimum differential eye opening at the receiver serial input pins ⁽³⁰⁾	_	100	_	_	100	_	_	mV
V _{ICM} (AC coupled)	—	_	0.7/0.75/ 0.8 ⁽³¹⁾			0.7/0.75/ 0.8 ⁽³¹⁾	—	mV
V _{ICM} (DC coupled)	\leq 3.2Gbps ⁽³²⁾	670	700	730	670	700	730	mV
	85- Ω setting		85			85	—	Ω
Differential on-chip	100- Ω setting		100			100		Ω
termination resistors	120-Ω setting		120			120	—	Ω
	150-Ω setting		150			150	—	Ω
$t_{LTR}^{(33)}$	_			10		—	10	μs
$t_{LTD}^{(34)}$		4	_		4	_	—	μs
t _{LTD_manual} ⁽³⁵⁾		4			4	—	—	μs
$t_{LTR_LTD_manual}^{(36)}$		15			15	—	_	μs
Programmable ppm detector ⁽³⁷⁾	_	±62.5, 100, 125, 200, 250, 300, 500, and 1000				ppm		

⁽³⁰⁾ The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(31) The AC coupled $V_{ICM} = 700 \text{ mV}$ for Arria V GX and SX in PCIe mode only. The AC coupled $V_{ICM} = 750 \text{ mV}$ for Arria V GT and ST in PCIe mode only.

⁽³²⁾ For standard protocol compliance, use AC coupling.

 $^{(33)}$ t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

 $^{(34)}$ t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.

 $^{(35)}$ t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.

 $t_{\text{LTR_LTD_manual}}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.



Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
Symbol/Description	Condition	Min	Тур	Max	Min	Тур	Max	Onit
Inter-transceiver block transmitter channel-to- channel skew ⁽³⁹⁾	×N PMA bonded mode			500		_	500	ps

Table 1-24: CMU PLL Specifications for Arria V GX and SX Devices

Symbol/Description	Transceiver Speed Grade 4		Transceiver S	peed Grade 6	Unit	
	Min	Мах	Min	Мах	Ont	
Supported data range	611	6553.6	611	3125	Mbps	
fPLL supported data range	611	3125	611	3125	Mbps	

Table 1-25: Transceiver-FPGA Fabric Interface Specifications for Arria V GX and SX Devices

Symbol/Description	Transceiver Spee	ed Grade 4 and 6	Unit	
Symbol Description	Min	Max		
Interface speed (single-width mode)	25	187.5	MHz	
Interface speed (double-width mode)	25	163.84	MHz	

Related Information

- CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain on page 1-35
- CTLE Response at Data Rates \leq 3.25 Gbps across Supported AC Gain and DC Gain on page 1-36
- Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines Provides more information about the power supply connection for different data rates.



⁽³⁹⁾ This specification is only applicable to channels on one side of the device across two transceiver banks.

Symbol/Description	Condition	Tran	Unit		
Symbol Description	Condition	Min	Тур	Max	Onic
	10 Hz	_	_	-50	dBc/Hz
	100 Hz			-80	dBc/Hz
Tronomitton paper unchass maios (43)	1 KHz			-110	dBc/Hz
Hansmitter REPCLK phase hoise	10 KHz			-120	dBc/Hz
	100 KHz			-120	dBc/Hz
	≥ 1 MHz			-130	dBc/Hz
R _{REF}	_		2000 ±1%		Ω

Table 1-27: Transceiver Clocks Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Tran	Unit			
Symbol/Description	Condition	Min	Тур	Max	onit	
fixedclk clock frequency	PCIe Receiver Detect	_	125		MHz	
Transceiver Reconfiguration Controller IP (mgmt_clk_clk) clock frequency	—	75	—	125	MHz	

Table 1-28: Receiver Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	T	Linit		
	Condition	Min	Тур	Мах	Onit
Supported I/O Standards	1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS				
Data rate (6-Gbps transceiver) ⁽⁴⁴⁾	_	611		6553.6	Mbps

⁽⁴³⁾ The transmitter REFCLK phase jitter is 30 ps p-p (5 ps RMS) with bit error rate (BER) 10⁻¹², equivalent to 14 sigma.



⁽⁴⁴⁾ To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Table 1-31: Transceiver-FPGA Fabric Interface Specifications for Arria V GT and ST Devices

Symbol/Description	Transceiver S	peed Grade 3	Unit	
Symbol Description	Min	Max	ont	
Interface speed (PMA direct mode)	50	153.6 ⁽⁵⁶⁾ , 161 ⁽⁵⁷⁾	MHz	
Interface speed (single-width mode)	25	187.5	MHz	
Interface speed (double-width mode)	25	163.84	MHz	

Related Information

- CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain on page 1-35
- CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain on page 1-36



⁽⁵⁶⁾ The maximum frequency when core transceiver local routing is selected.

⁽⁵⁷⁾ The maximum frequency when core transceiver network routing (GCLK, RCLK, or PCLK) is selected.

CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain

Figure 1-2: Continuous Time-Linear Equalizer (CTLE) Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices



Arria V GX, GT, SX, and ST Device Datasheet

Altera Corporation



Symbol	Parameter	Condition	Min	Тур	Мах	Unit
		-3 speed grade			670 ⁽⁶³⁾	MHz
f	Output frequency for external clock	-4 speed grade	_	_	670 ⁽⁶³⁾	MHz
IOUT_EXT	output	–5 speed grade		_	622 ⁽⁶³⁾	MHz
		–6 speed grade			500(63)	MHz
t _{OUTDUTY}	Duty cycle for external clock output (when set to 50%)	_	45	50	55	%
t _{FCOMP}	External feedback clock compensation time	_	_		10	ns
t _{DYCONFIGCLK}	Dynamic configuration clock for mgmt_ clk and scanclk	_	_		100	MHz
t _{LOCK}	Time required to lock from end-of- device configuration or deassertion of areset	_	_	_	1	ms
t _{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	_			1	ms
		Low	_	0.3	_	MHz
f_{CLBW}	PLL closed-loop bandwidth	Medium	_	1.5	_	MHz
		High ⁽⁶⁴⁾		4		MHz
t _{PLL_PSERR}	Accuracy of PLL phase shift				±50	ps
t _{ARESET}	Minimum pulse width on the areset signal		10			ns
t(65)(66)	Input clock cycle_to_cycle iitter	$F_{REF} \ge 100 \text{ MHz}$			0.15	UI (p-p)
'INCCJ	Input clock cycle-to-cycle jitter	$F_{REF} < 100 \text{ MHz}$			±750	ps (p-p)

⁽⁶⁴⁾ High bandwidth PLL settings are not supported in external feedback mode.



⁽⁶⁵⁾ A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

⁽⁶⁶⁾ F_{REF} is f_{IN}/N , specification applies when N = 1.

LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications





Table 1-42: LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.25 Gbps

Jitter Freq	uency (Hz)	Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350



Figure 1-12: USB Timing Diagram



Ethernet Media Access Controller (EMAC) Timing Characteristics

Table 1-56: Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements for Arria V Devices

Symbol	Description	Min	Тур	Мах	Unit
T _{clk} (1000Base-T)	TX_CLK clock period	_	8		ns
T _{clk} (100Base-T)	TX_CLK clock period	_	40		ns
T _{clk} (10Base-T)	TX_CLK clock period		400		ns
T _{dutycycle}	TX_CLK duty cycle	45	—	55	%
T _d	TX_CLK to TXD/TX_CTL output data delay	-0.85	—	0.15	ns

Figure 1-13: RGMII TX Timing Diagram





1-80 AS Configuration Timing

Symbol	Parameter	Minimum	Maximum	Unit
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times maximum$ DCLK period	—	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + ($T_{init} \times CLKUSR$ period)		
T _{init}	Number of clock cycles required for device initialization	8,576		Cycles

Related Information

FPP Configuration Timing

Provides the FPP configuration timing waveforms.

AS Configuration Timing

Table 1-68: AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices

The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

The t_{CF2CD} , t_{CF2ST0} , t_{CFG} , t_{STATUS} , and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in PS Timing Parameters for Arria V Devices table. You can obtain the t_{CF2ST1} value if you do not delay configuration by externally holding nSTATUS low.

Symbol	Parameter	Minimum	Maximum	Unit
t _{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	2	ns
t _{SU}	Data setup time before the falling edge on DCLK	1.5		ns
t _{DH}	Data hold time after the falling edge on DCLK	0	_	ns
t _{CD2UM}	CONF_DONE high to user mode	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	_	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + ($T_{init} \times CLKUSR$ period)	_	—
T _{init}	Number of clock cycles required for device initialization	8,576		Cycles



Term		Definition						
Single-ended voltage referenced I/O standard	The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing. Single-Ended Voltage Referenced I/O Standard							
			V _{CCI0}					
	V _{ОН}		V _{IH(AC)}					
			VIH(DC)					
		V _{REF}	V IL(DC)					
			VIL(AC)					
	V _{0L}							
			V _{SS}					
t _C	High-speed receiver/transmitter	input and output clock period.						
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).							
t _{DUTY}	High-speed I/O block—Duty cyc	le on high-speed transmitter output	clock.					



2-2 Absolute Maximum Ratings

Lower number refers to faster speed grade.

L = Low power devices.

Transceiver Speed Grade	Core Speed Grade							
	C3	C4	I3L	14				
2	Yes	_	Yes	_				
3		Yes		Yes				

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Arria V GZ devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions other than those listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 2-2: Absolute Maximum Ratings for Arria V GZ Devices

Symbol	Description	Minimum	Maximum	Unit
V _{CC}	Power supply for core voltage and periphery circuitry	-0.5	1.35	V
V _{CCPT}	Power supply for programmable power technology	-0.5	1.8	V
V _{CCPGM}	Power supply for configuration pins	-0.5	3.9	V
V _{CC_AUX}	Auxiliary supply for the programmable power technology	-0.5	3.4	V
V _{CCBAT}	Battery back-up power supply for design security volatile key register	-0.5	3.9	V
V _{CCPD}	I/O pre-driver power supply	-0.5	3.9	V
V _{CCIO}	I/O power supply	-0.5	3.9	V
V _{CCD_FPLL}	PLL digital power supply	-0.5	1.8	V
V _{CCA_FPLL}	PLL analog power supply	-0.5	3.4	V



Sumbol	Description	Conditions	Resistance	Unit		
Symbol	Description	Conditions	C3, I3L	C4, I4	Onic	
25-Ω R _S	Internal series termination without calibration (25- Ω setting)	V _{CCIO} = 1.8 and 1.5 V	±40	±40	%	
25-Ω R _S	Internal series termination without calibration (25- Ω setting)	$V_{CCIO} = 1.2 V$	±50	±50	%	
50-Ω R _S	Internal series termination without calibration (50- Ω setting)	V_{CCIO} = 1.8 and 1.5 V	±40	±40	%	
50-Ω R _S	Internal series termination without calibration (50- Ω setting)	$V_{CCIO} = 1.2 V$	±50	±50	%	
100-Ω R _D	Internal differential termination (100- Ω setting)	$V_{CCIO} = 2.5 V$	±25	±25	%	

Figure 2-1: OCT Variation Without Re-Calibration for Arria V GZ Devices

$$\mathbf{R}_{\text{OCT}} = \mathbf{R}_{\text{SCAL}} \left(1 + \left(\frac{dR}{dT} \times \bigtriangleup T \right) \pm \left(\frac{dR}{dV} \times \bigtriangleup V \right) \right)$$

Notes:

1. The R_{oct} value shows the range of OCT resistance with the variation of temperature and V_{ccio} . 2. R_{scAL} is the OCT resistance value at power-up. 3. ΔT is the variation of temperature with respect to the temperature at power-up. 4. ΔV is the variation of voltage with respect to the V_{ccio} at power-up. 5. dR/dT is the percentage change of R_{scAL} with temperature. 6. dR/dV is the percentage change of R_{scAL} with voltage

6. dR/dV is the percentage change of R_{SCAL} with voltage.

Table 2-12: OCT Variation after Power-Up Calibration for Arria V GZ Devices

Valid for a V_{CCIO} range of \pm 5% and a temperature range of 0° to 85°C.





Table 2-19: Differential SSTL I/O Standards for Arria V GZ Devices

I/O Standard	V _{CCIO} (V)			V _{SWING(DC)} (V)		V _{X(AC)} (V)			V _{SWING(AC)} (V)		
	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Max	
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V _{CCIO} + 0.6	V _{CCIO} /2 - 0.2		V _{CCIO} /2 + 0.2	0.62	$V_{CCIO} + 0.6$	
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V _{CCIO} + 0.6	V _{CCIO} /2 - 0.175	_	V _{CCIO} /2 + 0.175	0.5	$V_{CCIO} + 0.6$	
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(127)	V _{CCIO} /2 - 0.15		V _{CCIO} /2 + 0.15	0.35	_	
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	(127)	V _{CCIO} /2 - 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	$2(V_{IL(AC)} - V_{REF})$	
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(127)	V _{CCIO} /2 - 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	_	
SSTL-12 Class I, II	1.14	1.2	1.26	0.18		V _{REF} -0.15	V _{CCIO} /2	V _{REF} + 0.15	-0.30	0.30	

Table 2-20: Differential HSTL and HSUL I/O Standards for Arria V GZ Devices

I/O Standard	V _{CCIO} (V)		V _{DIF(DC)} (V)			V _{X(AC)} (V)			V _{CM(DC)} (V)			V _{DIF(AC)} (V)	
	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Мах
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	_	0.78		1.12	0.78	_	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	_	0.68		0.9	0.68		0.9	0.4	—



 $^{^{(127)}}$ The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Mode ⁽¹⁶⁴⁾	Transceiver	PMA Width	20	20	16	16	10	10	8	8
	Speed Grade	PCS/Core Width	40	20	32	16	20	10	16	8
Register	2	C3, I3L core speed grade	9.9	9	7.92	7.2	4.9	4.,5	3.92	3.6
	3	C4, I4 core speed grade	8.8	8.2	7.04	6.56	4.4	4.1	3.52	3.28

Related Information

Operating Conditions on page 2-1

10G PCS Data Rate

Table 2-31: 10G PCS Approximate Maximum Data Rate (Gbps) for Arria V GZ Devices

Mode ⁽¹⁶⁵⁾	Transceiver Speed	PMA Width	64	40	40	40	32	32
Mode	Grade	PCS Width	64	66/67	50	40	64/66/67	32
FIFO	2	C3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88
	3	C4, I4 core speed grade	10.3125	10.3125	10.69	10.3125	9.92	9.92
Register	2	C3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88
	3	C4, I4 core speed grade	10.3125	10.3125	10.69	10.3125	9.92	9.92

⁽¹⁶⁴⁾ The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.



⁽¹⁶⁵⁾ The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

t_{ARESET}

Symbol	Parameter	Min	Тур	Max	Unit
f	Output frequency for an internal global or regional clock (C3, I3L speed grade)	_	_	650	MHz
OUT	Output frequency for an internal global or regional clock (C4, I4 speed grade)	_		580	MHz
f _{OUT_EXT} ⁽¹⁶⁹⁾	Output frequency for an external clock output (C3, I3L speed grade)		_	667	MHz
	Output frequency for an external clock output (C4, I4 speed grade)	_	_	533	MHz
toutduty	Duty cycle for a dedicated external clock output (when set to 50%)	45	50	55	%
t _{FCOMP}	External feedback clock compensation time	—		10	ns
f _{DYCONFIGCLK}	Dynamic configuration clock for mgmt_clk and scanclk	_	_	100	MHz
t _{LOCK}	Time required to lock from the end-of-device configuration or deassertion of areset		_	1	ms
t _{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/ delays)	—	—	1	ms
	PLL closed-loop low bandwidth	_	0.3		MHz
f _{CLBW}	PLL closed-loop medium bandwidth	—	1.5		MHz
	PLL closed-loop high bandwidth (170)	_	4		MHz
t _{PLL_PSERR}	Accuracy of PLL phase shift	_	_	±50	ps

10

_

Minimum pulse width on the areset signal





ns

 $^{^{(169)}}$ This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.

⁽¹⁷⁰⁾ High bandwidth PLL settings are not supported in external feedback mode.

Active Serial Configuration Timing

Figure 2-9: AS Configuration Timing



Timing waveform for the active serial (AS) x1 mode and AS x4 mode configuration timing.

Notes:

1. If you are using AS ×4 mode, this signal represents the AS_DATA[3..0] and ERCQ sends in 4-bits of data for each DCLKcycle.

2. The initialization clock can be from internal oscillator or CLKUSR pin

3. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE ges low.

Table 2-58: AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices

The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in the "PS Timing Parameters for Arria V GZ Devices" table.



Passive Serial Configuration Timing

Figure 2-10: PS Configuration Timing Waveform

Timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.



Notes:

- 1. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- 2. After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.
- 3. After power-up, before and during configuration, CONF_DONE is low.
- 4. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- 5. DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the Device and Pins Option.
- 6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- 7. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.



Related Information

Configuration, Design Security, and Remote System Upgrades in Arria V Devices

Initialization

Table 2-61: Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices

Initialization Clock Source	Configuration Schemes	Maximum Frequency (MHz)	Minimum Number of Clock Cycles
Internal Oscillator	AS, PS, FPP	12.5	8576
CLKUSR ⁽²²²⁾	PS, FPP	125	
	AS	100	
DCLK	PS, FPP	125	

Configuration Files

Use the following table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (.hex) or tabular text file (.ttf) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size.

Arria V GZ Device Datasheet

Altera Corporation



⁽²²¹⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.

⁽²²²⁾ To enable CLKUSR as the initialization clock source, turn on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software from the General panel of the Device and Pin Options dialog box.

Glossary

Table 2-68: Glossary



