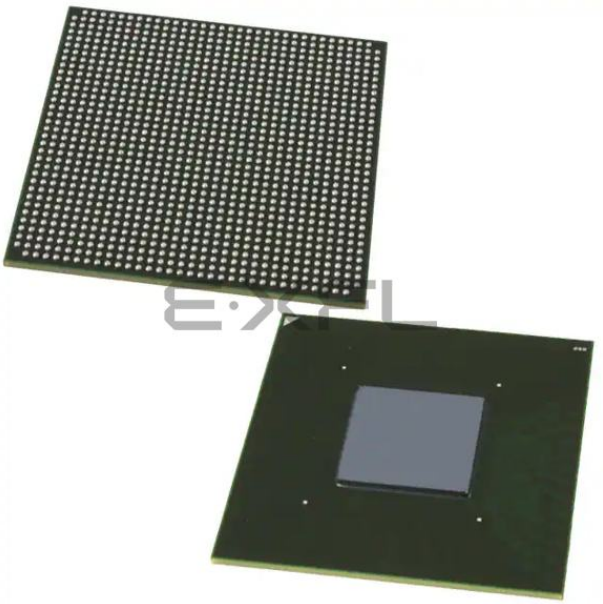

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	17110
Number of Logic Elements/Cells	362000
Total RAM Bits	19822592
Number of I/O	544
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxbb3d4f35c4n

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
Vi (AC)	AC input voltage	3.8	100	%
		3.85	68	%
		3.9	45	%
		3.95	28	%
		4	15	%
		4.05	13	%
		4.1	11	%
		4.15	9	%
		4.2	8	%
		4.25	7	%
		4.3	5.4	%
		4.35	3.2	%
		4.4	1.9	%
		4.45	1.1	%
		4.5	0.6	%
		4.55	0.4	%
		4.6	0.2	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Arria V devices.

Recommended Operating Conditions

Table 1-3: Recommended Operating Conditions for Arria V Devices

This table lists the steady-state voltage values expected from Arria V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Transceiver Power Supply Operating Conditions

Table 1-4: Transceiver Power Supply Operating Conditions for Arria V Devices

Symbol	Description	Minimum[5]	Typical	Maximum[5]	Unit
V_{CCA_GXBL}	Transceiver high voltage power (left side)	2.375	2.500	2.625	V
V_{CCA_GXBR}	Transceiver high voltage power (right side)				
V_{CCR_GXBL}	GX and SX speed grades—receiver power (left side)	1.08/1.12	1.1/1.15[6]	1.14/1.18	V
V_{CCR_GXBR}	GX and SX speed grades—receiver power (right side)				
V_{CCR_GXBL}	GT and ST speed grades—receiver power (left side)	1.17	1.20	1.23	V
V_{CCR_GXBR}	GT and ST speed grades—receiver power (right side)				
V_{CCT_GXBL}	GX and SX speed grades—transmitter power (left side)	1.08/1.12	1.1/1.15[6]	1.14/1.18	V
V_{CCT_GXBR}	GX and SX speed grades—transmitter power (right side)				
V_{CCT_GXBL}	GT and ST speed grades—transmitter power (left side)	1.17	1.20	1.23	V
V_{CCT_GXBR}	GT and ST speed grades—transmitter power (right side)				
V_{CCH_GXBL}	Transmitter output buffer power (left side)	1.425	1.500	1.575	V
V_{CCH_GXBR}	Transmitter output buffer power (right side)				

(5) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(6) For data rate <=3.2 Gbps, connect $V_{CCR\_GXBL/R}$, $V_{CCT\_GXBL/R}$, or $V_{CCL\_GXBL/R}$ to either 1.1-V or 1.15-V power supply. For data rate >3.2 Gbps, connect $V_{CCR\_GXBL/R}$, $V_{CCT\_GXBL/R}$, or $V_{CCL\_GXBL/R}$ to a 1.15-V power supply. For details, refer to the Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines.

I/O Pin Leakage Current

Table 1-6: I/O Pin Leakage Current for Arria V Devices

Symbol	Description	Condition	Min	Typ	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	–30	—	30	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	–30	—	30	µA

Bus Hold Specifications

Table 1-7: Bus Hold Parameters for Arria V Devices

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

Parameter	Symbol	Condition	V_{CCIO} (V)												Unit
			1.2		1.5		1.8		2.5		3.0		3.3		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (max)	8	—	12	—	30	—	50	—	70	—	70	—	µA
Bus-hold, high, sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (min)	–8	—	–12	—	–30	—	–50	—	–70	—	–70	—	µA
Bus-hold, low, overdrive current	I_{ODL}	0 V < V_{IN} < V_{CCIO}	—	125	—	175	—	200	—	300	—	500	—	500	µA
Bus-hold, high, overdrive current	I_{ODH}	0 V < V_{IN} < V_{CCIO}	—	–125	—	–175	—	–200	—	–300	—	–500	—	–500	µA

- **Transceiver Specifications for Arria V GT and ST Devices** on page 1-29
  Provides the specifications for transmitter, receiver, and reference clock I/O pin.

Switching Characteristics

This section provides performance characteristics of Arria V core and periphery blocks.

Transceiver Performance Specifications

Transceiver Specifications for Arria V GX and SX Devices

Table 1-20: Reference Clock Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported I/O standards	1.2 V PCML, 1.4 V PCML,1.5 V PCML, 2.5 V PCML, Differential LVPECL[23], HCSL, and LVDS							
Input frequency from REFCLK input pins	—	27	—	710	27	—	710	MHz
Rise time	Measure at ±60 mV of differential signal[24]	—	—	400	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal[24]	—	—	400	—	—	400	ps
Duty cycle	—	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	300[25]/ 2000	200	—	300[25]/ 2000	mV

(23) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.
(24) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
(25) The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

Transceiver Specifications for Arria V GT and ST Devices

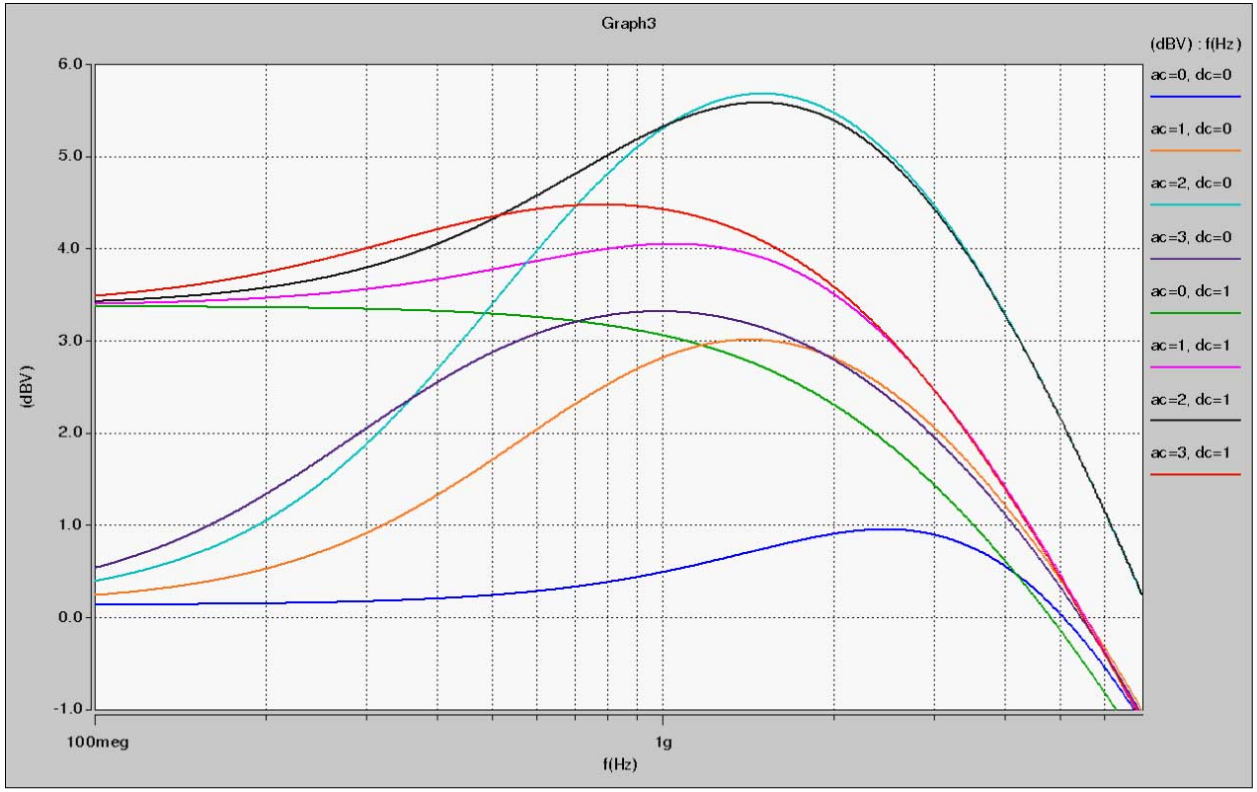
Table 1-26: Reference Clock Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O standards	1.2 V PCML, 1.4 VPCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL(40), HCSL, and LVDS				
Input frequency from REFCLK input pins	—	27	—	710	MHz
Rise time	Measure at ±60 mV of differential signal(41)	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal(41)	—	—	400	ps
Duty cycle	—	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	300(42)/2000	mV
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	Ω
V_{ICM} (AC coupled)	—	—	1.2	—	V
V_{ICM} (DC coupled)	HCSL I/O standard for the PCIe reference clock	250	—	550	mV

(40) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.
(41) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
(42) The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain

Figure 1-3: CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices



LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications

Figure 1-5: LVDS Soft-Clock Data Recovery (CDR)/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Equal to 1.25 Gbps

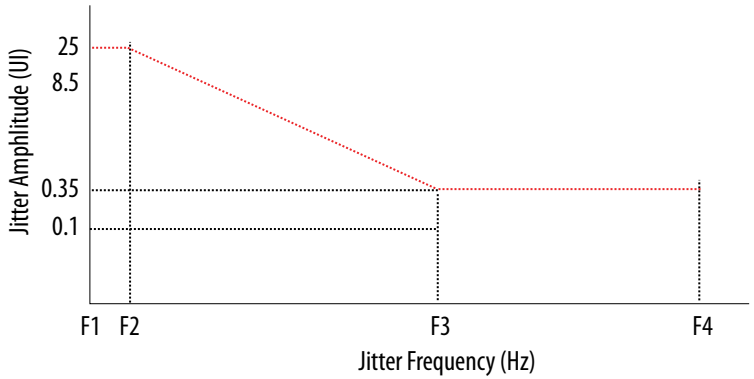


Table 1-42: LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.25 Gbps

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

HPS JTAG Timing Specifications

Table 1-62: HPS JTAG Timing Parameters and Values for Arria V Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	12(90)	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14(90)	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14(90)	ns

Configuration Specifications

This section provides configuration specifications and timing for Arria V devices.

POR Specifications

Table 1-63: Fast and Standard POR Delay Specification for Arria V Devices

POR Delay	Minimum	Maximum	Unit
Fast	4	12(91)	ms

(90) A 1-ns adder is required for each $V_{CCIO\ \_HPS}$ voltage step down from 3.0 V. For example, t_{JPCO}= 13 ns if $V_{CCIO\ \_HPS}$ of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

(91) The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

Symbol	Parameter	Minimum	Maximum	Unit
t_{STATUS}	nSTATUS low pulse width	268	1506(94)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506(95)	µs
t_{CF2CK}(96)	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}(96)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/ ×16)	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode(97)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4× maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} × CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

FPP Configuration Timing

Provides the FPP configuration timing waveforms.

(94) You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.
(95) You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.
(96) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.
(97) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CK}[105]	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}[105]	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode[106]	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times$ CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

PS Configuration Timing

Provides the PS configuration timing waveform.

(105) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

(106) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Variant	Member Code	Active Serial[108]			Fast Passive Parallel[109]		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
Arria V GX	A1	4	100	178	16	125	36
	A3	4	100	178	16	125	36
	A5	4	100	255	16	125	51
	A7	4	100	255	16	125	51
	B1	4	100	344	16	125	69
	B3	4	100	344	16	125	69
	B5	4	100	465	16	125	93
	B7	4	100	465	16	125	93
Arria V GT	C3	4	100	178	16	125	36
	C7	4	100	255	16	125	51
	D3	4	100	344	16	125	69
	D7	4	100	465	16	125	93
Arria V SX	B3	4	100	465	16	125	93
	B5	4	100	465	16	125	93
Arria V ST	D3	4	100	465	16	125	93
	D5	4	100	465	16	125	93

Related Information

Configuration Files on page 1-83

(108) DCLK frequency of 100 MHz using external CLKUSR.

(109) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Symbol	Description	Minimum	Maximum	Unit
V_I	DC input voltage	–0.5	3.8	V
T_J	Operating junction temperature	–55	125	°C
T_{STG}	Storage temperature (No bias)	–65	150	°C
I_{OUT}	DC output current per pin	–25	40	mA

Table 2-3: Transceiver Power Supply Absolute Conditions for Arria V GZ Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CCA_GXBL}	Transceiver channel PLL power supply (left side)	–0.5	3.75	V
V_{CCA_GXBR}	Transceiver channel PLL power supply (right side)	–0.5	3.75	V
V_{CCHIP_L}	Transceiver hard IP power supply (left side)	–0.5	1.35	V
V_{CCHSSI_L}	Transceiver PCS power supply (left side)	–0.5	1.35	V
V_{CCHSSI_R}	Transceiver PCS power supply (right side)	–0.5	1.35	V
V_{CCR_GXBL}	Receiver analog power supply (left side)	–0.5	1.35	V
V_{CCR_GXBR}	Receiver analog power supply (right side)	–0.5	1.35	V
V_{CCT_GXBL}	Transmitter analog power supply (left side)	–0.5	1.35	V
V_{CCT_GXBR}	Transmitter analog power supply (right side)	–0.5	1.35	V
V_{CCH_GXBL}	Transmitter output buffer power supply (left side)	–0.5	1.8	V
V_{CCH_GXBR}	Transmitter output buffer power supply (right side)	–0.5	1.8	V

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in the following table. They may also undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	—	85 ± 20%	—	Ω
	100-Ω setting	—	100 ± 20%	—	—	100 ± 20%	—	Ω
	120-Ω setting	—	120 ± 20%	—	—	120 ± 20%	—	Ω
	150-Ω setting	—	150 ± 20%	—	—	150 ± 20%	—	Ω
V_{OCM} (AC coupled)	0.65-V setting	—	650	—	—	650	—	mV
V_{OCM} (DC coupled)	—	—	650	—	—	650	—	mV
Intra-differential pair skew	Tx V_{CM} = 0.5 V and slew rate of 15 ps	—	—	15	—	—	15	ps
Intra-transceiver block transmitter channel-to-channel skew	x6 PMA bonded mode	—	—	120	—	—	120	ps
Inter-transceiver block transmitter channel-to-channel skew	xN PMA bonded mode	—	—	500	—	—	500	ps

Related Information

Arria V Device Overview

For more information about device ordering codes.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported data range	—	600	—	3250/ 3125(158)	600	—	3250/ 3125 (158)	Mbps
$t_{pll\_powerdown}$ (159)	—	1	—	—	1	—	—	µs
t_{pll_lock} (160)	—	—	—	10		—	10	µs

Related Information

Arria V Device Overview
For more information about device ordering codes.

Clock Network Data Rate

Table 2-29: Clock Network Maximum Data Rate Transmitter Specifications

Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.

Clock Network	ATX PLL			CMU PLL (161)			fPLL		
	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span
x1 (162)	12.5	—	6	12.5	—	6	3.125	—	3
x6 (162)	—	12.5	6	—	12.5	6	—	3.125	6
x6 PLL Feedback (163)	—	12.5	Side-wide	—	12.5	Side-wide	—	—	—

(158) When you use fPLL as a TXPLL of the transceiver.
(159) $t_{pll\_powerdown}$ is the PLL powerdown minimum pulse width.
(160) t_{pll_lock} is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
(161) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.
(162) Channel span is within a transceiver bank.
(163) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Clock Network	ATX PLL			CMU PLL [161]			fPLL		
	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span
xN (PCIe)	—	8.0	8	—	5.0	8	—	—	—
xN (Native PHY IP)	8.0	8.0	Up to 13 channels above and below PLL	7.99	7.99	Up to 13 channels above and below PLL	3.125	3.125	Up to 13 channels above and below PLL
	—	8.01 to 9.8304	Up to 7 channels above and below PLL						

Standard PCS Data Rate

Table 2-30: Standard PCS Approximate Maximum Date Rate (Gbps) for Arria V GZ Devices

The maximum data rate is also constrained by the transceiver speed grade. Refer to the "Commercial and Industrial Speed Grade Offering for Arria V GZ Devices" table for the transceiver speed grade.

Mode [164]	Transceiver Speed Grade	PMA Width	20	20	16	16	10	10	8	8
		PCS/Core Width	40	20	32	16	20	10	16	8
FIFO	2	C3, I3L core speed grade	9.9	9	7.84	7.2	5.3	4.7	4.24	3.76
	3	C4, I4 core speed grade	8.8	8.2	7.2	6.56	4.8	4.3	3.84	3.44

[161] ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

[164] The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Typical VOD Settings

Table 2-32: Typical V_{OD} Setting for Arria V GZ Channel, TX Termination = 100 Ω

The tolerance is +/-20% for all VOD settings except for settings 2 and below.

Symbol	V_{OD} Setting	V_{OD} Value (mV)	V_{OD} Setting	V_{OD} Value (mV)
V_{OD} **differential peak to peak typical**	0 (166)	0	32	640
	1 (166)	20	33	660
	2 (166)	40	34	680
	3 (166)	60	35	700
	4 (166)	80	36	720
	5 (166)	100	37	740
	6	120	38	760
	7	140	39	780
	8	160	40	800
	9	180	41	820
	10	200	42	840
	11	220	43	860
	12	240	44	880
	13	260	45	900
	14	280	46	920

(166) If TX termination resistance = 100 Ω,this VOD setting is illegal.

Core Performance Specifications

Clock Tree Specifications

Table 2-33: Clock Tree Performance for Arria V GZ Devices

Symbol	Performance		Unit
	C3, I3L	C4, I4	
Global and Regional Clock	650	580	MHz
Periphery Clock	500	500	MHz

PLL Specifications

Table 2-34: PLL Specifications for Arria V GZ Devices

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN} (167)	Input clock frequency (C3, I3L speed grade)	5	—	800	MHz
	Input clock frequency (C4, I4 speed grade)	5	—	650	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{FINPFD}	Fractional Input clock frequency to the PFD	50	—	160	MHz
f_{VCO} (168)	PLL VCO operating range (C3, I3L speed grade)	600	—	1600	MHz
	PLL VCO operating range (C4, I4 speed grade)	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%

(167) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(168) The VCO frequency reported by the Quartus II software in the **PLL Usage Summary** section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 3 to 10 (192), (193), (194), (195), (196), (197)	150	—	1250	150	—	1050	Mbps
	SERDES factor J ≥ 4 LVDS RX with DPA (193), (195), (196), (197)	150	—	1600	150	—	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(198)	—	(199)	(198)	—	(199)	Mbps
	SERDES factor J = 1, uses SDR Register	(198)	—	(199)	(198)	—	(199)	Mbps
f_{HSDR} (data rate)	SERDES factor J = 3 to 10	(198)	—	(200)	(198)	—	(200)	Mbps
	SERDES factor J = 2, uses DDR Registers	(198)	—	(199)	(198)	—	(199)	Mbps
	SERDES factor J = 1, uses SDR Register	(198)	—	(199)	(198)	—	(199)	Mbps

(192) The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.
(193) Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.
(194) Arria V GZ LVDS serialization and de-serialization factor needs to be x4 and above.
(195) Requires package skew compensation with PCB trace length.
(196) Do not mix single-ended I/O buffer within LVDS I/O bank.
(197) Chip-to-chip communication only with a maximum load of 5 pF.
(198) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.
(199) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.
(200) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

Number of DQS Delay Buffers	C3, I3L	C4, I4	Unit
4	120	128	ps

Memory Output Clock Jitter Specifications

Table 2-50: Memory Output Clock Jitter Specification for Arria V GZ Devices

The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

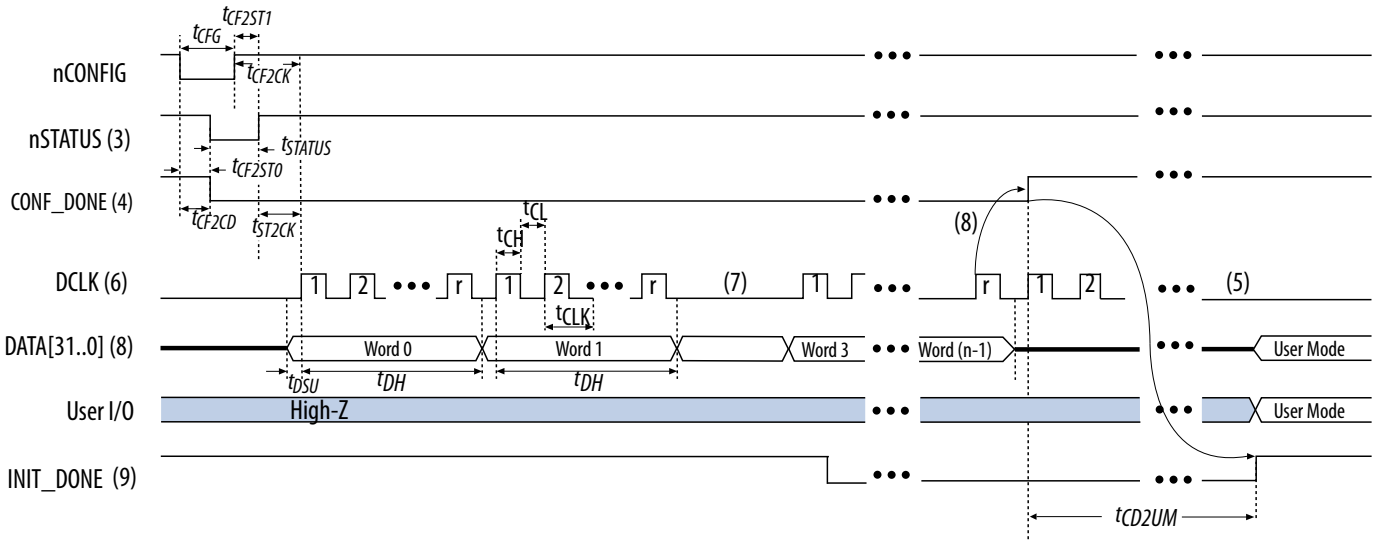
The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

Clock Network	Parameter	Symbol	C3, I3L		C4, I4		Unit
			Min	Max	Min	Max	
Regional	Clock period jitter	$t_{JIT(per)}$	–55	55	–55	55	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	–110	110	–110	110	ps
	Duty cycle jitter	$t_{JIT(duty)}$	–82.5	82.5	–82.5	82.5	ps
Global	Clock period jitter	$t_{JIT(per)}$	–82.5	82.5	–82.5	82.5	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	–165	165	–165	165	ps
	Duty cycle jitter	$t_{JIT(duty)}$	–90	90	–90	90	ps
PHY Clock	Clock period jitter	$t_{JIT(per)}$	–30	30	–35	35	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	–60	60	–70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	–45	45	–56	56	ps

FPP Configuration Timing when DCLK to DATA[] > 1

Figure 2-8: FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 ,

Timing when using a MAX II device, MAX V device, or microprocessor as an external host.



Notes:

1. To find out the DCLK-to-DATA[] ratio for your system, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
2. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
3. After power-up, the Arria V GZ device holds nSTATUS low for the time as specified by the POR delay.
4. After power-up, before and during configuration, CONF_DONE is low.
5. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
6. "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
7. If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31..0] pins prior to sending the first DCLK rising edge.
8. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
9. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.