Intel - 5AGXBB5D4F35C5N Datasheet





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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	19811
Number of Logic Elements/Cells	420000
Total RAM Bits	23625728
Number of I/O	544
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxbb5d4f35c5n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Symbol	Description	Condition	Minimum ⁽¹⁾	Typical	Maximum ⁽¹⁾	Unit
		3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
V	1/O buffers newer supply	1.8 V	1.71	1.8	1.89	V
V CCIO	1/O bullets power supply	1.5 V	1.425	1.5	1.575	V
		1.35 V	1.283	1.35	1.418	V
		1.25 V	1.19	1.25	1.31	V
		1.2 V	1.14	1.2	1.26	V
V _{CCD_FPLL}	PLL digital voltage regulator power supply	_	1.425	1.5	1.575	V
V _{CCA_FPLL}	PLL analog voltage regulator power supply	_	2.375	2.5	2.625	V
V _I	DC input voltage	_	-0.5	_	3.6	V
V _O	Output voltage	_	0	_	V _{CCIO}	V
T	Operating junction temperature	Commercial	0	_	85	°C
1 j	Operating junction temperature	Industrial	-40	_	100	°C
+ (4)	Power supply ramp time	Standard POR	200 µs	_	100 ms	_
$t_{RAMP}^{(4)}$	rower supply famp time	Fast POR	200 µs	_	4 ms	_



⁽¹⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁴⁾ This is also applicable to HPS power supply. For HPS power supply, refer to t_{RAMP} specifications for standard POR when HPS_PORSEL = 0 and t_{RAMP} specifications for fast POR when HPS_PORSEL = 1.

Transceiver Power Supply Operating Conditions

Table '	1-4:	Transceiver	Power S	upply	Operating	Conditions	for Arria V Devices	j
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Symbol	Description	Minimum ⁽⁵⁾	Typical	Maximum ⁽⁵⁾	Unit	
V _{CCA_GXBL}	Transceiver high voltage power (left side)	2 275	2 500	2 625	V	
V _{CCA_GXBR}	Transceiver high voltage power (right side)	2.575	2.300	2.025	v	
V _{CCR_GXBL}	GX and SX speed grades—receiver power (left side)	1.08/1.12	1 1/1 15(6)	1 14/1 18	V	
V _{CCR_GXBR}	GX and SX speed grades—receiver power (right side)	1.00/1.12	1.1/1.13	1.14/1.10	v	
V _{CCR_GXBL}	GT and ST speed grades—receiver power (left side)	1 17	1 20	1 23	V	
V _{CCR_GXBR}	GT and ST speed grades—receiver power (right side)	1.17	1.20	1.23	v	
V _{CCT_GXBL}	GX and SX speed grades—transmitter power (left side)	1.08/1.12	1 1/1 15(6)	1 14/1 19	V	
V _{CCT_GXBR}	GX and SX speed grades—transmitter power (right side)	1.00/1.12	1.1/1.15	1.14/1.10	V	
V _{CCT_GXBL}	GT and ST speed grades—transmitter power (left side)	1 17	1 20	1 23	V	
V _{CCT_GXBR}	GT and ST speed grades—transmitter power (right side)	1.17	1.20	1.23	v	
V _{CCH_GXBL}	Transmitter output buffer power (left side)	1 /25	1 500	1 575	V	
V _{CCH_GXBR}	Transmitter output buffer power (right side)	1.423	1.300	1.375	v	

⁽⁵⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁶⁾ For data rate <=3.2 Gbps, connect V_{CCR_GXBL/R}, V_{CCT_GXBL/R}, or V_{CCL_GXBL/R} to either 1.1-V or 1.15-V power supply. For data rate >3.2 Gbps, connect V_{CCR_GXBL/R}, V_{CCT_GXBL/R}, or V_{CCL_GXBL/R} to a 1.15-V power supply. For details, refer to the Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines.



I/O Pin Leakage Current

Table 1-6: I/O Pin Leakage Current for Arria V Devices

Symbol	Description	Condition	Min	Тур	Max	Unit
II	Input pin	$V_{I} = 0 V$ to $V_{CCIOMAX}$	-30	—	30	μΑ
I _{OZ}	Tri-stated I/O pin	$V_{O} = 0 V$ to $V_{CCIOMAX}$	-30		30	μΑ

Bus Hold Specifications

Table 1-7: Bus Hold Parameters for Arria V Devices

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

			V _{CCIO} (V)												
Parameter	Symbol	Condition	1.	.2	1	.5	1	.8	2	.5	3.	.0	3	.3	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I _{SUSL}	V _{IN} > V _{IL} (max)	8	_	12		30	_	50		70		70		μΑ
Bus-hold, high, sustaining current	I _{SUSH}	V _{IN} < V _{IH} (min)	-8	_	-12		-30	_	-50		-70	_	-70		μΑ
Bus-hold, low, overdrive current	I _{ODL}	$\begin{array}{c} 0 \ \mathrm{V} < \mathrm{V_{IN}} \\ < \mathrm{V_{CCIO}} \end{array}$		125	_	175	_	200		300		500	_	500	μΑ
Bus-hold, high, overdrive current	I _{ODH}	0 V <v<sub>IN <v<sub>CCIO</v<sub></v<sub>	_	-125	_	-175	_	-200		-300	_	-500	_	-500	μΑ

Arria V GX, GT, SX, and ST Device Datasheet

Altera Corporation



Symbol/Description	Condition	Trans	ceiver Speed Gr	ade 4	Transc	Unit		
Symbol/Description	Condition	Min	Тур	Max	Min	Тур	Max	Onit
Spread-spectrum modulating clock frequency	oread-spectrum PCI Express [®] (PCIe) odulating clock equency		—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to -0.5%			0 to -0.5%	—	—
On-chip termination resistors	—	—	100			100	_	Ω
V _{ICM} (AC coupled)	—	_	1.1/1.15 ⁽²⁶⁾			1.1/1.15 ⁽²⁶⁾	_	V
V_{ICM} (DC coupled)	HCSL I/O standard for the PCIe reference clock	250	_	550	250		550	mV
	10 Hz	_	_	-50		_	-50	dBc/Hz
	100 Hz	_	_	-80		_	-80	dBc/Hz
Transmitter REFCLK phase	1 KHz	_	—	-110		_	-110	dBc/Hz
noise ⁽²⁷⁾	10 KHz	—	—	-120		—	-120	dBc/Hz
_	100 KHz	_	_	-120		_	-120	dBc/Hz
	≥1 MHz	_	_	-130	_	_	-130	dBc/Hz
R _{REF}	_	_	2000 ±1%	_		2000 ±1%	_	Ω



⁽²⁶⁾ For data rate \leq 3.2 Gbps, connect V_{CCR_GXBL/R} to either 1.1-V or 1.15-V power supply. For data rate > 3.2 Gbps, connect V_{CCR_GXBL/R} to a 1.15-V power supply. For details, refer to the Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines.

⁽²⁷⁾ The transmitter REFCLK phase jitter is 30 ps p-p at bit error rate (BER) 10^{-12} .

Table 1-21: Transceiver Clocks Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transc	Unit		
Symbol/Description	Condition	Min	Тур	Max	Min	Тур	Max	
fixedclk clock frequency	PCIe Receiver Detect	_	125	_	_	125	_	MHz
Transceiver Reconfigura- tion Controller IP (mgmt_ clk_clk) clock frequency	_	75	_	125	75	_	125	MHz

Table 1-22: Receiver Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transc	llnit		
Symbol, Description		Min	Тур	Max	Min	Тур	Max	Onit
Supported I/O standards	1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS							
Data rate ⁽²⁸⁾		611	—	6553.6	611	—	3125	Mbps
Absolute V_{MAX} for a receiver pin ⁽²⁹⁾	_		_	1.2		—	1.2	V
Absolute V _{MIN} for a receiver pin	_	-0.4	_		-0.4	—	—	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) before device configuration	_	_		1.6		_	1.6	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) after device configuration	_	_	_	2.2		_	2.2	V



 ⁽²⁸⁾ To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.
 ⁽²⁹⁾ The device cannot tolerate prolonged operation at this absolute maximum.

Transceiver Specifications for Arria V GT and ST Devices

Table 1-26: Reference Clock Specifications	for Arria V GT and ST Devices
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Symbol/Description	Condition	Tran	sceiver Speed Gra	ide 3	Unit	
Symbol/Description	Condition	Min	Тур	Мах	Onic	
Supported I/O standards	1.2 V PCML, 1.4 VPCML,	1.5 V PCML, 2.5	V PCML, Differe	ential LVPECL ⁽⁴⁰⁾	, HCSL, and LVDS	
Input frequency from REFCLK input pins	_	27		710	MHz	
Rise time	Measure at ±60 mV of differential signal ⁽⁴¹⁾			400	ps	
Fall time	Measure at ±60 mV of differential signal ⁽⁴¹⁾			400	ps	
Duty cycle	_	45		55	%	
Peak-to-peak differential input voltage	—	200		300 ⁽⁴²⁾ /2000	mV	
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30		33	kHz	
Spread-spectrum downspread	PCIe		0 to -0.5%		_	
On-chip termination resistors	—		100		Ω	
V _{ICM} (AC coupled)	—	—	1.2		V	
V _{ICM} (DC coupled)	HCSL I/O standard for the PCIe reference clock	250		550	mV	



⁽⁴⁰⁾ Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

REFCLK performance requires to meet transmitter REFCLK phase noise specification. (41)

⁽⁴²⁾ The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain

Figure 1-3: CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices





1-40 Transceiver Compliance Specification

Quartus Prime 1st			Quar	tus Prime V _{OD} Se	etting			
Post Tap Pre- Emphasis Setting	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	Unit
16	_	_	9.56	7.73	6.49		_	dB
17	_		10.43	8.39	7.02		_	dB
18	_		11.23	9.03	7.52		_	dB
19	_		12.18	9.7	8.02		_	dB
20	_		13.17	10.34	8.59		_	dB
21	_		14.2	11.1			_	dB
22	_		15.38	11.87			_	dB
23	_		_	12.67	_	_	_	dB
24	_		_	13.48			_	dB
25	_		_	14.37			_	dB
26	_						_	dB
27	_						_	dB
28	_	_	_	_	_	_	_	dB
29	_		_				_	dB
30	_						_	dB
31	_		_				_	dB

Related Information

SPICE Models for Altera Devices

Provides the Arria V HSSI HSPICE models.

Transceiver Compliance Specification

The following table lists the physical medium attachment (PMA) specification compliance of all supported protocol for Arria V GX, GT, SX, and ST devices. For more information about the protocol parameter details and compliance specifications, contact your Altera Sales Representative.



Symbol	Parameter	Condition	Min	Тур	Max	Unit
t (67)	Period jitter for dedicated clock output	$F_{OUT} \ge 100 \text{ MHz}$	—	_	175	ps (p-p)
OUTPJ_DC	in integer PLL	$F_{OUT} < 100 \text{ MHz}$	—		17.5	mUI (p-p)
+ (67)	Period jitter for dedicated clock output	$F_{OUT} \ge 100 \text{ MHz}$	_		250 ⁽⁶⁸⁾ , 175 ⁽⁶⁹⁾	ps (p-p)
^L FOUTPJ_DC	in fractional PLL	F _{OUT} < 100 MHz	_		25 ⁽⁶⁸⁾ , 17.5 ⁽⁶⁹⁾	mUI (p-p)
t (67)	Cycle-to-cycle jitter for dedicated clock	$F_{OUT} \ge 100 \text{ MHz}$	—	_	175	ps (p-p)
OUTCCJ_DC	output in integer PLL	F _{OUT} < 100 MHz	—		17.5	mUI (p-p)
L (67)	Cycle-to-cycle jitter for dedicated clock	$F_{OUT} \ge 100 \text{ MHz}$	_		250 ⁽⁶⁸⁾ , 175 ⁽⁶⁹⁾	ps (p-p)
FOUTCCJ_DC	output in fractional PLL	F _{OUT} < 100 MHz	—	_	25 ⁽⁶⁸⁾ , 17.5 ⁽⁶⁹⁾	mUI (p-p)
t (67)(70)	Period jitter for clock output on a	$F_{OUT} \ge 100 \text{ MHz}$	—		600	ps (p-p)
OUTPJ_IO	regular I/O in integer PLL	F _{OUT} < 100 MHz	_		60	mUI (p-p)
t (67)(68)(70)	Period jitter for clock output on a	$F_{OUT} \ge 100 \text{ MHz}$	—		600	ps (p-p)
FOUTPJ_IO	regular I/O in fractional PLL	F _{OUT} < 100 MHz	_	_	60	mUI (p-p)
t (67)(70)	Cycle-to-cycle jitter for clock output on	$F_{OUT} \ge 100 \text{ MHz}$	_		600	ps (p-p)
OUTCCJ_IO	a regular I/O in integer PLL	F _{OUT} < 100 MHz	—	_	60	mUI (p-p)
t	Cycle-to-cycle jitter for clock output on	$F_{OUT} \ge 100 \text{ MHz}$	—		600	ps (p-p)
FOUTCCJ_IO	a regular I/O in fractional PLL	F _{OUT} < 100 MHz	_		60	mUI (p-p)



⁽⁶⁷⁾ Peak-to-peak jitter with a probability level of 10⁻¹² (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Memory Output Clock Jitter Specification for Arria V Devices table.

⁽⁶⁸⁾ This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05–0.95 must be \geq 1000 MHz.

⁽⁶⁹⁾ This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.20–0.80 must be \geq 1200 MHz.

⁽⁷⁰⁾ External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Arria V Devices table.

1-98 Document Revision History

Date	Version	Changes
July 2014	3.8	 Added a note in Table 3, Table 4, and Table 5: The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements. Updated V_{CC_HPS} specification in Table 5. Added a note in Table 19: Differential inputs are powered by V_{CCPD} which requires 2.5 V. Updated "Minimum differential eye opening at the receiver serial input pins" specification in Table 20 and Table 21. Updated description in "HPS PLL Specifications" section. Updated VCO range maximum specification in Table 39. Updated T_d and T_h specifications in Table 45. Added T_h specification in Table 47 and Figure 13. Updated a note in Figure 20, Figure 21, and Figure 23 as follows: Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required. Removed "Remote update only in AS mode" specification in Table 58. Added DCLK device initialization clock source specification in Table 60. Added description in "Configuration Files" section: The IOCSR .rbf size is specifically for the Configuration via Protocol (CvP) feature. Removed f_{MAX_RU_CLK} specification in Table 63.
February 2014	3.7	 Updated V_{CCRSTCLK_HPS} maximum specification in Table 1. Added V_{CC_AUX_SHARED} specification in Table 1.
December 2013	3.6	 Added "HPS PLL Specifications". Added Table 24, Table 39, and Table 40. Updated Table 1, Table 3, Table 5, Table 19, Table 20, Table 21, Table 38, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, Table 51, Table 55, Table 56, and Table 59. Updated Figure 7, Figure 13, Figure 15, Figure 16, and Figure 19. Removed table: GPIO Pulse Width for Arria V Devices.



Symbol	Description	Condition	Minimum ⁽¹¹⁴⁾	Typical	Maximum ⁽¹¹⁴⁾	Unit
VI	DC input voltage	_	-0.5	_	3.6	V
Vo	Output voltage		0		V _{CCIO}	V
 Т_	Operating junction temperature	Commercial	0		85	°C
1 j		Industrial	-40	_	100	°C
t	Power supply ramp time	Standard POR	200 µs	_	100 ms	
•RAMP		Fast POR	200 µs	—	4 ms	—

Recommended Transceiver Power Supply Operating Conditions

Table 2-6: Recommended Transceiver Power Supply Operating Conditions for Arria V GZ Devices

Symbol	Description	Minimum ⁽¹¹⁸⁾	Typical	Maximum ⁽¹¹⁸⁾	Unit
V _{CCA_GXBL}	Transceiver channel DLL nevver supply (left side)	2.85	3.0	3.15	V
(119), (120)	Transceiver channel PLL power supply (left side)	2.375	2.5	2.625	v
V _{CCA}	Transceiver channel DL newer supply (right side)	2.85	3.0	3.15	V
GXBR ⁽¹¹⁹⁾ , ⁽¹²⁰⁾	Transceiver channel FLL power supply (fight side)	2.375	2.5	2.625	
V _{CCHIP_L}	Transceiver hard IP power supply (left side)	0.82	0.85	0.88	V
V _{CCHSSI_L}	Transceiver PCS power supply (left side)	0.82	0.85	0.88	V
V _{CCHSSI_R}	Transceiver PCS power supply (right side)	0.82	0.85	0.88	V

⁽¹¹⁴⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹¹⁸⁾ This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹²⁰⁾ When using ATX PLLs, the supply must be 3.0 V.



⁽¹¹⁹⁾ This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

Sumbol	Description	Conditions	Resistance	Unit	
Symbol	Description	Conditions	C3, I3L	C4, I4	Unit
25-Ω R _S	Internal series termination without calibration (25- Ω setting)	V_{CCIO} = 1.8 and 1.5 V	±40	±40	%
25-Ω R _S	Internal series termination without calibration (25- Ω setting)	$V_{CCIO} = 1.2 V$	±50	±50	%
50-Ω R _S	Internal series termination without calibration (50- Ω setting)	V_{CCIO} = 1.8 and 1.5 V	±40	±40	%
50-Ω R _S	Internal series termination without calibration (50- Ω setting)	$V_{CCIO} = 1.2 V$	±50	±50	%
100-Ω R _D	Internal differential termination (100- Ω setting)	$V_{CCIO} = 2.5 V$	±25	±25	%

Figure 2-1: OCT Variation Without Re-Calibration for Arria V GZ Devices

$$\mathbf{R}_{\text{OCT}} = \mathbf{R}_{\text{SCAL}} \left(1 + \left(\frac{dR}{dT} \times \bigtriangleup T \right) \pm \left(\frac{dR}{dV} \times \bigtriangleup V \right) \right)$$

Notes:

1. The R_{oct} value shows the range of OCT resistance with the variation of temperature and V_{ccio} . 2. R_{scAL} is the OCT resistance value at power-up. 3. ΔT is the variation of temperature with respect to the temperature at power-up. 4. ΔV is the variation of voltage with respect to the V_{ccio} at power-up. 5. dR/dT is the percentage change of R_{scAL} with temperature. 6. dR/dV is the percentage change of R_{scAL} with voltage

6. dR/dV is the percentage change of R_{SCAL} with voltage.

Table 2-12: OCT Variation after Power-Up Calibration for Arria V GZ Devices

Valid for a V_{CCIO} range of \pm 5% and a temperature range of 0° to 85°C.





Hot Socketing

Table 2-14: Hot Socketing Specifications for Arria V GZ Devices

Symbol	Description	Maximum
I _{IOPIN (DC)}	DC current per I/O pin	300 µA
I _{IOPIN (AC)}	AC current per I/O pin	8 mA ⁽¹²⁴⁾
I _{XCVR-TX (DC)}	DC current per transceiver transmitter pin	100 mA
I _{XCVR-RX (DC)}	DC current per transceiver receiver pin	50 mA

Internal Weak Pull-Up Resistor

Table 2-15: Internal Weak Pull-Up Resistor for Arria V GZ Devices

All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins. The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 k Ω .

Symbol	Description	V _{CCIO} Conditions (V) ⁽¹²⁵⁾	Value ⁽¹²⁶⁾	Unit
		3.0 ±5%	25	kΩ
V		2.5 ±5%	25	kΩ
	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option.	1.8 ±5%	25	kΩ
R _{PU}		1.5 ±5%	25	kΩ
		1.35 ±5%	25	kΩ
		1.25 ±5%	25	kΩ
		1.2 ±5%	25	kΩ

⁽¹²⁴⁾ The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.





 $^{^{(125)}}$ The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO} .

 $^{^{(126)}}$ These specifications are valid with a ±10% tolerance to cover changes over PVT.

I/O Standard	V _{CCIO} (V)			V _{DIF(DC)} (V)		V _{X(AC)} (V)		V _{CM(DC)} (V)			V _{DIF(AC)} (V)		
	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Max
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V _{CCIO} + 0.3		$0.5 \times V_{CCIO}$	_	$0.4 \times V_{CCIO}$	0.5 × V _{CC} IO	$0.6 \times V_{CCIO}$	0.3	V _{CCIO} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5 × V _{CCIO} – 0.12	$0.5 \times V_{CCIO}$	$0.5 \times V_{CCIO} + 0.12$	$0.4 \times V_{CCIO}$	0.5 × V _{CC} IO	0.6 × V _{CCIO}	0.44	0.44

Table 2-21: Differential I/O Standard Specifications for Arria V GZ Devices

I/O Standard	V _{CCIO} (V) ⁽¹²⁸⁾		V _{ID} (mV) ⁽¹²⁹⁾		V _{ICM(DC)} (V)		V _{OD} (V) ⁽¹³⁰⁾		0)	V _{OCM} (V) ⁽¹³⁰⁾		(0)			
	Min	Тур	Max	Min	Condition	Max	Min	Condition	Max	Min	Тур	Max	Min	Тур	Max
PCML	Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to the "Transceiver Performance Specifications" section.														
2.5 V	2 375	25	2 625	100	V _{CM} =		0.05	D _{MAX} ≤ 700 Mbps	1.8	0.247	—	0.6	1.125	1.25	1.375
(131)	2.373	2.5	2.025	100	1.25 V		1.05	D _{MAX} > 700 Mbps	1.55	0.247	—	0.6	1.125	1.25	1.375
BLVDS (132)	2.375	2.5	2.625	100						_	_			—	

⁽¹²⁸⁾ Differential inputs are powered by VCCPD which requires 2.5 V.



⁽¹²⁹⁾ The minimum VID value is applicable over the entire common mode range, VCM.

⁽¹³⁰⁾ RL range: $90 \le \text{RL} \le 110 \Omega$.

⁽¹³¹⁾ For optimized LVDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.

 $^{^{(132)}}$ There are no fixed V_{ICM}, V_{OD}, and V_{OCM} specifications for BLVDS. They depend on the system topology.

Symbol	V _{OD} Setting	V _{OD} Value (mV)	V _{OD} Setting	V _{OD} Value (mV)
	15	300	47	940
	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
V_{OD} differential peak to peak typical	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260



t_{ARESET}

Symbol	Parameter	Min	Тур	Max	Unit
f	Output frequency for an internal global or regional clock (C3, I3L speed grade)	_	_	650	MHz
OUT	Output frequency for an internal global or regional clock (C4, I4 speed grade)	_		580	MHz
f (169)	Output frequency for an external clock output (C3, I3L speed grade)	_	_	667	MHz
LOUT_EXT	Output frequency for an external clock output (C4, I4 speed grade)	_	_	533	MHz
toutduty	Duty cycle for a dedicated external clock output (when set to 50%)	45	50	55	%
t _{FCOMP}	External feedback clock compensation time	—		10	ns
f _{DYCONFIGCLK}	Dynamic configuration clock for mgmt_clk and scanclk	_	_	100	MHz
t _{LOCK}	Time required to lock from the end-of-device configuration or deassertion of areset		_	1	ms
t _{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/ delays)	—	—	1	ms
	PLL closed-loop low bandwidth	_	0.3		MHz
f _{CLBW}	PLL closed-loop medium bandwidth	—	1.5		MHz
	PLL closed-loop high bandwidth (170)	_	4		MHz
t _{PLL_PSERR}	Accuracy of PLL phase shift	_	_	±50	ps

10

_

Minimum pulse width on the areset signal





ns

 $^{^{(169)}}$ This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.

⁽¹⁷⁰⁾ High bandwidth PLL settings are not supported in external feedback mode.

Symbol	Parameter	Min	Тур	Max	Unit
k _{VALUE}	Numerator of Fraction	128	8388608	2147483648	—
f _{RES}	Resolution of VCO frequency ($f_{INPFD} = 100 \text{ MHz}$)	390625	5.96	0.023	Hz

Related Information

- Duty Cycle Distortion (DCD) Specifications on page 2-56
- DLL Range Specifications on page 2-53

DSP Block Specifications

Table 2-35: DSP Block Performance Specifications for Arria V GZ Devices

Mada	Performance			Unit	
Mode	C3, I3L	C4	14	Onit	
Modes using One DSP Block					
Three 9 × 9	480	420		MHz	
One 18 × 18	480	420	400	MHz	
Two partial 18×18 (or 16×16)	480	420	400	MHz	
One 27 × 27	400	350		MHz	
One 36 × 18	400	350		MHz	
One sum of two 18×18 (One sum of two 16×16)	400	350		MHz	
One sum of square	400	350		MHz	
One 18×18 plus $36 (a \times b) + c$	400	350		MHz	
Modes using Two DSP Blocks					
Three 18 × 18	400	350		MHz	
One sum of four 18×18	380	300		MHz	



Active Serial Configuration Timing

Figure 2-9: AS Configuration Timing



Timing waveform for the active serial (AS) x1 mode and AS x4 mode configuration timing.

Notes:

1. If you are using AS ×4 mode, this signal represents the AS_DATA[3..0] and ERCQ sends in 4-bits of data for each DCLKcycle.

2. The initialization clock can be from internal oscillator or CLKUSR pin

3. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE ges low.

Table 2-58: AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices

The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in the "PS Timing Parameters for Arria V GZ Devices" table.



Term	Definition		
	Single-Ended WaveformVODPositive Channel (p) = VOHVCMNegative Channel (n) = VOLGroundGround		
	Differential Waveform V_{0D} V_{0D} V_{0D} V_{0D}		
f _{HSCLK}	Left and right PLL input clock frequency.		
f _{HSDR}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDR} = 1/TUI), non-DPA.		
f _{hsdrdpa}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDRDPA} = 1/TUI), DPA.		
J	High-speed I/O block—Deserialization factor (width of parallel data bus).		







