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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	19811
Number of Logic Elements/Cells	420000
Total RAM Bits	23625728
Number of I/O	704
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxbb5d4f40c5n

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Symbol	Description	Condition	Minimum ⁽¹⁾	Typical	Maximum ⁽¹⁾	Unit
V_{CC}	Core voltage power supply	–C4, –I5, –C5, –C6	1.07	1.1	1.13	V
		–I3	1.12	1.15	1.18	V
V_{CCP}	Periphery circuitry, PCIe hard IP block, and transceiver PCS power supply	–C4, –I5, –C5, –C6	1.07	1.1	1.13	V
		–I3	1.12	1.15	1.18	V
V_{CCPGM}	Configuration pins power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
V_{CC_AUX}	Auxiliary supply	—	2.375	2.5	2.625	V
$V_{CCBAT}^{(2)}$	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V
$V_{CCPD}^{(3)}$	I/O pre-driver power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V

⁽¹⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽²⁾ If you do not use the design security feature in Arria V devices, connect V_{CCBAT} to a 1.5-V, 2.5-V, or 3.0-V power supply. Arria V power-on reset (POR) circuitry monitors V_{CCBAT} . Arria V devices do not exit POR if V_{CCBAT} is not powered up.

⁽³⁾ V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25, or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V. V_{CCPD} must be 3.3 V when V_{CCIO} is 3.3 V.

Parameter	Symbol	Condition	V _{CCIO} (V)												Unit
			1.2		1.5		1.8		2.5		3.0		3.3		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold trip point	V _{TRIP}	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 1-8: OCT Calibration Accuracy Specifications for Arria V Devices

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (V)	Calibration Accuracy			Unit
			-I3, -C4	-I5, -C5	-C6	
25- Ω R_S	Internal series termination with calibration (25- Ω setting)	$V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2$	± 15	± 15	± 15	%
50- Ω R_S	Internal series termination with calibration (50- Ω setting)	$V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2$	± 15	± 15	± 15	%
34- Ω and 40- Ω R_S	Internal series termination with calibration (34- Ω and 40- Ω setting)	$V_{CCIO} = 1.5, 1.35, 1.25, 1.2$	± 15	± 15	± 15	%
48- Ω , 60- Ω , and 80- Ω R_S	Internal series termination with calibration (48- Ω , 60- Ω , and 80- Ω setting)	$V_{CCIO} = 1.2$	± 15	± 15	± 15	%
50- Ω R_T	Internal parallel termination with calibration (50- Ω setting)	$V_{CCIO} = 2.5, 1.8, 1.5, 1.2$	-10 to +40	-10 to +40	-10 to +40	%
20- Ω , 30- Ω , 40- Ω , 60- Ω , and 120- Ω R_T	Internal parallel termination with calibration (20- Ω , 30- Ω , 40- Ω , 60- Ω , and 120- Ω setting)	$V_{CCIO} = 1.5, 1.35, 1.25$	-10 to +40	-10 to +40	-10 to +40	%

I/O Standard	V_{CCIO} (V)			V_{ID} (mV) ⁽¹⁶⁾			$V_{ICM(DC)}$ (V)			V_{OD} (V) ⁽¹⁷⁾			V_{OCM} (V) ⁽¹⁷⁾⁽¹⁸⁾		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Transceiver Specifications for Arria V GX and SX Devices and Transceiver Specifications for Arria V GT and ST Devices tables.														
2.5 V LVDS ⁽¹⁹⁾	2.375	2.5	2.625	100	$V_{CM} = 1.25$ V	—	0.05	$D_{MAX} \leq 1.25$ Gbps	1.80	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	$D_{MAX} > 1.25$ Gbps	1.55						
RSDS (HIO) ⁽²⁰⁾	2.375	2.5	2.625	100	$V_{CM} = 1.25$ V	—	0.25	—	1.45	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO) ⁽²¹⁾	2.375	2.5	2.625	200	—	600	0.300	—	1.425	0.25	—	0.6	1	1.2	1.4
LVPECL ⁽²²⁾	—	—	—	300	—	—	0.60	$D_{MAX} \leq 700$ Mbps	1.80	—	—	—	—	—	—
							1.00	$D_{MAX} > 700$ Mbps	1.60						

Related Information

- [Transceiver Specifications for Arria V GX and SX Devices](#) on page 1-23
Provides the specifications for transmitter, receiver, and reference clock I/O pin.

⁽¹⁶⁾ The minimum V_{ID} value is applicable over the entire common mode range, V_{CM} .

⁽¹⁷⁾ R_L range: $90 \leq R_L \leq 110 \Omega$.

⁽¹⁸⁾ This applies to default pre-emphasis setting only.

⁽¹⁹⁾ For optimized LVDS receiver performance, the receiver voltage input range must be within 1.0 V to 1.6 V for data rates above 1.25 Gbps and 0 V to 1.85 V for data rates below 1.25 Gbps.

⁽²⁰⁾ For optimized RSDS receiver performance, the receiver voltage input range must be within 0.25 V to 1.45 V.

⁽²¹⁾ For optimized Mini-LVDS receiver performance, the receiver voltage input range must be within 0.3 V to 1.425 V.

⁽²²⁾ For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rates above 700 Mbps and 0.45 V to 1.95 V for data rates below 700 Mbps.

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Inter-transceiver block transmitter channel-to-channel skew ⁽³⁹⁾	×N PMA bonded mode	—	—	500	—	—	500	ps

Table 1-24: CMU PLL Specifications for Arria V GX and SX Devices

Symbol/Description	Transceiver Speed Grade 4		Transceiver Speed Grade 6		Unit
	Min	Max	Min	Max	
Supported data range	611	6553.6	611	3125	Mbps
fPLL supported data range	611	3125	611	3125	Mbps

Table 1-25: Transceiver-FPGA Fabric Interface Specifications for Arria V GX and SX Devices

Symbol/Description	Transceiver Speed Grade 4 and 6		Unit
	Min	Max	
Interface speed (single-width mode)	25	187.5	MHz
Interface speed (double-width mode)	25	163.84	MHz

Related Information

- [CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain](#) on page 1-35
- [CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain](#) on page 1-36
- [Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines](#)
Provides more information about the power supply connection for different data rates.

⁽³⁹⁾ This specification is only applicable to channels on one side of the device across two transceiver banks.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Data rate (10-Gbps transceiver) ⁽⁴⁴⁾	—	0.611	—	10.3125	Gbps
Absolute V_{MAX} for a receiver pin ⁽⁴⁵⁾	—	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	—	—	—	2.2	V
Minimum differential eye opening at the receiver serial input pins ⁽⁴⁶⁾	—	100	—	—	mV
V_{ICM} (AC coupled)	—	—	750 ⁽⁴⁷⁾ /800	—	mV
V_{ICM} (DC coupled)	$\leq 3.2\text{Gbps}$ ⁽⁴⁸⁾	670	700	730	mV
Differential on-chip termination resistors	85- Ω setting	85			Ω
	100- Ω setting	100			Ω
	120- Ω setting	120			Ω
	150- Ω setting	150			Ω
t_{LTR} ⁽⁴⁹⁾	—	—	—	10	μs
t_{LTD} ⁽⁵⁰⁾	—	4	—	—	μs

⁽⁴⁵⁾ The device cannot tolerate prolonged operation at this absolute maximum.

⁽⁴⁶⁾ The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

⁽⁴⁷⁾ The AC coupled V_{ICM} is 750 mV for PCIe mode only.

⁽⁴⁸⁾ For standard protocol compliance, use AC coupling.

⁽⁴⁹⁾ t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

⁽⁵⁰⁾ t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedto data signal goes high.

Memory Output Clock Jitter Specifications

Table 1-45: Memory Output Clock Jitter Specifications for Arria V Devices

The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

The memory output clock jitter is applicable when an input jitter of 30 ps (p-p) is applied with bit error rate (BER) 10^{-12} , equivalent to 14 sigma.

Altera recommends using the UniPHY intellectual property (IP) with PHYCLK connections for better jitter performance.

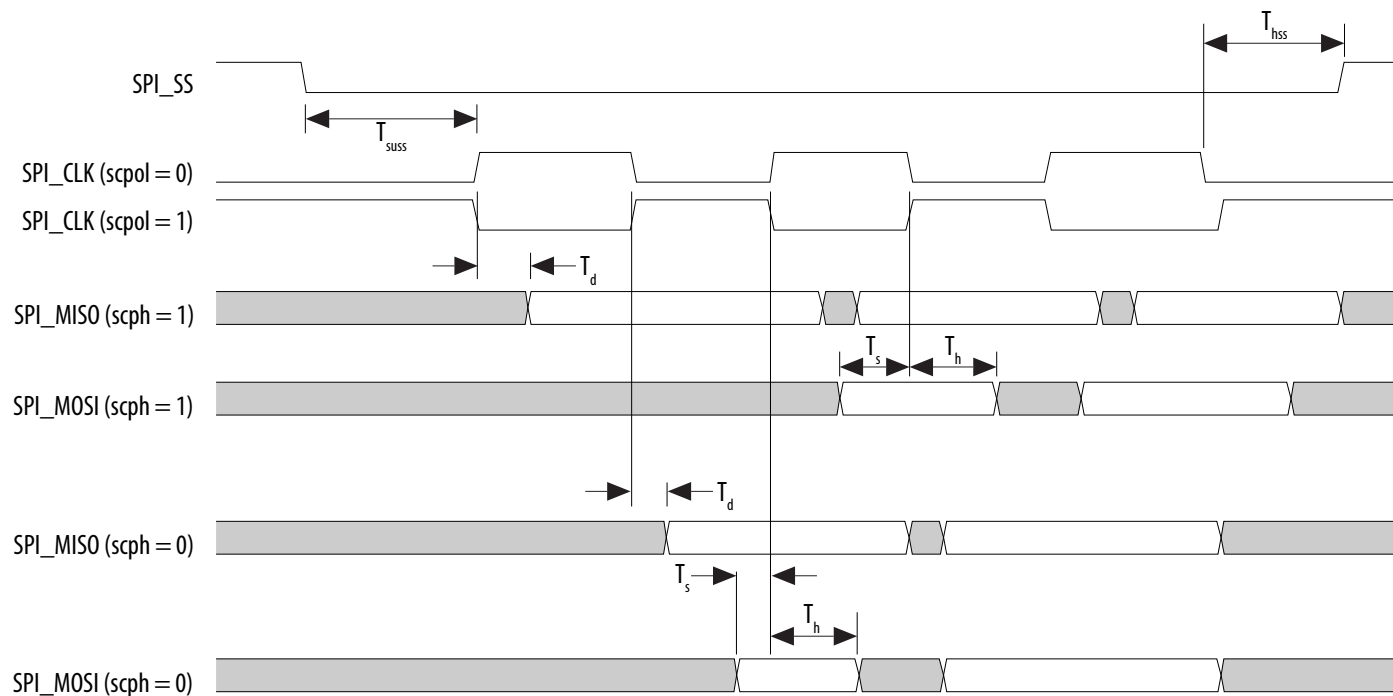
Parameter	Clock Network	Symbol	-I3, -C4		-I5, -C5		-C6		Unit
			Min	Max	Min	Max	Min	Max	
Clock period jitter	PHYCLK	$t_{JIT(per)}$	-41	41	-50	50	-55	55	ps
Cycle-to-cycle period jitter	PHYCLK	$t_{JIT(cc)}$	63		90		94		ps

OCT Calibration Block Specifications

Table 1-46: OCT Calibration Block Specifications for Arria V Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for R_S OCT/ R_T OCT calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	—	2.5	—	ns

Figure 1-10: SPI Slave Timing Diagram

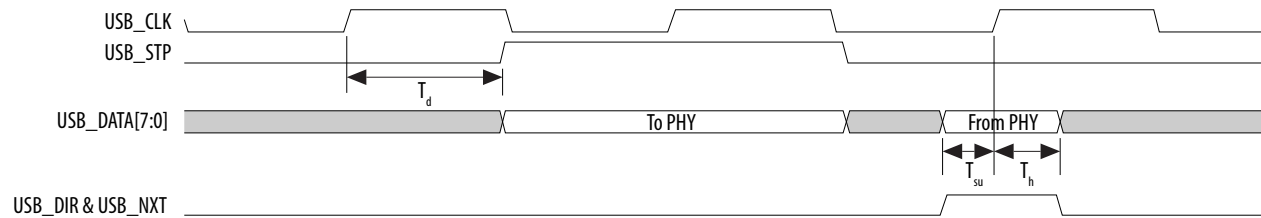
**Related Information****SPI Controller, Arria V Hard Processor System Technical Reference Manual**

Provides more information about rx_sample_delay.

SD/MMC Timing Characteristics**Table 1-54: Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices**

After power up or cold reset, the Boot ROM uses `drvsel = 3` and `smplsel = 0` to execute the code. At the same time, the SD/MMC controller enters the Identification Phase followed by the Data Phase. During this time, the value of interface output clock `SDMMC_CLK_OUT` changes from a maximum of 400 kHz (Identification Phase) up to a maximum of 12.5 MHz (Data Phase), depending on the internal reference clock `SDMMC_CLK` and the `CSEL` setting. The value of `SDMMC_CLK` is based on the external oscillator frequency and has a maximum value of 50 MHz.

Figure 1-12: USB Timing Diagram



Ethernet Media Access Controller (EMAC) Timing Characteristics

Table 1-56: Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements for Arria V Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	TX_CLK clock period	—	8	—	ns
T_{clk} (100Base-T)	TX_CLK clock period	—	40	—	ns
T_{clk} (10Base-T)	TX_CLK clock period	—	400	—	ns
$T_{duty cycle}$	TX_CLK duty cycle	45	—	55	%
T_d	TX_CLK to TXD/TX_CTL output data delay	-0.85	—	0.15	ns

Figure 1-13: RGMII TX Timing Diagram

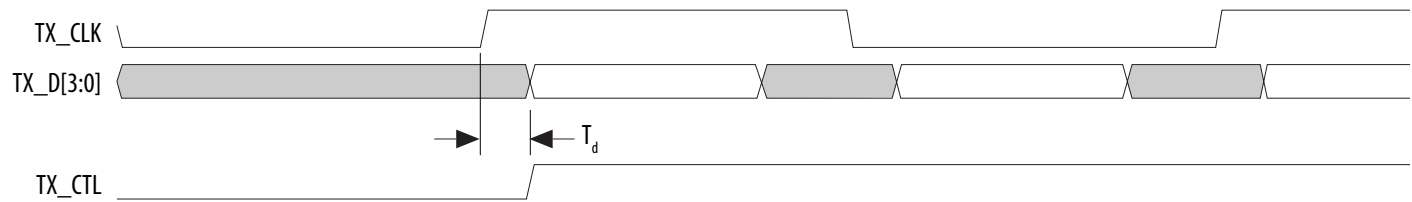
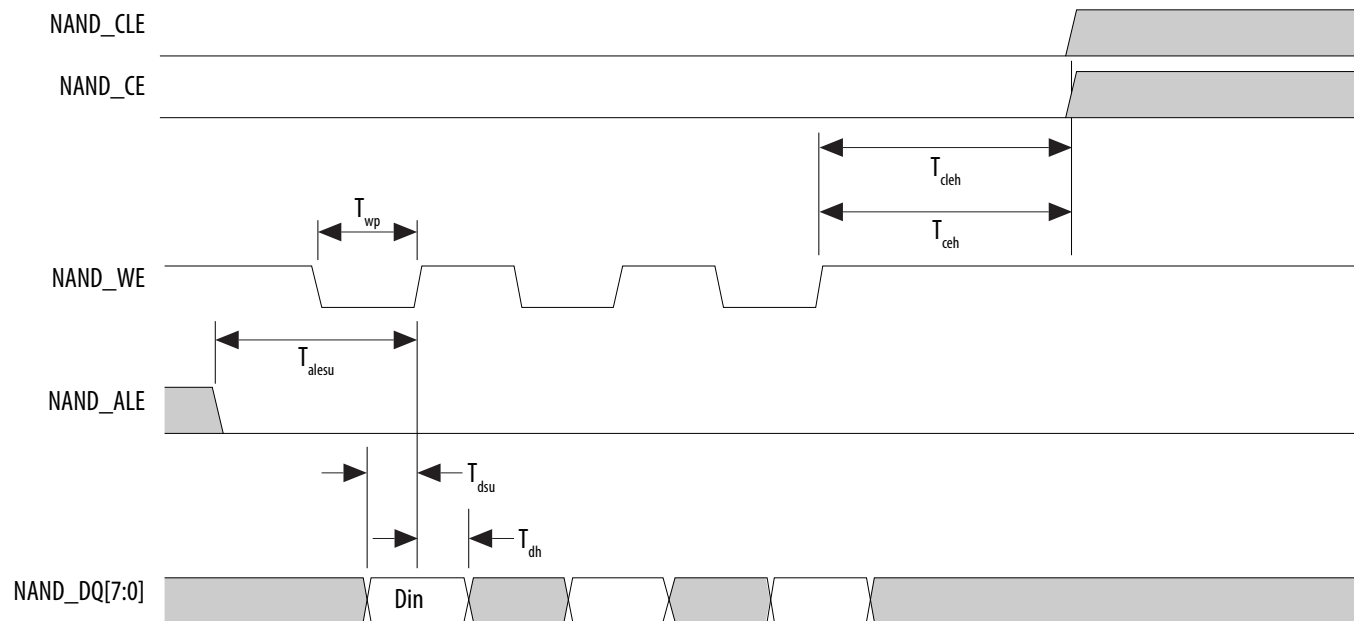


Figure 1-19: NAND Data Write Timing Diagram



Variant	Member Code	Active Serial ⁽¹⁰⁸⁾			Fast Passive Parallel ⁽¹⁰⁹⁾		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
Arria V GX	A1	4	100	178	16	125	36
	A3	4	100	178	16	125	36
	A5	4	100	255	16	125	51
	A7	4	100	255	16	125	51
	B1	4	100	344	16	125	69
	B3	4	100	344	16	125	69
	B5	4	100	465	16	125	93
	B7	4	100	465	16	125	93
Arria V GT	C3	4	100	178	16	125	36
	C7	4	100	255	16	125	51
	D3	4	100	344	16	125	69
	D7	4	100	465	16	125	93
Arria V SX	B3	4	100	465	16	125	93
	B5	4	100	465	16	125	93
Arria V ST	D3	4	100	465	16	125	93
	D5	4	100	465	16	125	93

Related Information**Configuration Files** on page 1-83⁽¹⁰⁸⁾ DCLK frequency of 100 MHz using external CLKUSR.⁽¹⁰⁹⁾ Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Date	Version	Changes
January 2015	2015.01.30	- Updated the description for $V_{CC_AUX_SHARED}$ to “HPS auxiliary power supply” in the following tables: - Absolute Maximum Ratings for Arria V Devices - HPS Power Supply Operating Conditions for Arria V SX and ST Devices - Added statement in I/O Standard Specifications: You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards. - Updated the conditions for transceiver reference clock rise time and fall time: Measure at ± 60 mV of differential signal. Added a note to the conditions: REFCLK performance requires to meet transmitter REFCLK phase noise specification. - Updated the description in Periphery Performance Specifications to mention that proper timing closure is required in design. - Updated HPS Clock Performance main_base_clk specifications from 525 MHz (for –I3 speed grade) and 462 MHz (for –C4 speed grade) to 400 MHz. - Updated HPS PLL VCO maximum frequency to 1,600 MHz (for –C5, –I5, and –C6 speed grades), 1,850 MHz (for –C4 speed grade), and 2,100 MHz (for –I3 speed grade). - Changed the symbol for HPS PLL input jitter divide value from NR to N. - Removed “Slave select pulse width (Texas Instruments SSP mode)” parameter from the following tables: - SPI Master Timing Requirements for Arria V Devices - SPI Slave Timing Requirements for Arria V Devices - Added descriptions to USB Timing Characteristics section in HPS Specifications: PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board. - Added HPS JTAG timing specifications. - Updated FPGA JTAG timing specifications note as follows: A 1-ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, $t_{pCO} = 13$ ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V. - Updated the value in the V_{ICM} (AC Coupled) row and in note 6 from 650 mV to 750 mV in the Transceiver Specifications for Arria V GT and ST Devices table.

Date	Version	Changes
August 2013	3.5	- Removed “Pending silicon characterization” note in Table 29. - Updated Table 25.
August 2013	3.4	- Removed Preliminary tags for Table 1, Table 2, Table 3, Table 4, Table 5, Table 6, Table 7, Table 9, Table 12, Table 13, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, Table 21, Table 22, Table 23, Table 24, Table 25, Table 26, Table 27, Table 28, Table 29, Table 30, Table 31, Table 35, Table 36, Table 51, Table 53, Table 54, Table 55, Table 56, Table 57, Table 60, Table 62, and Table 64. - Updated Table 1, Table 3, Table 11, Table 19, Table 20, Table 21, Table 22, Table 25, and Table 29.
June 2013	3.3	Updated Table 20, Table 21, Table 25, and Table 38.
May 2013	3.2	- Added Table 37. - Updated Figure 8, Figure 9, Figure 20, Figure 22, and Figure 23. - Updated Table 1, Table 5, Table 10, Table 13, Table 19, Table 20, Table 21, Table 23, Table 29, Table 39, Table 40, Table 46, Table 56, Table 57, Table 60, and Table 64. - Updated industrial junction temperature range for –I3 speed grade in “PLL Specifications” section.
March 2013	3.1	- Added HPS reset information in the “HPS Specifications” section. - Added Table 60. - Updated Table 1, Table 3, Table 17, Table 20, Table 29, and Table 59. - Updated Figure 21.

I/O Standard	$V_{IL(DC)} (V)$		$V_{IH(DC)} (V)$		$V_{IL(AC)} (V)$	$V_{IH(AC)} (V)$	$V_{OL} (V)$	$V_{OH} (V)$	$I_{ol} (mA)$	$I_{oh} (mA)$
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-18 Class II	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCIO} + 0.3$	$V_{REF} - 0.25$	$V_{REF} + 0.25$	0.28	$V_{CCIO} - 0.28$	13.4	-13.4
SSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	8	-8
SSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	16	-16
SSTL-135 Class I, II	—	$V_{REF} - 0.09$	$V_{REF} + 0.09$	—	$V_{REF} - 0.16$	$V_{REF} + 0.16$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	—	—
SSTL-125 Class I, II	—	$V_{REF} - 0.85$	$V_{REF} + 0.85$	—	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	—	—
SSTL-12 Class I, II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	—	—
HSTL-18 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-18 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-12 Class I	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	16	-16
HSUL-12	—	$V_{REF} - 0.13$	$V_{REF} + 0.13$	—	$V_{REF} - 0.22$	$V_{REF} + 0.22$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	—	—

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
fixedclk clock frequency	PCIe Receiver Detect	—	100 or 125	—	—	100 or 125	—	MHz
Reconfiguration clock (mgmt_clk_clk) frequency	—	100	—	125	100	—	125	MHz

Related Information[Arria V Device Overview](#)

For more information about device ordering codes.

Receiver**Table 2-24: Receiver Specifications for Arria V GZ Devices**

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported I/O Standards	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS							
Data rate (Standard PCS) ⁽¹⁴³⁾ , ⁽¹⁴⁴⁾	—	600	—	9900	600	—	8800	Mbps
Data rate (10G PCS) ⁽¹⁴³⁾ , ⁽¹⁴⁴⁾	—	600	—	12500	600	—	10312.5	Mbps
Absolute V _{MAX} for a receiver pin ⁽¹⁴⁵⁾	—	—	—	1.2	—	—	1.2	V
Absolute V _{MIN} for a receiver pin	—	−0.4	—	—	−0.4	—	—	V

⁽¹⁴³⁾ The line data rate may be limited by PCS-FPGA interface speed grade.

⁽¹⁴⁴⁾ To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

⁽¹⁴⁵⁾ The device cannot tolerate prolonged operation at this absolute maximum.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Programmable DC gain	DC gain setting = 0	—	0	—	—	0	—	dB
	DC gain setting = 1	—	2	—	—	2	—	dB
	DC gain setting = 2	—	4	—	—	4	—	dB
	DC gain setting = 3	—	6	—	—	6	—	dB
	DC gain setting = 4	—	8	—	—	8	—	dB

Related Information[Arria V Device Overview](#)

For more information about device ordering codes.

Transmitter**Table 2-25: Transmitter Specifications for Arria V GZ Devices**

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported I/O Standards	1.4-V and 1.5-V PCML							
Data rate (Standard PCS)	—	600	—	9900	600	—	8800	Mbps
Data rate (10G PCS)	—	600	—	12500	600	—	10312.5	Mbps

Symbol	V _{OD} Setting	V _{OD} Value (mV)	V _{OD} Setting	V _{OD} Value (mV)
V _{OD} differential peak to peak typical	15	300	47	940
	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260

Table 2-57: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is > 1

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	μ s
t_{STATUS}	nSTATUS low pulse width	268	1,506 ⁽²¹⁰⁾	μ s
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽²¹¹⁾	μ s
t_{CF2CK} ⁽²¹²⁾	nCONFIG high to first rising edge on DCLK	1,506	—	μ s
t_{ST2CK} ⁽²¹²⁾	nSTATUS high to first rising edge of DCLK	2	—	μ s
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N - 1/f_{DCLK}$ ⁽²¹³⁾	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP $\times 8/\times 16$)	—	125	MHz
	DCLK frequency (FPP $\times 32$)	—	100	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode ⁽²¹⁴⁾	175	437	μ s

⁽²¹⁰⁾ You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

⁽²¹¹⁾ You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

⁽²¹²⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

⁽²¹³⁾ N is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.

⁽²¹⁴⁾ The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

Table 2-62: Uncompressed .rbf Sizes for Arria V GZ Devices

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ⁽²²³⁾
Arria V GZ	E1	137,598,880	562,208
	E3	137,598,880	562,208
	E5	213,798,880	561,760
	E7	213,798,880	561,760

Table 2-63: Minimum Configuration Time Estimation for Arria V GZ Devices

Variant	Member Code	Active Serial ⁽²²⁴⁾			Fast Passive Parallel ⁽²²⁵⁾		
		Width	DCLK (MHz)	Min Config Time (ms)	Width	DCLK (MHz)	Min Config Time (ms)
Arria V GZ	E1	4	100	344	32	100	43
	E3	4	100	344	32	100	43
	E5	4	100	534	32	100	67
	E7	4	100	534	32	100	67

Remote System Upgrades Circuitry Timing Specification

Table 2-64: Remote System Upgrade Circuitry Timing Specifications

Parameter	Minimum	Maximum	Unit
$t_{RU_nCONFIG}$ ⁽²²⁶⁾	250	—	ns
$t_{RU_nRSTIMER}$ ⁽²²⁷⁾	250	—	ns

⁽²²³⁾ The IOCSR .rbf size is specifically for the Configuration via Protocol (CvP) feature.

⁽²²⁴⁾ DCLK frequency of 100 MHz using external CLKUSR.

⁽²²⁵⁾ Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Date	Version	Changes
July 2014	3.8	- Updated Table 21. - Updated Table 22 V_{OCM} (DC Coupled) condition. - Updated the DCLK note to Figure 6, Figure 7, and Figure 9. - Added note to Table 5 and Table 6. - Added the DCLK specification to Table 50. - Added note to Table 51. - Updated the list of parameters in Table 53.
February 2014	3.7	Updated Table 28.
December 2013	3.6	- Updated Table 2, Table 13, Table 18, Table 19, Table 22, Table 30, Table 33, Table 37, Table 38, Table 45, Table 46, Table 47, Table 56, Table 49. - Updated “PLL Specifications”.
August 2013	3.5	Updated Table 28.
August 2013	3.4	- Removed Preliminary tags for Table 2, Table 4, Table 5, Table 14, Table 27, Table 28, Table 29, Table 31, Table 32, Table 43, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, and Table 54. - Updated Table 2 and Table 28.
June 2013	3.3	Updated Table 23, Table 28, Table 51, and Table 55.
May 2013	3.2	- Added Table 23. - Updated Table 5, Table 22, Table 26, and Table 57. - Updated Figure 6, Figure 7, Figure 8, and Figure 9.
March 2013	3.1	- Updated Table 2, Table 6, Table 7, Table 8, Table 19, Table 22, Table 26, Table 29, Table 52. - Updated “Maximum Allowed Overshoot and Undershoot Voltage”.
December 2012	3.0	Initial release.