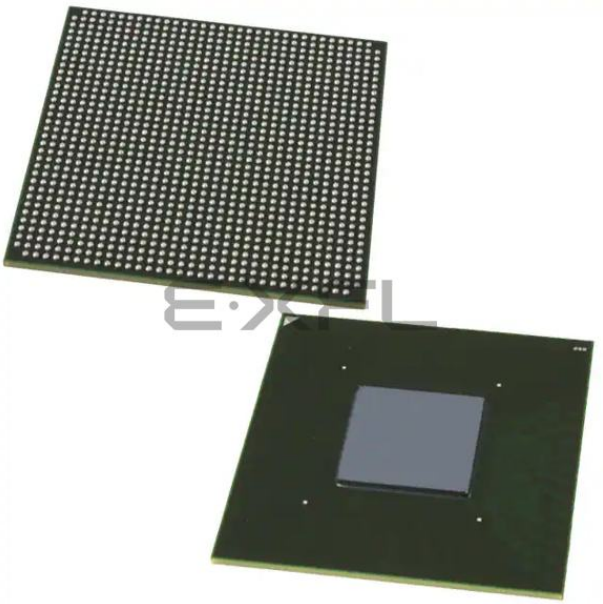

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Details	
Product Status	Obsolete
Number of LABs/CLBs	23780
Number of Logic Elements/Cells	504000
Total RAM Bits	27695104
Number of I/O	544
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxbb7d4f35c5n

Figure 1-1: Equation for OCT Variation Without Recalibration

$$R_{OCT} = R_{SCAL}\left(1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle\right)$$

The definitions for the equation are as follows:

- The R_{OCT} value calculated shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
- R_{SCAL} is the OCT resistance value at power-up.
- ΔT is the variation of temperature with respect to the temperature at power up.
- ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
- dR/dT is the percentage change of R_{SCAL} with temperature.
- dR/dV is the percentage change of R_{SCAL} with voltage.

OCT Variation after Power-Up Calibration

Table 1-10: OCT Variation after Power-Up Calibration for Arria V Devices

This table lists OCT variation with temperature and voltage after power-up calibration. The OCT variation is valid for a V_{CCIO} range of ±5% and a temperature range of 0°C to 85°C.

Symbol	Description	V_{CCIO} (V)	Value	Unit
dR/dV	OCT variation with voltage without recalibration	3.0	0.100	%/mV
		2.5	0.100	
		1.8	0.100	
		1.5	0.100	
		1.35	0.150	
		1.25	0.150	
		1.2	0.150	

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Spread-spectrum modulating clock frequency	PCI Express® (PCIe)	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	Ω
V_{ICM} (AC coupled)	—	—	1.1/1.15[26]	—	—	1.1/1.15[26]	—	V
V_{ICM} (DC coupled)	HCSL I/O standard for the PCIe reference clock	250	—	550	250	—	550	mV
Transmitter REFCLK phase noise[27]	10 Hz	—	—	–50	—	—	–50	dBc/Hz
	100 Hz	—	—	–80	—	—	–80	dBc/Hz
	1 KHz	—	—	–110	—	—	–110	dBc/Hz
	10 KHz	—	—	–120	—	—	–120	dBc/Hz
	100 KHz	—	—	–120	—	—	–120	dBc/Hz
	≥1 MHz	—	—	–130	—	—	–130	dBc/Hz
R_{REF}	—	—	2000 ±1%	—	—	2000 ±1%	—	Ω

(26) For data rate ≤3.2 Gbps, connect $V_{CCR\_GXBL/R}$ to either 1.1-V or 1.15-V power supply. For data rate >3.2 Gbps, connect $V_{CCR\_GXBL/R}$ to a 1.15-V power supply. For details, refer to the Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines.

(27) The transmitter REFCLK phase jitter is 30 ps p-p at bit error rate (BER) 10^{-12}.

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Minimum differential eye opening at the receiver serial input pins[30]	—	100	—	—	100	—	—	mV
V_{ICM} (AC coupled)	—	—	0.7/0.75/ 0.8[31]	—	—	0.7/0.75/ 0.8 [31]	—	mV
V_{ICM} (DC coupled)	≤ 3.2Gbps[32]	670	700	730	670	700	730	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	—	85	—	Ω
	100-Ω setting	—	100	—	—	100	—	Ω
	120-Ω setting	—	120	—	—	120	—	Ω
	150-Ω setting	—	150	—	—	150	—	Ω
t_{LTR}[33]	—	—	—	10	—	—	10	µs
t_{LTD}[34]	—	4	—	—	4	—	—	µs
t_{LTD_manual}[35]	—	4	—	—	4	—	—	µs
$t_{LTR\_LTD\_manual}$[36]	—	15	—	—	15	—	—	µs
Programmable ppm detector[37]	—	±62.5, 100, 125, 200, 250, 300, 500, and 1000						ppm

(30) The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(31) The AC coupled V_{ICM} = 700 mV for Arria V GX and SX in PCIe mode only. The AC coupled V_{ICM} = 750 mV for Arria V GT and ST in PCIe mode only.

(32) For standard protocol compliance, use AC coupling.

(33) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

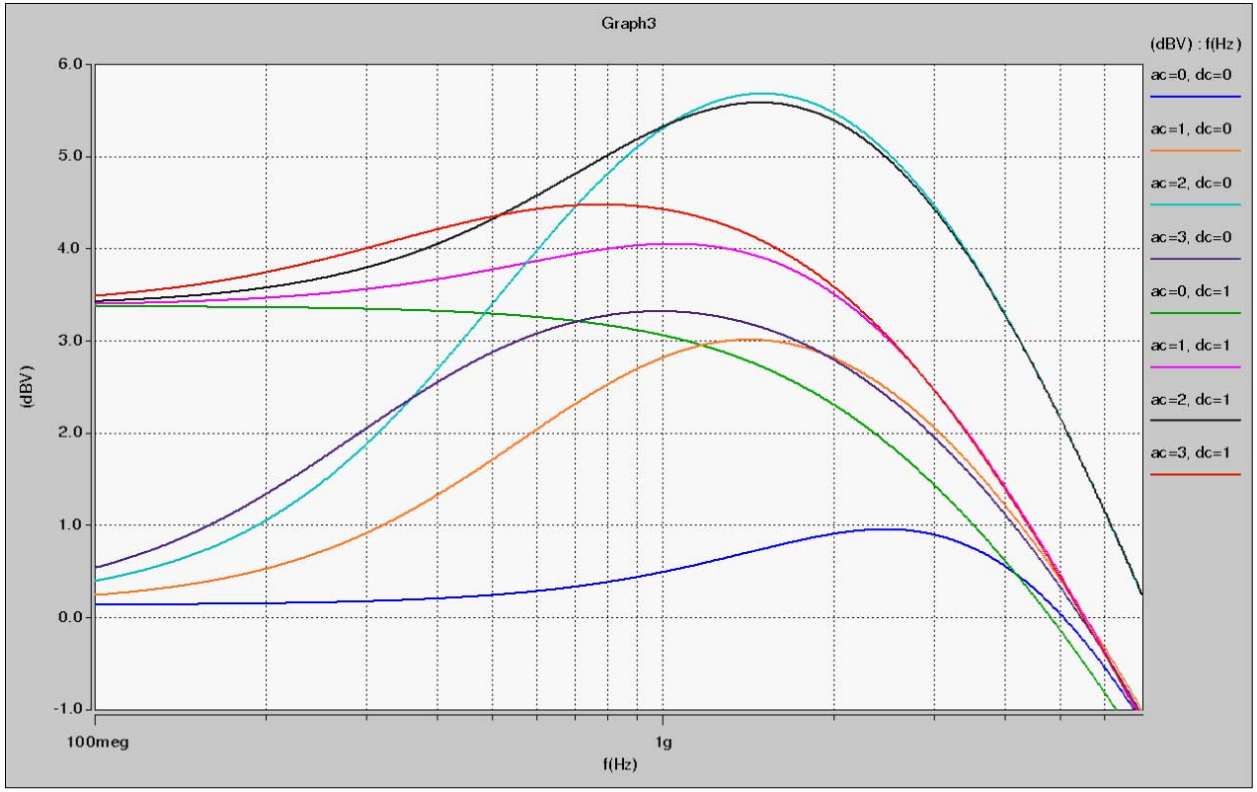
(34) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(35) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(36) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain

Figure 1-3: CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices



Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{OUTPJ_DC}[67]	Period jitter for dedicated clock output in integer PLL	$F_{OUT} \geq 100$ MHz	—	—	175	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	17.5	mUI (p-p)
t_{FOUTPJ_DC}[67]	Period jitter for dedicated clock output in fractional PLL	$F_{OUT} \geq 100$ MHz	—	—	250[68], 175[69]	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	25[68], 17.5[69]	mUI (p-p)
t_{OUTCCJ_DC}[67]	Cycle-to-cycle jitter for dedicated clock output in integer PLL	$F_{OUT} \geq 100$ MHz	—	—	175	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	17.5	mUI (p-p)
$t_{FOUTCCJ\_DC}$[67]	Cycle-to-cycle jitter for dedicated clock output in fractional PLL	$F_{OUT} \geq 100$ MHz	—	—	250[68], 175[69]	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	25[68], 17.5[69]	mUI (p-p)
t_{OUTPJ_IO}[67][70]	Period jitter for clock output on a regular I/O in integer PLL	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
t_{FOUTPJ_IO}[67][68][70]	Period jitter for clock output on a regular I/O in fractional PLL	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
t_{OUTCCJ_IO}[67][70]	Cycle-to-cycle jitter for clock output on a regular I/O in integer PLL	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
$t_{FOUTCCJ\_IO}$[67][68][70]	Cycle-to-cycle jitter for clock output on a regular I/O in fractional PLL	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)

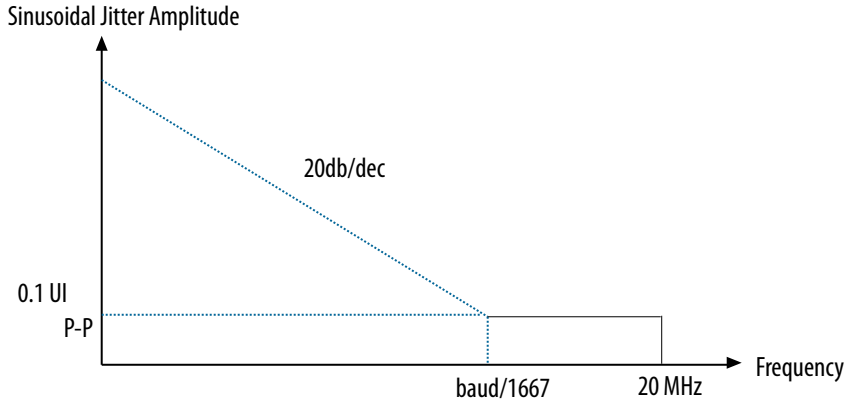
(67) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Memory Output Clock Jitter Specification for Arria V Devices table.

(68) This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05–0.95 must be ≥ 1000 MHz.

(69) This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.20–0.80 must be ≥ 1200 MHz.

(70) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Arria V Devices table.

Figure 1-6: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Less than 1.25 Gbps



DLL Frequency Range Specifications

Table 1-43: DLL Frequency Range Specifications for Arria V Devices

Parameter	–I3, –C4	–I5, –C5	–C6	Unit
DLL operating frequency range	200 – 667	200 – 667	200 – 667	MHz

DQS Logic Block Specifications

Table 1-44: DQS Phase Shift Error Specifications for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria V Devices

This error specification is the absolute maximum and minimum error.

Number of DQS Delay Buffer	–I3, –C4	–I5, –C5	–C6	Unit
2	40	80	80	ps

Symbol	Parameter	Minimum	Maximum	Unit
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} × CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

FPP Configuration Timing
Provides the FPP configuration timing waveforms.

AS Configuration Timing

Table 1-68: AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices

The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

The t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in PS Timing Parameters for Arria V Devices table. You can obtain the t_{CF2ST1} value if you do not delay configuration by externally holding nSTATUS low.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	2	ns
t_{SU}	Data setup time before the falling edge on DCLK	1.5	—	ns
t_{DH}	Data hold time after the falling edge on DCLK	0	—	ns
t_{CD2UM}	CONF_DONE high to user mode	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} × CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CK}[105]	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}[105]	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode[106]	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times$ CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

PS Configuration Timing

Provides the PS configuration timing waveform.

(105) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

(106) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Variant	Member Code	Active Serial[108]			Fast Passive Parallel[109]		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
Arria V GX	A1	4	100	178	16	125	36
	A3	4	100	178	16	125	36
	A5	4	100	255	16	125	51
	A7	4	100	255	16	125	51
	B1	4	100	344	16	125	69
	B3	4	100	344	16	125	69
	B5	4	100	465	16	125	93
	B7	4	100	465	16	125	93
Arria V GT	C3	4	100	178	16	125	36
	C7	4	100	255	16	125	51
	D3	4	100	344	16	125	69
	D7	4	100	465	16	125	93
Arria V SX	B3	4	100	465	16	125	93
	B5	4	100	465	16	125	93
Arria V ST	D3	4	100	465	16	125	93
	D5	4	100	465	16	125	93

Related Information

Configuration Files on page 1-83

(108) DCLK frequency of 100 MHz using external CLKUSR.

(109) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Rise time	Measure at ±60 mV of differential signal (138)	—	—	400	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal (138)	—	—	400	—	—	400	
Duty cycle	—	45	—	55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express ®(PCIe)	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5	—	—	0 to –0.5	—	%
On-chip termination resistors	—	—	100	—	—	100	—	Ω
Absolute V_{MAX}	Dedicated reference clock pin	—	—	1.6	—	—	1.6	V
	RX reference clock pin	—	—	1.2	—	—	1.2	
Absolute V_{MIN}	—	–0.4	—	—	–0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	mV
V_{ICM} (AC coupled)	Dedicated reference clock pin	1000/900/850 (139)			1000/900/850 (139)			mV
	RX reference clock pin	1.0/0.9/0.85 (140)			1.0/0.9/0.85(140)			mV
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	mV

(138) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
(139) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.
(140) This supply follows VCCR_GXB

Clock Network	ATX PLL			CMU PLL [161]			fPLL		
	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span
xN (PCIe)	—	8.0	8	—	5.0	8	—	—	—
xN (Native PHY IP)	8.0	8.0	Up to 13 channels above and below PLL	7.99	7.99	Up to 13 channels above and below PLL	3.125	3.125	Up to 13 channels above and below PLL
	—	8.01 to 9.8304	Up to 7 channels above and below PLL						

Standard PCS Data Rate

Table 2-30: Standard PCS Approximate Maximum Date Rate (Gbps) for Arria V GZ Devices

The maximum data rate is also constrained by the transceiver speed grade. Refer to the "Commercial and Industrial Speed Grade Offering for Arria V GZ Devices" table for the transceiver speed grade.

Mode [164]	Transceiver Speed Grade	PMA Width	20	20	16	16	10	10	8	8
		PCS/Core Width	40	20	32	16	20	10	16	8
FIFO	2	C3, I3L core speed grade	9.9	9	7.84	7.2	5.3	4.7	4.24	3.76
	3	C4, I4 core speed grade	8.8	8.2	7.2	6.56	4.8	4.3	3.84	3.44

[161] ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

[164] The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Typical VOD Settings

Table 2-32: Typical V_{OD} Setting for Arria V GZ Channel, TX Termination = 100 Ω

The tolerance is +/-20% for all VOD settings except for settings 2 and below.

Symbol	V_{OD} Setting	V_{OD} Value (mV)	V_{OD} Setting	V_{OD} Value (mV)
V_{OD} **differential peak to peak typical**	0 (166)	0	32	640
	1 (166)	20	33	660
	2 (166)	40	34	680
	3 (166)	60	35	700
	4 (166)	80	36	720
	5 (166)	100	37	740
	6	120	38	760
	7	140	39	780
	8	160	40	800
	9	180	41	820
	10	200	42	840
	11	220	43	860
	12	240	44	880
	13	260	45	900
	14	280	46	920

(166) If TX termination resistance = 100 Ω,this VOD setting is illegal.

Symbol	V_{OD} Setting	V_{OD} Value (mV)	V_{OD} Setting	V_{OD} Value (mV)
V_{OD} **differential peak to peak typical**	15	300	47	940
	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
$t_{x\ Jitter}$ - True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	UI
$t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	300	—	—	325	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.2	—	—	0.25	UI
t_{DUTY}	Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	%
t_{RISE} & t_{FALL}	True Differential I/O Standards	—	—	200	—	—	200	ps
	Emulated Differential I/O Standards with three external output resistor networks	—	—	250	—	—	300	ps
TCCS	True Differential I/O Standards	—	—	150	—	—	150	ps
	Emulated Differential I/O Standards	—	—	300	—	—	300	ps

Receiver High-Speed I/O Specifications

Table 2-41: Receiver High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

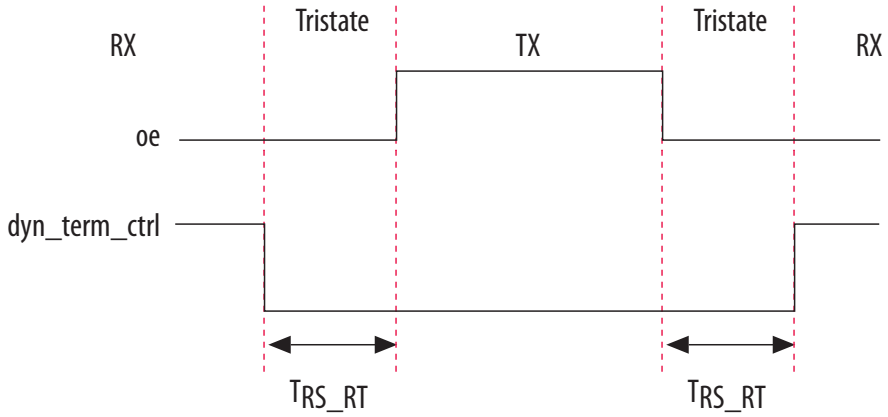
When J = 1 or 2, bypass the SERDES block.

OCT Calibration Block Specifications

Table 2-51: OCT Calibration Block Specifications for Arria V GZ Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT R_S/R_T calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between OCT R_S and R_T (See the figure below.)	—	2.5	—	ns

Figure 2-6: Timing Diagram for `oe` and `dyn_term_ctrl` Signals



Related Information

Configuration, Design Security, and Remote System Upgrades in Arria V Devices

Initialization

Table 2-61: Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices

Initialization Clock Source	Configuration Schemes	Maximum Frequency (MHz)	Minimum Number of Clock Cycles
Internal Oscillator	AS, PS, FPP	12.5	8576
CLKUSR (222)	PS, FPP	125	
	AS	100	
DCLK	PS, FPP	125	

Configuration Files

Use the following table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (`.hex`) or tabular text file (`.ttf`) format, have different file sizes.

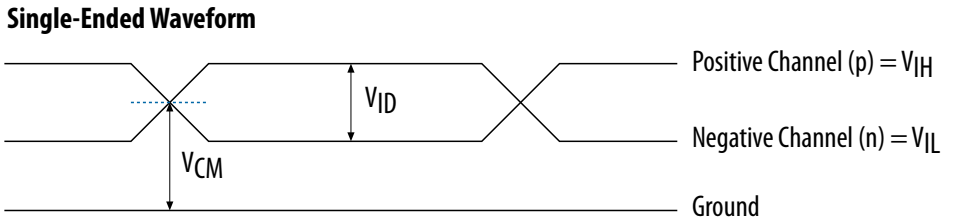
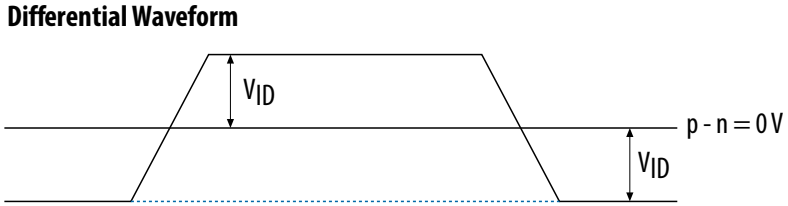
For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size.

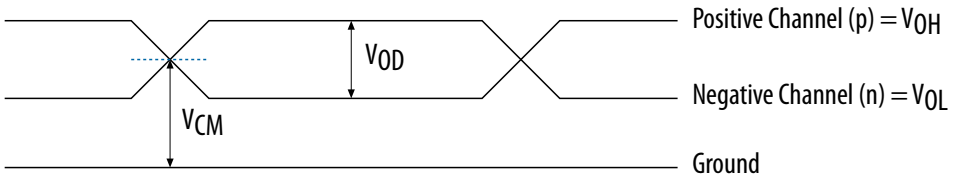
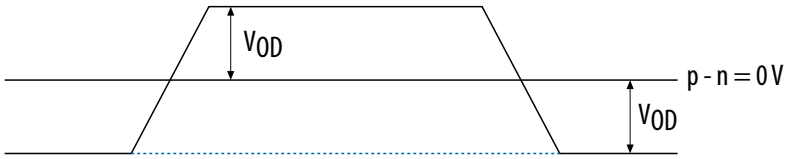
(221) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

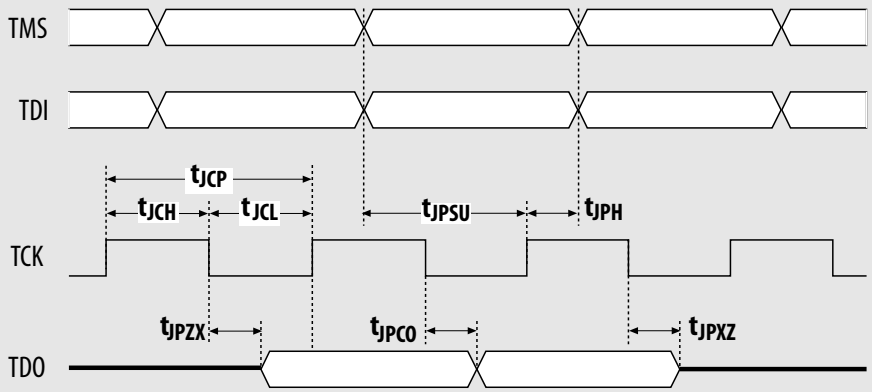
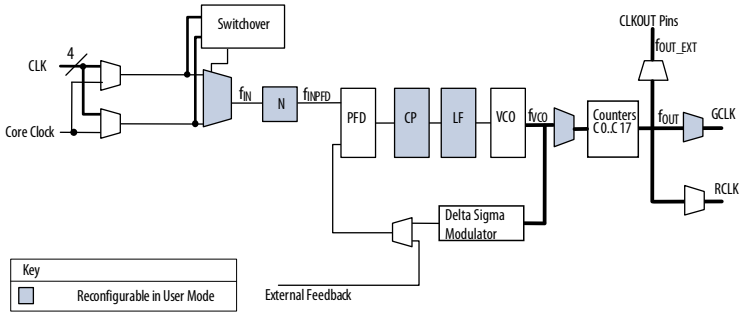
(222) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** panel of the **Device and Pin Options** dialog box.

Glossary

Table 2-68: Glossary

Term	Definition
Differential I/O Standards	Receiver Input Waveforms   Transmitter Output Waveforms

Term	Definition
	Single-Ended Waveform  **Differential Waveform** 
f_{HSCLK}	Left and right PLL input clock frequency.
f_{HSDR}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	High-speed I/O block—Maximum and minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
J	High-speed I/O block—Deserialization factor (width of parallel data bus).

Term	Definition
JTAG Timing Specifications	JTAG Timing Specifications: 
PLL Specifications	Diagram of PLL Specifications  Note: 1. Core Clock can only be fed by dedicated clock input pins or PLL outputs.

Term	Definition
V_{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
V_{SWING}	Differential input voltage
V_X	Input differential cross point voltage
V_{OX}	Output differential cross point voltage
W	High-speed I/O block—clock boost factor

Document Revision History

Date	Version	Changes
February 2017	2017.02.10	• Changed the minimum value for t_{CD2UMC} in the “FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1” table. • Changed the minimum value for t_{CD2UMC} in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1" table. • Changed the minimum value for t_{CD2UMC} in the "AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices" table. • Changed the minimum value for t_{CD2UMC} in the "PS Timing Parameters for Arria V GZ Devices" table. • Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices" table.