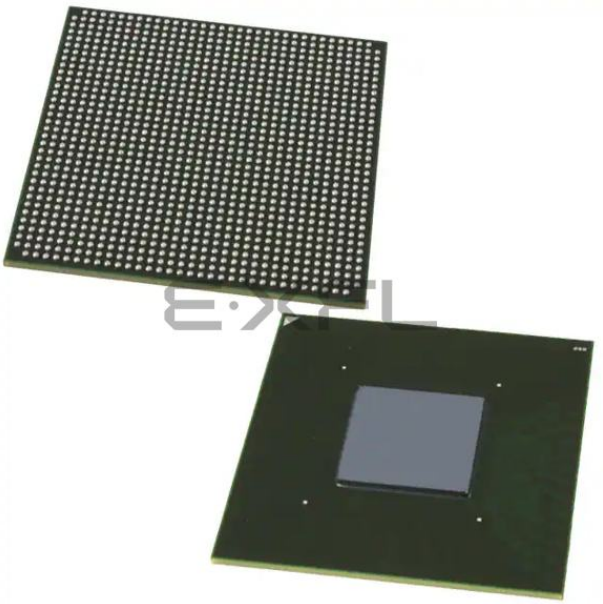


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	23780
Number of Logic Elements/Cells	504000
Total RAM Bits	27695104
Number of I/O	544
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxbb7d4f35i5n

Symbol	Description	Condition	Minimum[7]	Typical	Maximum[7]	Unit
V_{CCPD_HPS} [8]	HPS I/O pre-driver power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
V_{CCIO_HPS}	HPS I/O buffers power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V [9]	1.283	1.35	1.418	V
		1.2 V	1.14	1.2	1.26	V
$V_{CCRSTCLK\_HPS}$	HPS reset and clock input pins power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
V_{CCPLL_HPS}	HPS PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V

(7) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(8) V_{CCPD_HPS} must be 2.5 V when V_{CCIO_HPS} is 2.5, 1.8, 1.5, or 1.2 V. V_{CCPD_HPS} must be 3.0 V when V_{CCIO_HPS} is 3.0 V. V_{CCPD_HPS} must be 3.3 V when V_{CCIO_HPS} is 3.3 V.

(9) V_{CCIO_HPS} 1.35 V is supported for HPS row I/O bank only.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)[16]			$V_{ICM(DC)}$ (V)			V_{OD} (V)[17]			V_{OCM} (V)[17][18]		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Transceiver Specifications for Arria V GX and SX Devices and Transceiver Specifications for Arria V GT and ST Devices tables.														
2.5 V LVDS[19]	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	$D_{MAX} \leq$ 1.25 Gbps	1.80	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	$D_{MAX} >$ 1.25 Gbps	1.55						
RSDS (HIO)[20]	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.25	—	1.45	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO)[21]	2.375	2.5	2.625	200	—	600	0.300	—	1.425	0.25	—	0.6	1	1.2	1.4
LVPECL[22]	—	—	—	300	—	—	0.60	$D_{MAX} \leq$ 700 Mbps	1.80	—	—	—	—	—	—
							1.00	$D_{MAX} >$ 700 Mbps	1.60						

Related Information

- **Transceiver Specifications for Arria V GX and SX Devices** on page 1-23
  Provides the specifications for transmitter, receiver, and reference clock I/O pin.

(16) The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.
(17) R_L range: $90 \leq R_L \leq 110\ \Omega$.
(18) This applies to default pre-emphasis setting only.
(19) For optimized LVDS receiver performance, the receiver voltage input range must be within 1.0 V to 1.6 V for data rates above 1.25 Gbps and 0 V to 1.85 V for data rates below 1.25 Gbps.
(20) For optimized RSDS receiver performance, the receiver voltage input range must be within 0.25 V to 1.45 V.
(21) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be within 0.3 V to 1.425 V.
(22) For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rates above 700 Mbps and 0.45 V to 1.95 V for data rates below 700 Mbps.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Transmitter REFCLK phase noise(43)	10 Hz	—	—	–50	dBc/Hz
	100 Hz	—	—	–80	dBc/Hz
	1 KHz	—	—	–110	dBc/Hz
	10 KHz	—	—	–120	dBc/Hz
	100 KHz	—	—	–120	dBc/Hz
	≥ 1 MHz	—	—	–130	dBc/Hz
R_{REF}	—	—	2000 ±1%	—	Ω

Table 1-27: Transceiver Clocks Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
fixedclk clock frequency	PCIe Receiver Detect	—	125	—	MHz
Transceiver Reconfiguration Controller IP (mgmt_clk_clk) clock frequency	—	75	—	125	MHz

Table 1-28: Receiver Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS				
Data rate (6-Gbps transceiver)(44)	—	611	—	6553.6	Mbps

(43) The transmitter REFCLK phase jitter is 30 ps p-p (5 ps RMS) with bit error rate (BER) 10^{-12}, equivalent to 14 sigma.
(44) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

High-Speed I/O Specifications

Table 1-40: High-Speed I/O Specifications for Arria V Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block. When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

The Arria V devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 360 Mbps
- True mini-LVDS output standard with data rates of up to 400 Mbps

Symbol		Condition	–I3, –C4			–I5, –C5			–C6			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards		Clock boost factor W = 1 to 40[72]	5	—	800	5	—	750	5	—	625	MHz
f_{HSCLK_in} (input clock frequency) Single-Ended I/O Standards[73]		Clock boost factor W = 1 to 40[72]	5	—	625	5	—	625	5	—	500	MHz
f_{HSCLK_in} (input clock frequency) Single-Ended I/O Standards[74]		Clock boost factor W = 1 to 40[72]	5	—	420	5	—	420	5	—	420	MHz
f_{HSCLK_OUT} (output clock frequency)		—	5	—	625[75]	5	—	625[75]	5	—	500[75]	MHz
Transmitter	True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J =3 to 10[76]	[77]	—	1250	[77]	—	1250	[77]	—	1050	Mbps

[72] Clock boost factor (W) is the ratio between the input data rate and the input clock rate.
[73] This applies to DPA and soft-CDR modes only.
[74] This applies to non-DPA mode only.
[75] This is achieved by using the LVDS clock network.
[76] The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.
[77] The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

Symbol	Condition	–I3, –C4			–I5, –C5			–C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	SERDES factor J ≥ 8[76][78], LVDS TX with RX DPA	[77]	—	1600	[77]	—	1500	[77]	—	1250	Mbps
	SERDES factor J = 1 to 2, Uses DDR Registers	[77]	—	[79]	[77]	—	[79]	[77]	—	[79]	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Network - f_{HSDR} (data rate)[80]	SERDES factor J = 4 to 10[81]	[77]	—	945	[77]	—	945	[77]	—	945	Mbps
Emulated Differential I/O Standards with One External Output Resistor Network - f_{HSDR} (data rate)[80]	SERDES factor J = 4 to 10[81]	[77]	—	200	[77]	—	200	[77]	—	200	Mbps
$t_{x\ Jitter}$ -True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps – 1.25 Gbps	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	UI

(78) The V_{CC} and V_{CCP} must be on a separate power layer and a maximum load of 5 pF for chip-to-chip interface.
(79) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}), provided you can close the design timing and the signal integrity simulation is clean.
(80) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.
(81) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications

Figure 1-5: LVDS Soft-Clock Data Recovery (CDR)/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Equal to 1.25 Gbps

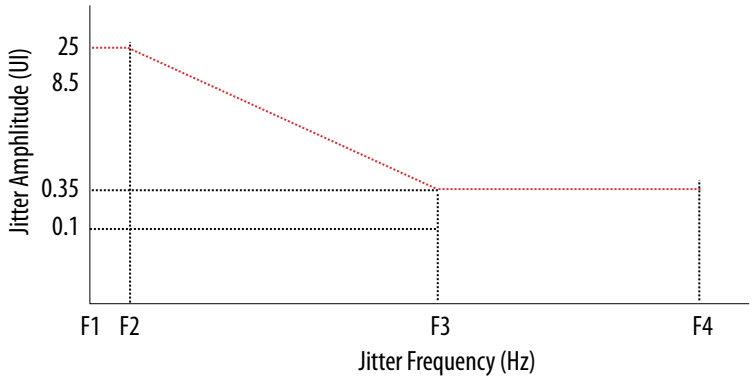
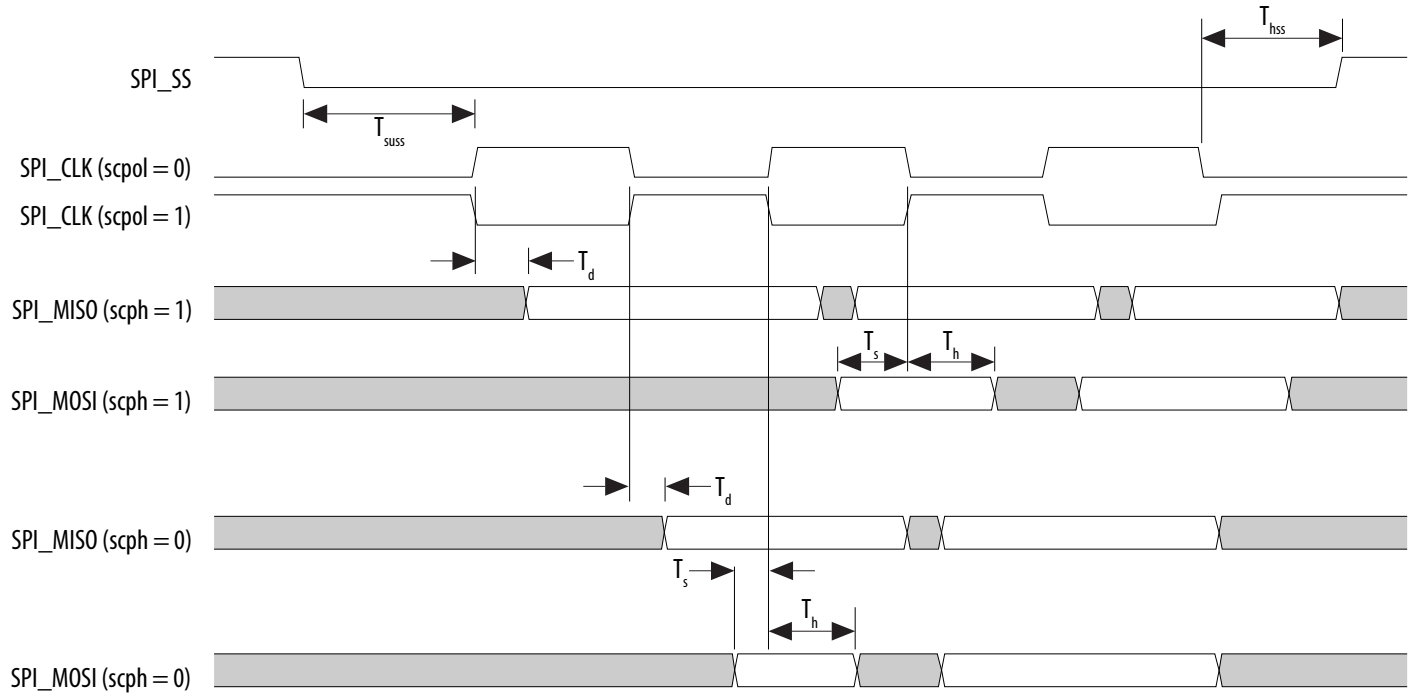


Table 1-42: LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.25 Gbps

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Figure 1-10: SPI Slave Timing Diagram



Related Information

SPI Controller, Arria V Hard Processor System Technical Reference Manual
Provides more information about rx_sample_delay.

SD/MMC Timing Characteristics

Table 1-54: Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices

After power up or cold reset, the Boot ROM uses `drvsel` = 3 and `smplsel` = 0 to execute the code. At the same time, the SD/MMC controller enters the Identification Phase followed by the Data Phase. During this time, the value of interface output clock `SDMMC_CLK_OUT` changes from a maximum of 400 kHz (Identification Phase) up to a maximum of 12.5 MHz (Data Phase), depending on the internal reference clock `SDMMC_CLK` and the `CSEL` setting. The value of `SDMMC_CLK` is based on the external oscillator frequency and has a maximum value of 50 MHz.

Table 1-57: RGMII RX Timing Requirements for Arria V Devices

Symbol	Description	Min	Typ	Unit
T_{clk} (1000Base-T)	RX_CLK clock period	—	8	ns
T_{clk} (100Base-T)	RX_CLK clock period	—	40	ns
T_{clk} (10Base-T)	RX_CLK clock period	—	400	ns
T_{su}	RX_D/RX_CTL setup time	1	—	ns
T_h	RX_D/RX_CTL hold time	1	—	ns

Figure 1-14: RGMII RX Timing Diagram

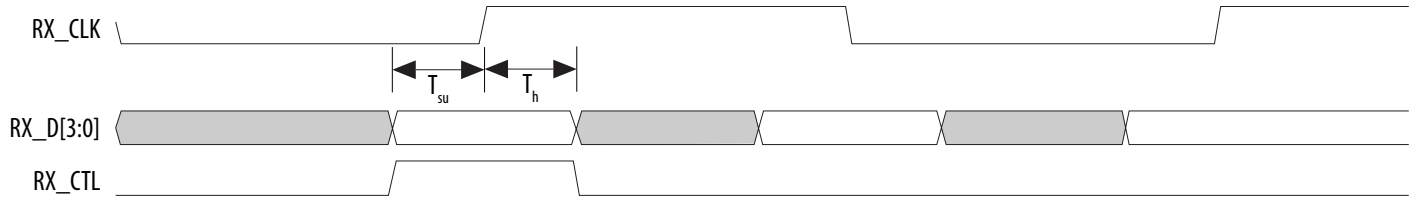
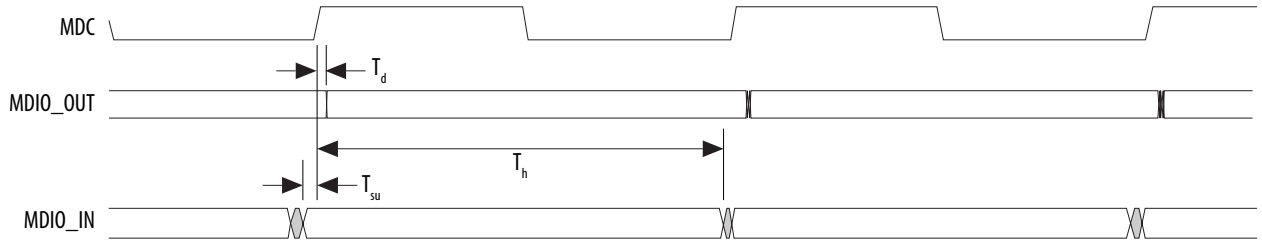


Table 1-58: Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	MDC clock period	—	400	—	ns
T_d	MDC to MDIO output data delay	10	—	20	ns
T_s	Setup time for MDIO data	10	—	—	ns
T_h	Hold time for MDIO data	0	—	—	ns

Figure 1-15: MDIO Timing Diagram



I²C Timing Characteristics

Table 1-59: I²C Timing Requirements for Arria V Devices

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T_{clk}	Serial clock (SCL) clock period	10	—	2.5	—	µs
$T_{clkhigh}$	SCL high time	4.7	—	0.6	—	µs
T_{clklow}	SCL low time	4	—	1.3	—	µs
T_s	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1	—	µs
T_h	Hold time for SCL to SDA data	0	3.45	0	0.9	µs
T_d	SCL to SDA output data delay	—	0.2	—	0.2	µs
T_{su_start}	Setup time for a repeated start condition	4.7	—	0.6	—	µs
T_{hd_start}	Hold time for a repeated start condition	4	—	0.6	—	µs
T_{su_stop}	Setup time for a stop condition	4	—	0.6	—	µs

HPS JTAG Timing Specifications

Table 1-62: HPS JTAG Timing Parameters and Values for Arria V Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	12(90)	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14(90)	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14(90)	ns

Configuration Specifications

This section provides configuration specifications and timing for Arria V devices.

POR Specifications

Table 1-63: Fast and Standard POR Delay Specification for Arria V Devices

POR Delay	Minimum	Maximum	Unit
Fast	4	12(91)	ms

(90) A 1-ns adder is required for each $V_{CCIO\ \_HPS}$ voltage step down from 3.0 V. For example, t_{JPCO}= 13 ns if $V_{CCIO\ \_HPS}$ of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

(91) The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

Term	Definition
V_{OX}	Output differential cross point voltage
W	High-speed I/O block—Clock boost factor

Document Revision History

Date	Version	Changes

December 2016	2016.12.09	• Updated V_{ICM} (AC coupled) specifications in Receiver Specifications for Arria V GX and SX Devices table.
		• Added maximum specification for T_d in Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices table.
		• Updated T_{init} specifications in the following tables:
		  • FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Arria V Devices
		  • FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices
		  • AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices
		  • PS Timing Parameters for Arria V Devices

June 2016	2016.06.10	• Changed pin capacitance to maximum values.
		• Updated SPI Master Timing Requirements for Arria V Devices table.
		  • Added T_{su} and T_h specifications.
		  • Removed T_{dinmax} specifications.
		• Updated SPI Master Timing Diagram.
		• Updated T_{clk} spec from maximum to minimum in I^2C Timing Requirements for Arria V Devices table.

Date	Version	Changes

June 2015	2015.06.16	• Added the supported data rates for the following output standards using true LVDS output buffer types in the High-Speed I/O Specifications for Arria V Devices table:
		  • True RSDS output standard: data rates of up to 360 Mbps
		  • True mini-LVDS output standard: data rates of up to 400 Mbps
		• Added note in the condition for Transmitter—Emulated Differential I/O Standards f_{HSDR} data rate parameter in the High-Speed I/O Specifications for Arria V Devices table. Note: When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.
		• Changed Queued Serial Peripheral Interface (QSPI) to Quad Serial Peripheral Interface (SPI) Flash.
		• Updated T_h location in I^2C Timing Diagram.
		• Updared T_{wp} location in NAND Address Latch Timing Diagram.
		• Corrected the unit for t_{DH} from ns to s in FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices table.
		• Updated the maximum value for t_{CO} from 4 ns to 2 ns in AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices table.
		• Moved the following timing diagrams to the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.
		  • FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is 1
		  • FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is >1
		  • AS Configuration Timing Waveform
		  • PS Configuration Timing Waveform

Symbol	Description	Condition	Minimum[114]	Typical	Maximum [114]	Unit
V_I	DC input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	–40	—	100	°C
t_{RAMP}	Power supply ramp time	Standard POR	200 µs	—	100 ms	—
		Fast POR	200 µs	—	4 ms	—

Recommended Transceiver Power Supply Operating Conditions

Table 2-6: Recommended Transceiver Power Supply Operating Conditions for Arria V GZ Devices

Symbol	Description	Minimum [118]	Typical	Maximum[118]	Unit
V_{CCA_GXBL} [119], [120]	Transceiver channel PLL power supply (left side)	2.85	3.0	3.15	V
		2.375	2.5	2.625	
V_{CCA_GXBR} [119], [120]	Transceiver channel PLL power supply (right side)	2.85	3.0	3.15	V
		2.375	2.5	2.625	
V_{CCHIP_L}	Transceiver hard IP power supply (left side)	0.82	0.85	0.88	V
V_{CCHSSI_L}	Transceiver PCS power supply (left side)	0.82	0.85	0.88	V
V_{CCHSSI_R}	Transceiver PCS power supply (right side)	0.82	0.85	0.88	V

(114) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(118) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(119) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

(120) When using ATX PLLs, the supply must be 3.0 V.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Rise time	Measure at ±60 mV of differential signal (138)	—	—	400	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal (138)	—	—	400	—	—	400	
Duty cycle	—	45	—	55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express ®(PCIe)	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5	—	—	0 to –0.5	—	%
On-chip termination resistors	—	—	100	—	—	100	—	Ω
Absolute V_{MAX}	Dedicated reference clock pin	—	—	1.6	—	—	1.6	V
	RX reference clock pin	—	—	1.2	—	—	1.2	
Absolute V_{MIN}	—	–0.4	—	—	–0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	mV
V_{ICM} (AC coupled)	Dedicated reference clock pin	1000/900/850 (139)			1000/900/850 (139)			mV
	RX reference clock pin	1.0/0.9/0.85 (140)			1.0/0.9/0.85(140)			mV
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	mV

(138) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
(139) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.
(140) This supply follows VCCR_GXB

CMU PLL

Table 2-26: CMU PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported data range	—	600	—	12500	600	—	10312.5	Mbps
$t_{pll\_powerdown}$ (153)	—	1	—	—	1	—	—	µs
t_{pll_lock} (154)	—		—	10	—	—	10	µs

Related Information

Arria V Device Overview

For more information about device ordering codes.

ATX PLL

Table 2-27: ATX PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

(153) $t_{pll\_powerdown}$ is the PLL powerdown minimum pulse width.

(154) t_{pll_lock} is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
$t_{x\ Jitter}$ - True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	UI
$t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	300	—	—	325	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.2	—	—	0.25	UI
t_{DUTY}	Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	%
t_{RISE} & t_{FALL}	True Differential I/O Standards	—	—	200	—	—	200	ps
	Emulated Differential I/O Standards with three external output resistor networks	—	—	250	—	—	300	ps
TCCS	True Differential I/O Standards	—	—	150	—	—	150	ps
	Emulated Differential I/O Standards	—	—	300	—	—	300	ps

Receiver High-Speed I/O Specifications

Table 2-41: Receiver High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions (201)	Maximum
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
	01010101	8	32	640 data transitions

Soft CDR Mode High-Speed I/O Specifications

Table 2-44: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Soft-CDR ppm tolerance	—	—	—	300	—	—	300	± ppm

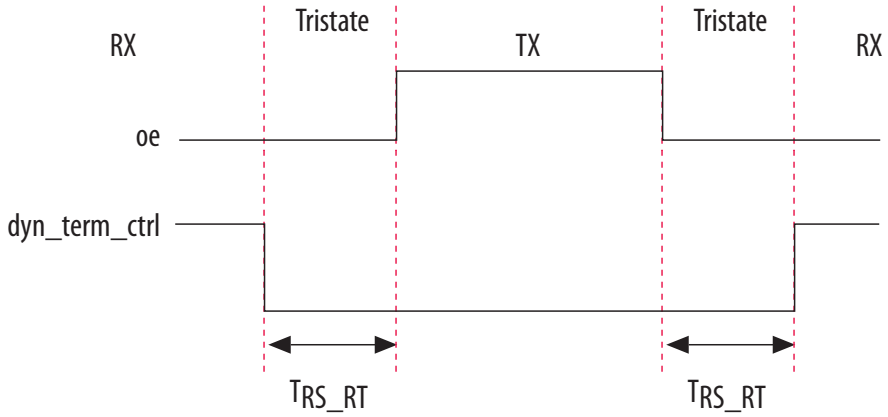
(201) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

OCT Calibration Block Specifications

Table 2-51: OCT Calibration Block Specifications for Arria V GZ Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT R_S/R_T calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between OCT R_S and R_T (See the figure below.)	—	2.5	—	ns

Figure 2-6: Timing Diagram for `oe` and `dyn_term_ctrl` Signals



Note: When you enable the decompression or design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8, FPP ×16, and FPP ×32. For the respective DCLK-to-DATA[] ratio, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.

Table 2-56: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1

Use these timing parameters when the decompression and design security features are disabled.

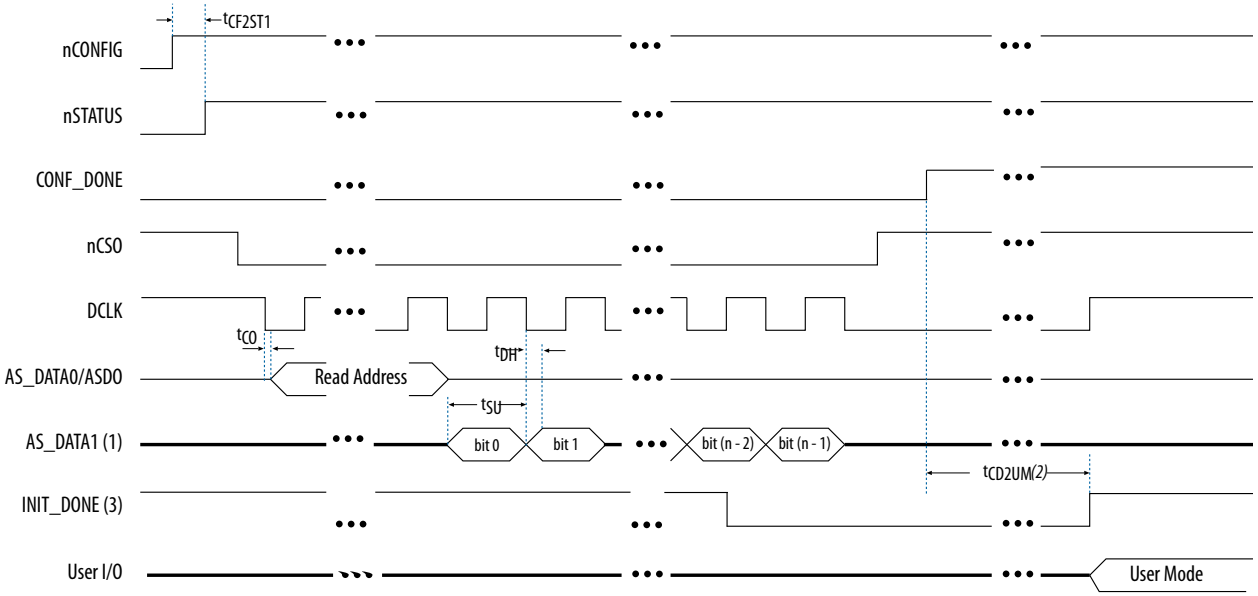
Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1,506 (205)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 (206)	µs
t_{CF2CK} (207)	nCONFIG high to first rising edge on DCLK	1,506	—	µs
t_{ST2CK} (207)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16)	—	125	MHz
	DCLK frequency (FPP ×32)	—	100	MHz
t_{CD2UM}	CONF_DONE high to user mode (208)	175	437	µs

(205) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(206) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.
(207) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Active Serial Configuration Timing

Figure 2-9: AS Configuration Timing

Timing waveform for the active serial (AS) x1 mode and AS x4 mode configuration timing.



Notes:
1. If you are using AS ×4 mode, this signal represents the AS_DATA[3..0] and EPCQ sends in 4-bits of data for each DCLK cycle.
2. The initialization clock can be from internal oscillator or CLKUSR pin.
3. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 2-58: AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices

The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in the "PS Timing Parameters for Arria V GZ Devices" table.