E·XFL

Intel - 5AGXBB7D4F40C4N Datasheet



Welcome to E-XFL.COM

Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

2014110	
Product Status	Obsolete
Number of LABs/CLBs	23780
Number of Logic Elements/Cells	504000
Total RAM Bits	27695104
Number of I/O	704
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxbb7d4f40c4n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Arria V GX, GT, SX, and ST Device Datasheet



This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Arria® V devices.

Arria V devices are offered in commercial and industrial grades. Commercial devices are offered in -C4 (fastest), -C5, and -C6 speed grades. Industrial grade devices are offered in the -I3 and -I5 speed grades.

Related Information

Arria V Device Overview

Provides more information about the densities and packages of devices in the Arria V family.

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Arria V devices.

Operating Conditions

Arria V devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Arria V devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Arria V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms.

The functional operation of the device is not implied for these conditions.

[©] 2017 Intel Corporation. All rights reserved. Intel, the Intel logo, Altera, Arria, Cyclone, Enpirion, MAX, NIOS, Quartus and Stratix words and logos are trademarks of Intel Corporation in the US and/or other countries. Other marks and brands may be claimed as the property of others. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.





AV-51002 2017.02.10

1-5

Symbol	Description	Condition	Minimum ⁽¹⁾	Typical	Maximum ⁽¹⁾	Unit
V	Coro voltago powor supply	-C4, -I5, -C5, -C6	1.07	1.1	1.13	V
V CC	Core voltage power suppry	-I3	1.12	1.15	1.18	V
V	Periphery circuitry, PCIe hard IP block,	-C4, -I5, -C5, -C6	1.07	1.1	1.13	V
V CCP	and transceiver PCS power supply	-I3	1.12	1.15	1.18	V
		3.3 V	3.135	3.3	3.465	V
V	Configuration pins power supply	3.0 V	2.85	3.0	3.15	V
V CCPGM		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
V _{CC_AUX}	Auxiliary supply	_	2.375	2.5	2.625	V
V _{CCBAT} ⁽²⁾	Battery back-up power supply	_	1.2	—	3.0	V
	(For design security volatile key register)					
		3.3 V	3.135	3.3	3.465	V
V _{CCPD} ⁽³⁾	I/O pre-driver power supply	3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V

⁽¹⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(2) If you do not use the design security feature in Arria V devices, connect V_{CCBAT} to a 1.5-V, 2.5-V, or 3.0-V power supply. Arria V power-on reset (POR) circuitry monitors V_{CCBAT}. Arria V devices do not exit POR if V_{CCBAT} is not powered up.



⁽³⁾ V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25, or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V. V_{CCPD} must be 3.3 V when V_{CCIO} is 3.3 V.

AV-51002 2017.02.10

Symbol	Description	Condition	Minimum ⁽⁷⁾	Typical	Maximum ⁽⁷⁾	Unit
	HPS I/O	3.3 V	3.135	3.3	3.465	V
V _{CCPD_HPS} ⁽⁸⁾	pre-driver	3.0 V	2.85	3.0	3.15	V
	supply	2.5 V	2.375	2.5	2.625	V
		3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
	HPS I/O	2.5 V	2.375	2.5	2.625	V
V _{CCIO_HPS}	buffers power	1.8 V	1.71	1.8	1.89	V
	supply	1.5 V	1.425	1.5	1.575	V
		1.35 V ⁽⁹⁾	1.283	1.35	1.418	V
		1.2 V	1.14	1.2	1.26	V
	HPS reset	3.3 V	3.135	3.3	3.465	V
V	and clock	3.0 V	2.85	3.0	3.15	V
V CCRSTCLK_HPS	power	2.5 V	2.375	2.5	2.625	V
	supply	1.8 V	1.71	1.8	1.89	V
V _{CCPLL_HPS}	HPS PLL analog voltage regulator power supply	_	2.375	2.5	2.625	V



⁽⁷⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁸⁾ V_{CCPD_HPS} must be 2.5 V when V_{CCIO_HPS} is 2.5, 1.8, 1.5, or 1.2 V. V_{CCPD_HPS} must be 3.0 V when V_{CCIO_HPS} is 3.0 V. V_{CCPD_HPS} must be 3.3 V when V_{CCIO_HPS} is 3.3 V.

 $^{^{(9)}\,}$ V_{CCIO_HPS} 1.35 V is supported for HPS row I/O bank only.

Table 1-21: Transceiver Clocks Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
Symbol/Description	Condition	Min	Тур	Max	Min	Тур	Max	
fixedclk clock frequency	PCIe Receiver Detect	_	125	_	_	125	_	MHz
Transceiver Reconfigura- tion Controller IP (mgmt_ clk_clk) clock frequency	_	75	_	125	75	_	125	MHz

Table 1-22: Receiver Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4		Transceiver Speed Grade 6			llnit	
Symbol/Description	Condition	Min	Тур	Max	Min	Тур	Max	Onit
Supported I/O standards		1	.5 V PCML,	2.5 V PCML,	LVPECL, an	d LVDS		
Data rate ⁽²⁸⁾		611	—	6553.6	611	—	3125	Mbps
Absolute V_{MAX} for a receiver pin ⁽²⁹⁾	_		_	1.2		—	1.2	V
Absolute V _{MIN} for a receiver pin	_	-0.4	_		-0.4	—	—	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) before device configuration	_	_		1.6		_	1.6	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) after device configuration	_	_	_	2.2		_	2.2	V



 ⁽²⁸⁾ To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.
 ⁽²⁹⁾ The device cannot tolerate prolonged operation at this absolute maximum.

CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain

Figure 1-2: Continuous Time-Linear Equalizer (CTLE) Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices



Arria V GX, GT, SX, and ST Device Datasheet

Altera Corporation



Typical TX V_{OD} Setting for Arria V Transceiver Channels with termination of 100 Ω

Table 1-32: Typical TX Vor	Setting for Arria V Tran	sceiver Channels with	termination of 100 Ω

Symbol	V _{OD} Setting ⁽⁵⁸⁾	V _{OD} Value (mV)	V _{OD} Setting ⁽⁵⁸⁾	V _{OD} Value (mV)
	6 ⁽⁵⁹⁾	120	34	680
	7 ⁽⁵⁹⁾	140	35	700
	8(59)	160	36	720
	9	180	37	740
	10	200	38	760
	11	220	39	780
	12	240	40	800
	13	260	41	820
	14	280	42	840
V _{OD} differential peak-to-peak typical	15	300	43	860
7 I	16	320	44	880
	17	340	45	900
	18	360	46	920
	19	380	47	940
	20	400	48	960
	21	420	49	980
	22	440	50	1000
	23	460	51	1020
	24	480	52	1040

⁽⁵⁸⁾ Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

⁽⁵⁹⁾ Only valid for data rates \leq 5 Gbps.



For example, when V_{OD} = 800 mV, the corresponding V_{OD} value setting is 40. The following conditions show that the 1st post tap pre-emphasis setting = 2 is valid:

- $|B| + |C| \le 60 \Rightarrow 40 + 2 = 42$ ٠
- $|B| |C| > 5 \rightarrow 40 2 = 38$
- $(V_{MAX}/V_{MIN} 1)\% < 600\% \Rightarrow (42/38 1)\% = 10.52\%$

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Arria V HSSI HSPICE models.

Table 1-33: Transmitter Pre-Emphasis Levels for Arria V Devices

Quartus Prime 1st	Quartus Prime V _{OD} Setting							
Post Tap Pre- Emphasis Setting	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	Unit
0	0	0	0	0	0	0	0	dB
1	1.97	0.88	0.43	0.32	0.24	0.19	0.13	dB
2	3.58	1.67	0.95	0.76	0.61	0.5	0.41	dB
3	5.35	2.48	1.49	1.2	1	0.83	0.69	dB
4	7.27	3.31	2	1.63	1.36	1.14	0.96	dB
5	_	4.19	2.55	2.1	1.76	1.49	1.26	dB
6	_	5.08	3.11	2.56	2.17	1.83	1.56	dB
7	_	5.99	3.71	3.06	2.58	2.18	1.87	dB
8	_	6.92	4.22	3.47	2.93	2.48	2.11	dB
9	_	7.92	4.86	4	3.38	2.87	2.46	dB
10	_	9.04	5.46	4.51	3.79	3.23	2.77	dB
11	_	10.2	6.09	5.01	4.23	3.61	_	dB
12	_	11.56	6.74	5.51	4.68	3.97	_	dB
13	_	12.9	7.44	6.1	5.12	4.36	_	dB
14	_	14.44	8.12	6.64	5.57	4.76	_	dB
15	_	_	8.87	7.21	6.06	5.14	_	dB

Arria V GX, GT, SX, and ST Device Datasheet

Altera Corporation



Table 1-34: Transceiver Compliance Specification for All Supported Protocol for Arria V GX, GT, SX, and ST Devices

Protocol	Sub-protocol	Data Rate (Mbps)
	PCIe Gen1	2,500
PCIe	PCIe Gen2	5,000
	PCIe Cable	2,500
XAUI	XAUI 2135	3,125
	SRIO 1250 SR	1,250
	SRIO 1250 LR	1,250
	SRIO 2500 SR	2,500
	SRIO 2500 LR	2,500
	SRIO 3125 SR	3,125
Serial BanidIO [®] (SBIO)	SRIO 3125 LR	3,125
Serial Rapidio (SRIO)	SRIO 5000 SR	5,000
	SRIO 5000 MR	5,000
	SRIO 5000 LR	5,000
	SRIO_6250_SR	6,250
	SRIO_6250_MR	6,250
	SRIO_6250_LR	6,250



Symbol	Parameter	Condition	Min	Тур	Мах	Unit
t a	Period jitter for dedicated clock output	$F_{OUT} \ge 100 \text{ MHz}$			175	ps (p-p)
CASC_OUTPJ_DC	in cascaded PLLs	F _{OUT} < 100 MHz			17.5	mUI (p-p)
t _{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 μs	_			±10	%
dK _{BIT}	Bit number of Delta Sigma Modulator (DSM)	_	8	24	32	bits
k _{VALUE}	Numerator of fraction	_	128	8388608	2147483648	_
f _{RES}	Resolution of VCO frequency	$f_{INPFD} = 100 \text{ MHz}$	390625	5.96	0.023	Hz

Related Information

Memory Output Clock Jitter Specifications on page 1-57

Provides more information about the external memory interface clock output jitter specifications.

- Upstream PLL: 0.59 MHz ≤ Upstream PLL BW < 1 MHz
- Downstream PLL: Downstream PLL BW > 2 MHz



⁽⁷¹⁾ The cascaded PLL specification is only applicable with the following conditions:

Figure 1-7: Timing Diagram for oe and dyn_term_ctrl Signals



Duty Cycle Distortion (DCD) Specifications

Table 1-47: Worst-Case DCD on Arria V I/O Pins

The output DCD cycle only applies to the I/O buffer. It does not cover the system DCD.

Symbol	-I3,	-C4	–C5, –I5		-C6		Unit	
Зутрої	Min	Max	Min	Max	Min	Max	Unit	
Output Duty Cycle	45	55	45	55	45	55	%	

HPS Specifications

This section provides HPS specifications and timing for Arria V devices.

For HPS reset, the minimum reset pulse widths for the HPS cold and warm reset signals (HPS_nRST and HPS_nPOR) are six clock cycles of HPS_CLK1.



Table 1-57: RGMII RX Timing Requirements for Arria V Devices

Symbol	Description	Min	Тур	Unit
T _{clk} (1000Base-T)	RX_CLK clock period		8	ns
T _{clk} (100Base-T)	RX_CLK clock period		40	ns
T _{clk} (10Base-T)	RX_CLK clock period		400	ns
T _{su}	RX_D/RX_CTL setup time	1		ns
T _h	RX_D/RX_CTL hold time	1		ns

Figure 1-14: RGMII RX Timing Diagram



Table 1-58: Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices

Symbol	Description	Min	Тур	Мах	Unit
T _{clk}	MDC clock period	—	400	_	ns
T _d	MDC to MDIO output data delay	10		20	ns
T _s	Setup time for MDIO data	10	_		ns
T _h	Hold time for MDIO data	0			ns



1-82 PS Configuration Timing

Symbol	Parameter	Minimum	Maximum	Unit
$t_{CF2CK}^{(105)}$	nCONFIG high to first rising edge on DCLK	1506	—	μs
t _{ST2CK} ⁽¹⁰⁵⁾	nSTATUS high to first rising edge of DCLK	2		μs
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5		ns
t _{DH}	DATA[] hold time after rising edge on DCLK	0	_	ns
t _{CH}	DCLK high time	$0.45 imes 1/f_{ m MAX}$		S
t _{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$		S
t _{CLK}	DCLK period	1/f _{MAX}	—	S
f _{MAX}	DCLK frequency	_	125	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽¹⁰⁶⁾	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$		_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} × CLKUSR period)	_	_
T _{init}	Number of clock cycles required for device initialization	8,576		Cycles

Related Information

PS Configuration Timing

Provides the PS configuration timing waveform.



 $^{^{(105)}}$ If <code>nstatus</code> is monitored, follow the t_{ST2CK} specification. If <code>nstatus</code> is not monitored, follow the t_{CF2CK} specification.

⁽¹⁰⁶⁾ The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

1-96 Document Revision History

Date	Version	Changes
June 2015	2015.06.16	• Added the supported data rates for the following output standards using true LVDS output buffer types in the High-Speed I/O Specifications for Arria V Devices table:
		True RSDS output standard: data rates of up to 360 Mbps
		True mini-LVDS output standard: data rates of up to 400 Mbps
		• Added note in the condition for Transmitter—Emulated Differential I/O Standards f _{HSDR} data rate parameter in the High-Speed I/O Specifications for Arria V Devices table. Note: When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.
		Changed Queued Serial Peripheral Interface (QSPI) to Quad Serial Peripheral Interface (SPI) Flash.
		• Updated T _h location in I ² C Timing Diagram.
		 Updared T_{wp} location in NAND Address Latch Timing Diagram.
		 Corrected the unit for t_{DH} from ns to s in FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices table.
		• Updated the maximum value for t_{CO} from 4 ns to 2 ns in AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices table.
		• Moved the following timing diagrams to the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.
		FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is 1
		 FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is >1
		AS Configuration Timing Waveform
		PS Configuration Timing Waveform



Date	Version	Changes
June 2012	2.0	 Updated for the Quartus II software v12.0 release: Restructured document. Updated "Supply Current and Power Consumption" section. Updated Table 20, Table 21, Table 24, Table 25, Table 26, Table 35, Table 39, Table 43, and Table 52. Added Table 22, Table 23, and Table 33. Added Figure 1–1 and Figure 1–2. Added "Initialization" and "Configuration Files" sections.
February 2012	1.3	 Updated Table 2–1. Updated Transceiver-FPGA Fabric Interface rows in Table 2–20. Updated V_{CCP} description.
December 2011	1.2	Updated Table 2–1 and Table 2–3.
November 2011	1.1	 Updated Table 2–1, Table 2–19, Table 2–26, and Table 2–36. Added Table 2–5. Added Figure 2–4.
August 2011	1.0	Initial release.



Sumbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
Symbol/Description	Conditions	Min	Тур	Мах	Min	Тур	Max	Onit
	$V_{CCR_GXB} = 0.85 V$ full bandwidth	—	600		_	600	_	mV
Varia (AC and DC coupled)	$V_{CCR_GXB} = 0.85 V$ half bandwidth	—	600		_	600	_	mV
V _{ICM} (AC and DC coupled)	$V_{CCR_{GXB}} = 1.0 V$ full bandwidth	—	700		—	700	_	mV
	$V_{CCR_{GXB}} = 1.0 V$ half bandwidth	—	700		_	700	_	mV
t _{LTR} ⁽¹⁴⁹⁾	—		—	10	—	—	10	μs
t _{LTD} ⁽¹⁵⁰⁾	—	4	—		4	_	_	μs
t _{LTD_manual} ⁽¹⁵¹⁾	—	4	—	_	4	—	—	μs
t _{LTR_LTD_manual} ⁽¹⁵²⁾	_	15	—		15	—	_	μs
Programmable equalization (AC Gain)	Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz)		_	16			16	dB

2-26

Receiver



 $^{^{(149)}}$ t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

 $^{^{(150)}}$ t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.

⁽¹⁵¹⁾ t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.

 $t_{\text{LTR_LTD_manual}}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.

Typical VOD Settings

The tolerance is +/-20% for all VOD settings except for settings 2 and below.							
Symbol	V _{OD} Setting	V _{OD} Value (mV)	V _{OD} Setting	V _{OD} Value (mV)			
	0 (166)	0	32	640			
	1(166)	20	33	660			
	2(166)	40	34	680			
	3(166)	60	35	700			
	4 ⁽¹⁶⁶⁾	80	36	720			
	5 ⁽¹⁶⁶⁾	100	37	740			
	6	120	38	760			
V_{OD} differential peak to peak typical	7	140	39	780			
	8	160	40	800			
	9	180	41	820			
	10	200	42	840			
	11	220	43	860			
	12	240	44	880			
	13	260	45	900			
	14	280	46	920			

⁽¹⁶⁶⁾ If TX termination resistance = 100 Ω , this VOD setting is illegal.





2-42 Memory Block Specifications

Modo	Performar	nce	Unit		
Mode	C3, I3L	C4	14	Onit	
One sum of two 27×27	380	300	MHz		
One sum of two 36×18	380	300		MHz	
One complex 18×18	400	350		MHz	
One 36 × 36	380	30	MHz		
Modes using Three DSP Blocks					
One complex 18×25	340	275	265	MHz	
Modes using Four DSP Blocks					
One complex 27×27	350	310		MHz	

Memory Block Specifications

Table 2-36: Memory Block Performance Specifications for Arria V GZ Devices

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.

Momony	Mode	Resour	ces Used	Performance				Linit
memory	Mode	ALUTs	Memory	C3	C4	I3L	14	
MLAB	Single port, all supported widths	0	1	400	315	400	315	MHz
	Simple dual-port, x32/x64 depth	0	1	400	315	400	315	MHz
	Simple dual-port, x16 depth (178)	0	1	533	400	533	400	MHz
	ROM, all supported widths	0	1	500	450	500	450	MHz

⁽¹⁷⁸⁾ The F_{MAX} specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.



FPP Configuration Timing when DCLK to DATA[] > 1

Figure 2-8: FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1,

t_{CF2ST1} tcfg ;↔ nCONFIG ŤĊF2CK nSTATUS (3) 🕳 tstatus tCF2ST0 CONF_DONE (4) TCL tCH tsT2CK ŤĊF2CD (8) DCLK (6) (7) 1 2 ••• r 2 ••• r 1 \mathbf{D} (5) tCLK DATA[31..0] (8) Word 0 Word User Mode Word 3 • • • Word (n-1) tDH tDH tpsy High-Z User I/O User Mode INIT DONE (9) tCD2UM

Timing when using a MAX II device, MAX V device, or microprocessor as an external host.

Notes:

- 1. To find out the DCLK-to-DATA[] ratio for your system, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
- 2. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- 3. After power-up, the Arria V GZ device holds nSTATUS low for the time as specified by the POR delay.
- 4. After power-up, before and during configuration, CONF_DONE is low.
- 5. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- 6. "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
- 7. If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31.0] pins prior to sending the first DCLK rising edge.
- 8. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- 9. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.





Active Serial Configuration Timing

Figure 2-9: AS Configuration Timing



Timing waveform for the active serial (AS) x1 mode and AS x4 mode configuration timing.

Notes:

1. If you are using AS ×4 mode, this signal represents the AS_DATA[3..0] and ERCQ sends in 4-bits of data for each DCLKcycle.

2. The initialization clock can be from internal oscillator or CLKUSR pin

3. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE ges low.

Table 2-58: AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices

The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in the "PS Timing Parameters for Arria V GZ Devices" table.



Symbol	Parameter	Minimum	Maximum	Unit
t _{CO}	DCLK falling edge to AS_DATA0/ASDO output	_	4	ns
t _{SU}	Data setup time before falling edge on DCLK	1.5		ns
t _H	Data hold time after falling edge on DCLK	0	—	ns
t _{CD2UM}	CONF_DONE high to user mode ⁽²¹⁶⁾	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK}$ period	—	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (8576 × clkusr period)	_	_

Table 2-59: DCLK Frequency Specification in the AS Configuration Scheme

This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

The AS multi-device configuration scheme does not support ${\tt DCLK}$ frequency of 100 MHz.

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

Related Information

- Passive Serial Configuration Timing on page 2-67
- Configuration, Design Security, and Remote System Upgrades in Arria V Devices





⁽²¹⁶⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.