Intel - 5AGXFA5H4F35C4N Datasheet





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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	8962
Number of Logic Elements/Cells	190000
Total RAM Bits	13284352
Number of I/O	544
Number of Gates	
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxfa5h4f35c4n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Symbol	Description	Minimum	Maximum	Unit
V _{CCPLL_HPS}	HPS PLL analog power supply	-0.50	3.25	V
V _{CC_AUX_SHARED}	HPS auxiliary power supply	-0.50	3.25	V
I _{OUT}	DC output current per pin	-25	40	mA
T _J	Operating junction temperature	-55	125	°C
T _{STG}	Storage temperature (no bias)	-65	150	°C

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 4.00 V can only be at 4.00 V for ~15% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 1.5 years.

Table 1-2: Maximum Allowed Overshoot During Transitions for Arria V Devices

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

1-3



1-4 Recommended Operating Conditions

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
		3.8	100	%
		3.85	68	%
		3.9	45	%
		3.95	28	%
		4	15	%
		4.05	13	%
		4.1	11	%
		4.15	9	%
Vi (AC)	AC input voltage	4.2	8	%
		4.25	7	%
		4.3	5.4	%
		4.35	3.2	%
		4.4	1.9	%
		4.45	1.1	%
		4.5	0.6	%
		4.55	0.4	%
		4.6	0.2	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Arria V devices.

Recommended Operating Conditions

Table 1-3: Recommended Operating Conditions for Arria V Devices

This table lists the steady-state voltage values expected from Arria V devices. Power supply ramps must all be strictly monotonic, without plateaus.



Symbol/Description	Condition	Tran	sceiver Speed Gra	Unit	
Symbol/Description	Condition	Min	Тур	Max	Ont
	85- Ω setting	—	85	—	Ω
Differential on-chip termination	100- Ω setting	—	100	—	Ω
resistors	120-Ω setting	—	120	—	Ω
	150-Ω setting		150	_	Ω
Intra-differential pair skew	TX V_{CM} = 0.65 V (AC coupled) and slew rate of 15 ps			15	ps
Intra-transceiver block transmitter channel-to-channel skew	×6 PMA bonded mode			180	ps
Inter-transceiver block transmitter channel-to-channel skew ⁽⁵⁵⁾	× <i>N</i> PMA bonded mode			500	ps

Table 1-30: CMU PLL Specifications for Arria V GT and ST Devices

Symbol/Description	Transceiver S	peed Grade 3	Unit
Symbol Description	Min	Max	onit
Supported data range	0.611	10.3125	Gbps
fPLL supported data range	611	3125	Mbps

⁽⁵⁵⁾ This specification is only applicable to channels on one side of the device across two transceiver banks.



Symbol	Parameter	Condition	Min	Тур	Мах	Unit
t a	Period jitter for dedicated clock output	$F_{OUT} \ge 100 \text{ MHz}$			175	ps (p-p)
CASC_OUTPJ_DC	in cascaded PLLs	F _{OUT} < 100 MHz			17.5	mUI (p-p)
t _{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 μs	_			±10	%
dK _{BIT}	Bit number of Delta Sigma Modulator (DSM)	_	8	24	32	bits
k _{VALUE}	Numerator of fraction	_	128	8388608	2147483648	_
f _{RES}	Resolution of VCO frequency	$f_{INPFD} = 100 \text{ MHz}$	390625	5.96	0.023	Hz

Memory Output Clock Jitter Specifications on page 1-57

Provides more information about the external memory interface clock output jitter specifications.

- Upstream PLL: 0.59 MHz ≤ Upstream PLL BW < 1 MHz
- Downstream PLL: Downstream PLL BW > 2 MHz



⁽⁷¹⁾ The cascaded PLL specification is only applicable with the following conditions:

Cumbal	Condition		-I3, -C4			-I5, -C5			-C6		11
Symbol	Condition	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
t _{x Jitter} -Emulated Differential I/O Standards with Three	Total Jitter for Data Rate 600 Mbps – 1.25 Gbps	_		260	_	_	300	_		350	ps
External Output Resistor Network	Total Jitter for Data Rate < 600 Mbps	—		0.16	_	_	0.18	_		0.21	UI
t _{x Jitter} -Emulated Differential I/O Standards with One External Output Resistor Network	_			0.15		_	0.15			0.15	UI
t _{DUTY}	TX output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	%
	True Differential I/O Standards ⁽⁸²⁾			160	_	_	180			200	ps
t _{RISE} and t _{FALL}	Emulated Differential I/O Standards with Three External Output Resistor Network		_	250		_	250		_	300	ps
	Emulated Differential I/O Standards with One External Output Resistor Network	_		500	_		500	_		500	ps



 $^{^{(82)}\,}$ This applies to default pre-emphasis and V_{OD} settings only.

HPS PLL Input Jitter

Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate. The divide value (N) is the value programmed into the denominator field of the VCO register for each PLL. The PLL input reference clock is divided by this value. The range of the denominator is 1 to 64.

Maximum input jitter = Input clock period × Divide value (N) × 0.02

Table 1-50: Examples of Maximum Input Jitter

Input Reference Clock Period	Divide Value (N)	Maximum Jitter	Unit
40 ns	1	0.8	ns
40 ns	2	1.6	ns
40 ns	4	3.2	ns

Quad SPI Flash Timing Characteristics

Table 1-51: Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices

Symbol	Description	Min	Тур	Max	Unit
F _{clk}	SCLK_OUT clock frequency (External clock)	_	_	108	MHz
T _{qspi_clk}	QSPI_CLK clock period (Internal reference clock)	2.32			ns
T _{dutycycle}	SCLK_OUT duty cycle	45		55	%
T _{dssfrst}	Output delay QSPI_SS valid before first clock edge		1/2 cycle of SCLK_OUT		ns
T _{dsslst}	Output delay QSPI_SS valid after last clock edge	-1		1	ns
T _{dio}	I/O data output delay	-1		1	ns
T _{din_start}	Input data valid start			$(2 + R_{delay}) \times T_{qspi_clk} - 7.52^{(85)}$	ns



Symbol	Description	Min	Тур	Max	Unit
T _{din_end}	Input data valid end	$(2 + R_{delay}) \times T_{qspi_clk} - 1.21^{(85)}$			ns

Figure 1-8: Quad SPI Flash Timing Diagram

This timing diagram illustrates clock polarity mode 0 and clock phase mode 0.



Related Information

Quad SPI Flash Controller Chapter, Arria V Hard Processor System Technical Reference Manual

Provides more information about Rdelay.

SPI Timing Characteristics

Table 1-52: SPI Master Timing Requirements for Arria V Devices

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

Symbol	Description	Min	Max	Unit
T _{clk}	CLK clock period	16.67	—	ns
T _{su}	SPI Master-in slave-out (MISO) setup time	8.35 (86)	—	ns

 $^{^{(85)}}$ R_{delay} is set by programming the register <code>qspiregs.rddatacap</code>. For the SoC EDS software version 13.1 and later, Altera provides automatic Quad SPI calibration in the preloader. For more information about R_{delay}, refer to the Quad SPI Flash Controller chapter in the Arria V Hard Processor System Technical Reference Manual.



Figure 1-10: SPI Slave Timing Diagram



Related Information

SPI Controller, Arria V Hard Processor System Technical Reference Manual

Provides more information about rx_sample_delay.

SD/MMC Timing Characteristics

Table 1-54: Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices

After power up or cold reset, the Boot ROM uses drvsel = 3 and smplsel = 0 to execute the code. At the same time, the SD/MMC controller enters the Identification Phase followed by the Data Phase. During this time, the value of interface output clock SDMMC_CLK_OUT changes from a maximum of 400 kHz (Identification Phase) up to a maximum of 12.5 MHz (Data Phase), depending on the internal reference clock SDMMC_CLK and the CSEL setting. The value of SDMMC_CLK is based on the external oscillator frequency and has a maximum value of 50 MHz.



Figure 1-11: SD/MMC Timing Diagram



Related Information

Booting and Configuration Chapter, Arria V Hard Processor System Technical Reference Manual Provides more information about CSEL pin settings in the SD/MMC Controller CSEL Pin Settings table.

USB Timing Characteristics

PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board.

Table 1-55: USB Timing Requirements for Arria V Devices

Symbol	Description	Min	Тур	Мах	Unit
T _{clk}	USB CLK clock period	—	16.67	_	ns
T _d	CLK to USB_STP/USB_DATA[7:0] output delay	4.4	_	11	ns
T _{su}	Setup time for USB_DIR/USB_NXT/USB_DATA[7:0]	2			ns
T _h	Hold time for USB_DIR/USB_NXT/USB_DATA[7:0]	1			ns



Symbol	Parameter	Minimum	Maximum	Unit
t _{STATUS}	nSTATUS low pulse width	268	1506 ⁽⁹⁴⁾	μs
t _{CF2ST1}	nCONFIG high to nSTATUS high	—	1506 ⁽⁹⁵⁾	μs
t _{CF2CK} ⁽⁹⁶⁾	nCONFIG high to first rising edge on DCLK	1506	—	μs
t _{ST2CK} ⁽⁹⁶⁾	nSTATUS high to first rising edge of DCLK	2		μs
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t _{DH}	DATA[] hold time after rising edge on DCLK	0		ns
t _{CH}	DCLK high time	$0.45 imes 1/f_{MAX}$	—	S
t _{CL}	DCLK low time	$0.45 imes 1/f_{ m MAX}$	—	S
t _{CLK}	DCLK period	1/f _{MAX}	—	S
f _{MAX}	DCLK frequency (FPP ×8/ ×16)	_	125	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽⁹⁷⁾	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	4× maximum DCLK period	_	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + ($T_{init} \times CLKUSR$ period)	_	_
T _{init}	Number of clock cycles required for device initialization	8,576	_	Cycles

FPP Configuration Timing

Provides the FPP configuration timing waveforms.



⁽⁹⁴⁾ You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.

⁽⁹⁵⁾ You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

⁽⁹⁶⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

⁽⁹⁷⁾ The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

AV-51002 2017.02.10

The Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

Arria V I/O Timing Spreadsheet

Provides the Arria V Excel-based I/O timing spreadsheet.

Programmable IOE Delay

Parameter ⁽¹¹² Available) Settings	Available	Minimum	Fast Model				Slow Model			llait
	Settings	Offset ⁽¹¹³⁾	Industrial	Commercial	-C4	-C5	-C6	- I 3	-15	
D1	32	0	0.508	0.517	0.870	1.063	1.063	0.872	1.057	ns
D3	8	0	1.763	1.795	2.999	3.496	3.571	3.031	3.643	ns
D4	32	0	0.508	0.518	0.869	1.063	1.063	1.063	1.057	ns
D5	32	0	0.508	0.517	0.870	1.063	1.063	0.872	1.057	ns

Table 1-76: I/O element (IOE) Programmable Delay for Arria V Devices

Programmable Output Buffer Delay

Table 1-77: Programmable Output Buffer Delay for Arria V Devices

This table lists the delay chain settings that control the rising and falling edge delays of the output buffer.

You can set the programmable output buffer delay in the Quartus Prime software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.



⁽¹¹²⁾ You can set this value in the Quartus Prime software by selecting **D1**, **D3**, **D4**, and **D5** in the **Assignment Name** column of **Assignment Editor**.

⁽¹¹³⁾ Minimum offset does not include the intrinsic delay.





Date	Version	Changes
Date December 2015	Version 2015.12.16	 Updated Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices table. Updated F_{clk}, T_{dutycycle}, and T_{dssfrst} specifications. Added T_{qspi_clk}, T_{din_starb}, and T_{din_end} specifications. Removed T_{dinmax} specifications. Updated the minimum specification for T_{clk} to 16.67 ns and removed the maximum specification in SPI Master Timing Requirements for Arria V Devices table. Updated Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices table. Updated T_{clk} to T_{sdmmc_clk_out} symbol. Updated T_{sdmmc_clk_out} and T_d specifications. Added T_{sdmmc_clk}, T_{su}, and T_h specifications. Removed T_{dinmax} specifications. Updated the following diagrams: Quad SPI Flash Timing Diagram SD/MMC Timing Diagram
		 Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.



Date	Version	Changes
January 2015	2015.01.30	Updated the description for V _{CC_AUX_SHARED} to "HPS auxiliary power supply" in the following tables:
		 Absolute Maximum Ratings for Arria V Devices HPS Power Supply Operating Conditions for Arria V SX and ST Devices
		• Added statement in I/O Standard Specifications: You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.
		• Updated the conditions for transceiver reference clock rise time and fall time: Measure at ±60 mV of differential signal. Added a note to the conditions: REFCLK performance requires to meet transmitter REFCLK phase noise specification.
		• Updated the description in Periphery Performance Specifications to mention that proper timing closure is required in design.
		• Updated HPS Clock Performance main_base_clk specifications from 525 MHz (for -I3 speed grade) and 462 MHz (for -C4 speed grade) to 400 MHz.
		• Updated HPS PLL VCO maximum frequency to 1,600 MHz (for -C5, -I5, and -C6 speed grades), 1,850 MHz (for -C4 speed grade), and 2,100 MHz (for -I3 speed grade).
		Changed the symbol for HPS PLL input jitter divide value from NR to N.
		• Removed "Slave select pulse width (Texas Instruments SSP mode)" parameter from the following tables:
		 SPI Master Timing Requirements for Arria V Devices SPI Slave Timing Requirements for Arria V Devices
		 Added descriptions to USB Timing Characteristics section in HPS Specifications: PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board.
		Added HPS JTAG timing specifications.
		• Updated FPGA JTAG timing specifications note as follows: A 1-ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, $t_{JPCO} = 13$ ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.
		• Updated the value in the V _{ICM} (AC Coupled) row and in note 6 from 650 mV to 750 mV in the Transceiver Specifications for Arria V GT and ST Devices table.



1-98 Document Revision History

Date	Version	Changes
July 2014	3.8	 Added a note in Table 3, Table 4, and Table 5: The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements. Updated V_{CC_HPS} specification in Table 5. Added a note in Table 19: Differential inputs are powered by V_{CCPD} which requires 2.5 V. Updated "Minimum differential eye opening at the receiver serial input pins" specification in Table 20 and Table 21. Updated description in "HPS PLL Specifications" section. Updated VCO range maximum specification in Table 39. Updated T_d and T_h specifications in Table 45. Added T_h specification in Table 47 and Figure 13. Updated a note in Figure 20, Figure 21, and Figure 23 as follows: Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required. Removed "Remote update only in AS mode" specification in Table 58. Added DCLK device initialization clock source specification in Table 60. Added description in "Configuration Files" section: The IOCSR .rbf size is specifically for the Configuration via Protocol (CvP) feature. Removed f_{MAX_RU_CLK} specification in Table 63.
February 2014	3.7	 Updated V_{CCRSTCLK_HPS} maximum specification in Table 1. Added V_{CC_AUX_SHARED} specification in Table 1.
December 2013	3.6	 Added "HPS PLL Specifications". Added Table 24, Table 39, and Table 40. Updated Table 1, Table 3, Table 5, Table 19, Table 20, Table 21, Table 38, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, Table 51, Table 55, Table 56, and Table 59. Updated Figure 7, Figure 13, Figure 15, Figure 16, and Figure 19. Removed table: GPIO Pulse Width for Arria V Devices.



- PowerPlay Early Power Estimator User Guide For more information about the EPE tool.
- **PowerPlay Power Analysis** ٠ For more information about PowerPlay power analysis.

Power Consumption

Altera offers two ways to estimate power consumption for a design-the Excel-based Early Power Estimator and the Quartus II PowerPlay Power Analyzer feature.

Note: You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

Related Information

- PowerPlay Early Power Estimator User Guide For more information about the EPE tool.
- PowerPlay Power Analysis For more information about PowerPlay power analysis.

I/O Pin Leakage Current

Table 2-8: I/O Pin Leakage Current for Arria V GZ Devices

If $V_O = V_{CCIO}$ to $V_{CCIOMax}$, 100 µA of leakage current per I/O is expected.

Symbol	Description	Conditions	Min	Тур	Max	Unit
II	Input pin	$V_I = 0 V$ to $V_{CCIOMAX}$	-30	—	30	μΑ
I _{OZ}	Tri-stated I/O pin	$V_{O} = 0 V$ to $V_{CCIOMAX}$	-30	_	30	μΑ



I/O Standard Specifications

The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL} , respectively.

Table 2-16: Single-Ended I/O Standards for Arria V GZ Devices

1/O Standard) Standard		V _{CCIO} (V)		V _{IL} (V)		(V)	V _{OL} (V)	V _{OH} (V)	Ι (mΔ)	Ι (m Λ)	
i/O Stanuaru	Min	Тур	Max	Min	Max	Min	Max	Мах	Min	10L (1114)	OH (IIII)	
LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2	
LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	V _{CCIO} – 0.2	0.1	-0.1	
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1	
1.8 V	1.71	1.8	1.89	-0.3	$0.35 \times V_{ m CCIO}$	0.65 × V _{CCIO}	V _{CCIO} + 0.3	0.45	V _{CCIO} – 0.45	2	-2	
1.5 V	1.425	1.5	1.575	-0.3	$0.35 \times V_{ m CCIO}$	0.65 × V _{CCIO}	V _{CCIO} + 0.3	$0.25 imes V_{ m CCIO}$	$0.75 \times V_{CCIO}$	2	-2	
1.2 V	1.14	1.2	1.26	-0.3	$0.35 \times V_{\rm CCIO}$	0.65 × V _{CCIO}	V _{CCIO} + 0.3	$0.25 \times V_{ m CCIO}$	$0.75 \times V_{CCIO}$	2	-2	

Table 2-17: Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V GZ Devices

I/O Standard	V _{CCIO} (V)				V _{REF} (V)		V _{TT} (V)			
	Min	Тур	Max	Min	Тур	Max	Min	Тур	Мах	
SSTL-2 Class I, II	2.375	2.5	2.625	$0.49 \times V_{CCIO}$	$0.5 imes V_{ m CCIO}$	$0.51 imes V_{ m CCIO}$	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04	
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04	
SSTL-15 Class I, II	1.425	1.5	1.575	$0.49 \times V_{CCIO}$	$0.5 imes V_{ m CCIO}$	0.51 × V _{CCIO}	$0.49 \times V_{CCIO}$	0.5 × VCCIO	$0.51 \times V_{CCIO}$	



Table 2-19: Differential SSTL I/O Standards for Arria V GZ Devices

I/O Standard	V _{CCIO} (V)			V _{SWING}	V _{SWING(DC)} (V)		$V_{X(AC)}(V)$			V _{SWING(AC)} (V)		
	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Max		
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V _{CCIO} + 0.6	V _{CCIO} /2 - 0.2		V _{CCIO} /2 + 0.2	0.62	$V_{CCIO} + 0.6$		
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V _{CCIO} + 0.6	V _{CCIO} /2 - 0.175	_	V _{CCIO} /2 + 0.175	0.5	$V_{CCIO} + 0.6$		
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(127)	V _{CCIO} /2 - 0.15		V _{CCIO} /2 + 0.15	0.35	_		
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	(127)	V _{CCIO} /2 - 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	$2(V_{IL(AC)} - V_{REF})$		
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(127)	V _{CCIO} /2 - 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	_		
SSTL-12 Class I, II	1.14	1.2	1.26	0.18		V _{REF} -0.15	V _{CCIO} /2	V _{REF} + 0.15	-0.30	0.30		

Table 2-20: Differential HSTL and HSUL I/O Standards for Arria V GZ Devices

I/O Standard	V _{CCIO} (V)		$V_{DIF(DC)}(V)$			V _{CM(DC)} (V)			V _{DIF(AC)} (V)				
	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Мах
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	_	0.78		1.12	0.78	_	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	_	0.68		0.9	0.68		0.9	0.4	—



 $^{^{(127)}}$ The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Sumbol/Description	Conditions	Trans	ceiver Spee	d Grade 2	Transc	Unit		
Symbol/Description	Conditions	Min	Тур	Мах	Min	Тур	Max	Onit
	$V_{CCR_GXB} = 0.85 V$ full bandwidth	—	600		_	600	_	mV
Varia (AC and DC coupled)	$V_{CCR_GXB} = 0.85 V$ half bandwidth	—	600		_	600	_	mV
V _{ICM} (AC and DC coupled)	$V_{CCR_{GXB}} = 1.0 V$ full bandwidth	—	700		—	700	_	mV
	$V_{CCR_{GXB}} = 1.0 V$ half bandwidth	—	700		_	700	_	mV
t _{LTR} ⁽¹⁴⁹⁾	—		—	10	—	—	10	μs
t _{LTD} ⁽¹⁵⁰⁾	—	4	—		4	_	_	μs
t _{LTD_manual} ⁽¹⁵¹⁾	—	4	—	_	4	—	—	μs
t _{LTR_LTD_manual} ⁽¹⁵²⁾	—	15	—		15	_	_	μs
Programmable equalization (AC Gain)	Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz)		_	16			16	dB

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Receiver



 $^{^{(149)}}$ t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

 $^{^{(150)}}$ t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.

⁽¹⁵¹⁾ t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.

 $t_{\text{LTR_LTD_manual}}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.

Mode ⁽¹⁶⁴⁾	Transceiver	PMA Width	20	20	16	16	10	10	8	8
	Speed Grade	PCS/Core Width	40	20	32	16	20	10	16	8
Decision	2	C3, I3L core speed grade	9.9	9	7.92	7.2	4.9	4.,5	3.92	3.6
icgistei	3	C4, I4 core speed grade	8.8	8.2	7.04	6.56	4.4	4.1	3.52	3.28

Operating Conditions on page 2-1

10G PCS Data Rate

Table 2-31: 10G PCS Approximate Maximum Data Rate (Gbps) for Arria V GZ Devices

Mode ⁽¹⁶⁵⁾	Transceiver Speed Grade	PMA Width	64	40	40	40	32	32
		PCS Width	64	66/67	50	40	64/66/67	32
FIFO	2	C3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88
	3	C4, I4 core speed grade	10.3125	10.3125	10.69	10.3125	9.92	9.92
Register	2	C3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88
	3	C4, I4 core speed grade	10.3125	10.3125	10.69	10.3125	9.92	9.92

⁽¹⁶⁴⁾ The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.



⁽¹⁶⁵⁾ The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.