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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	8962
Number of Logic Elements/Cells	190000
Total RAM Bits	13284352
Number of I/O	544
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/5agxfa5h4f35c5n">https://www.e-xfl.com/product-detail/intel/5agxfa5h4f35c5n</a>

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## I/O Standard Specifications

Tables in this section list the input voltage ( $V_{IH}$  and  $V_{IL}$ ), output voltage ( $V_{OH}$  and  $V_{OL}$ ), and current drive characteristics ( $I_{OH}$  and  $I_{OL}$ ) for various I/O standards supported by Arria V devices.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

### Single-Ended I/O Standards

**Table 1-14: Single-Ended I/O Standards for Arria V Devices**

I/O Standard	$V_{CCIO}$ (V)			$V_{IL}$ (V)		$V_{IH}$ (V)		$V_{OL}$ (V)	$V_{OH}$ (V)	$I_{OL}^{(13)}$ (mA)	$I_{OH}^{(13)}$ (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V LVTTL	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.45	2.4	4	-4
3.3-V LVCMOS	3.135	3.3	3.465	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	2	-2
3.0-V LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
3.0-V LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
3.0-V PCI	2.85	3	3.15	—	$0.3 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5
3.0-V PCI-X	2.85	3	3.15	—	$0.35 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	1.5	-0.5
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	0.45	$V_{CCIO} - 0.45$	2	-2
1.5 V	1.425	1.5	1.575	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
1.2 V	1.14	1.2	1.26	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2

<sup>(13)</sup> To meet the  $I_{OL}$  and  $I_{OH}$  specifications, you must set the current strength settings accordingly. For example, to meet the 3.3-V LVTTL specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the  $I_{OL}$  and  $I_{OH}$  specifications in the datasheet.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Data rate (10-Gbps transceiver) <sup>(44)</sup>	—	0.611	—	10.3125	Gbps
Absolute $V_{MAX}$ for a receiver pin <sup>(45)</sup>	—	—	—	1.2	V
Absolute $V_{MIN}$ for a receiver pin	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) before device configuration	—	—	—	1.6	V
Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) after device configuration	—	—	—	2.2	V
Minimum differential eye opening at the receiver serial input pins <sup>(46)</sup>	—	100	—	—	mV
$V_{ICM}$ (AC coupled)	—	—	750 <sup>(47)</sup> /800	—	mV
$V_{ICM}$ (DC coupled)	$\leq 3.2\text{Gbps}$ <sup>(48)</sup>	670	700	730	mV
Differential on-chip termination resistors	85- $\Omega$ setting	85			$\Omega$
	100- $\Omega$ setting	100			$\Omega$
	120- $\Omega$ setting	120			$\Omega$
	150- $\Omega$ setting	150			$\Omega$
$t_{LTR}$ <sup>(49)</sup>	—	—	—	10	$\mu\text{s}$
$t_{LTD}$ <sup>(50)</sup>	—	4	—	—	$\mu\text{s}$

<sup>(45)</sup> The device cannot tolerate prolonged operation at this absolute maximum.

<sup>(46)</sup> The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

<sup>(47)</sup> The AC coupled  $V_{ICM}$  is 750 mV for PCIe mode only.

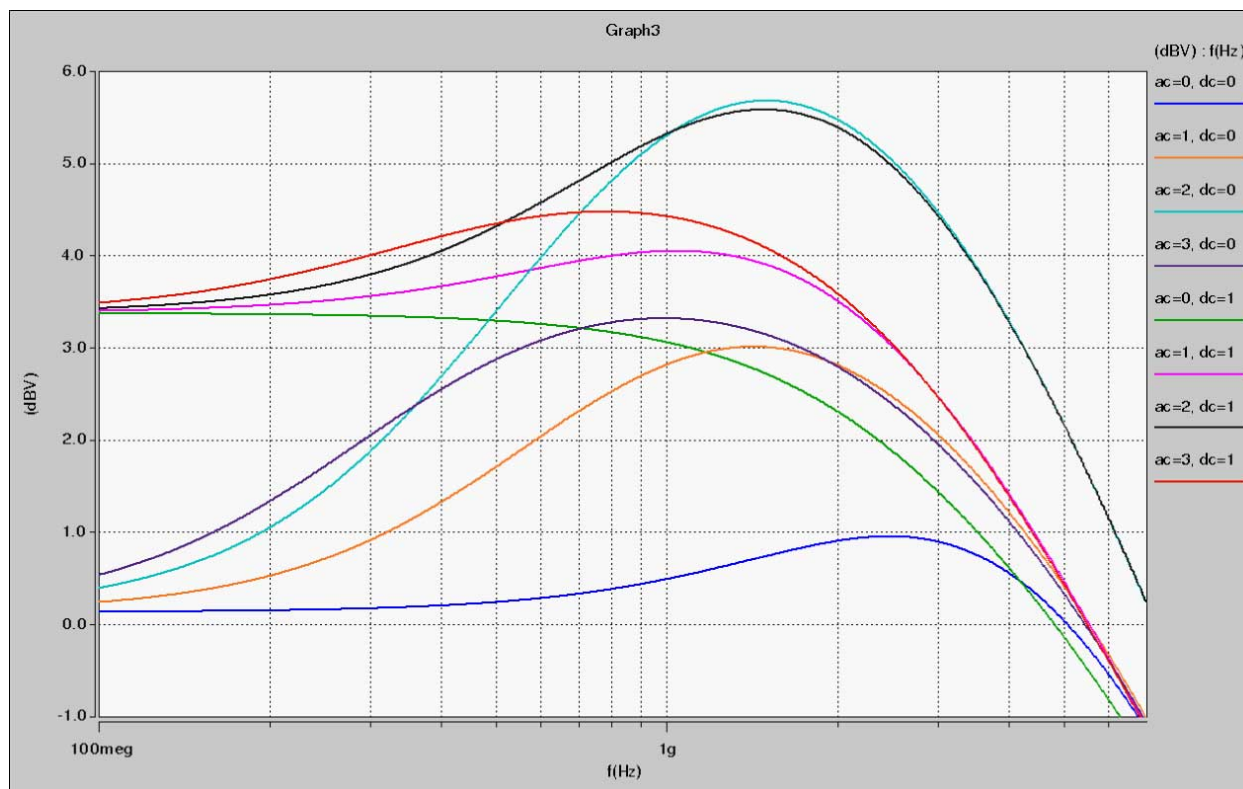
<sup>(48)</sup> For standard protocol compliance, use AC coupling.

<sup>(49)</sup>  $t_{LTR}$  is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

<sup>(50)</sup>  $t_{LTD}$  is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedto data` signal goes high.

## CTLE Response at Data Rates $\leq 3.25$ Gbps across Supported AC Gain and DC Gain

Figure 1-3: CTLE Response at Data Rates  $\leq 3.25$  Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices



Quartus Prime 1st Post Tap Pre-Emphasis Setting	Quartus Prime V <sub>OD</sub> Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
16	—	—	9.56	7.73	6.49	—	—	dB
17	—	—	10.43	8.39	7.02	—	—	dB
18	—	—	11.23	9.03	7.52	—	—	dB
19	—	—	12.18	9.7	8.02	—	—	dB
20	—	—	13.17	10.34	8.59	—	—	dB
21	—	—	14.2	11.1	—	—	—	dB
22	—	—	15.38	11.87	—	—	—	dB
23	—	—	—	12.67	—	—	—	dB
24	—	—	—	13.48	—	—	—	dB
25	—	—	—	14.37	—	—	—	dB
26	—	—	—	—	—	—	—	dB
27	—	—	—	—	—	—	—	dB
28	—	—	—	—	—	—	—	dB
29	—	—	—	—	—	—	—	dB
30	—	—	—	—	—	—	—	dB
31	—	—	—	—	—	—	—	dB

**Related Information****[SPICE Models for Altera Devices](#)**

Provides the Arria V HSSI HSPICE models.

**Transceiver Compliance Specification**

The following table lists the physical medium attachment (PMA) specification compliance of all supported protocol for Arria V GX, GT, SX, and ST devices. For more information about the protocol parameter details and compliance specifications, contact your Altera Sales Representative.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{IN}$	Input clock frequency	–3 speed grade	5	—	800 <sup>(61)</sup>	MHz
		–4 speed grade	5	—	800 <sup>(61)</sup>	MHz
		–5 speed grade	5	—	750 <sup>(61)</sup>	MHz
		–6 speed grade	5	—	625 <sup>(61)</sup>	MHz
$f_{INPFD}$	Integer input clock frequency to the phase frequency detector (PFD)	—	5	—	325	MHz
$f_{FINPFD}$	Fractional input clock frequency to the PFD	—	50	—	160	MHz
$f_{VCO}^{(62)}$	PLL voltage-controlled oscillator (VCO) operating range	–3 speed grade	600	—	1600	MHz
		–4 speed grade	600	—	1600	MHz
		–5 speed grade	600	—	1600	MHz
		–6 speed grade	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	—	40	—	60	%
$f_{OUT}$	Output frequency for internal global or regional clock	–3 speed grade	—	—	500 <sup>(63)</sup>	MHz
		–4 speed grade	—	—	500 <sup>(63)</sup>	MHz
		–5 speed grade	—	—	500 <sup>(63)</sup>	MHz
		–6 speed grade	—	—	400 <sup>(63)</sup>	MHz

<sup>(61)</sup> This specification is limited in the Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

<sup>(62)</sup> The VCO frequency reported by the Quartus Prime software takes into consideration the VCO post-scale counter  $\kappa$  value. Therefore, if the counter  $\kappa$  has a value of 2, the frequency reported can be lower than the  $f_{VCO}$  specification.

<sup>(63)</sup> This specification is limited by the lower of the two: I/O  $f_{MAX}$  or  $F_{OUT}$  of the PLL.

## DPA Lock Time Specifications

Figure 1-4: Dynamic Phase Alignment (DPA) Lock Time Specifications with DPA PLL Calibration Enabled

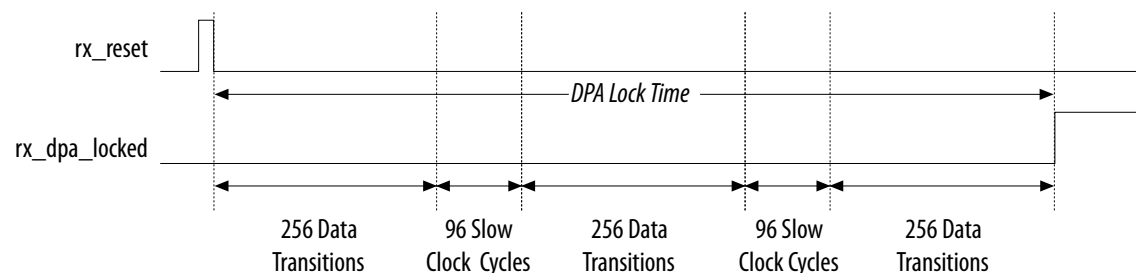


Table 1-41: DPA Lock Time Specifications for Arria V Devices

The specifications are applicable to both commercial and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions <sup>(84)</sup>	Maximum Data Transition
SPI-4	00000000001111111111	2	128	640
Parallel Rapid I/O	00001111	2	128	640
	10010000	4	64	640
Miscellaneous	10101010	8	32	640
	01010101	8	32	640

<sup>(84)</sup> This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.



## LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications

Figure 1-5: LVDS Soft-Clock Data Recovery (CDR)/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Equal to 1.25 Gbps

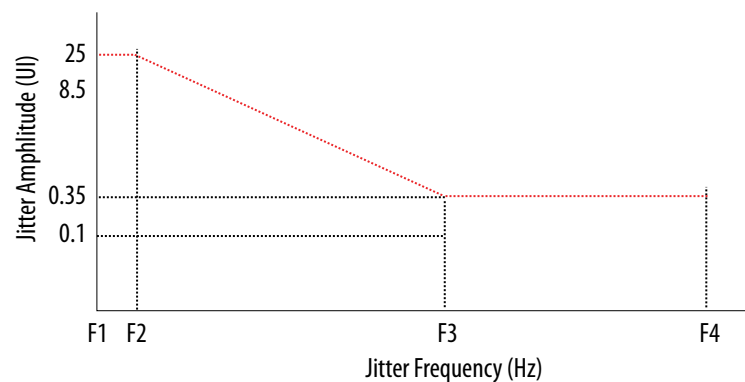


Table 1-42: LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.25 Gbps

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

## Initialization

**Table 1-71: Initialization Clock Source Option and the Maximum Frequency for Arria V Devices**

Initialization Clock Source	Configuration Scheme	Maximum Frequency (MHz)	Minimum Number of Clock Cycles
Internal Oscillator	AS, PS, and FPP	12.5	$T_{init}$
CLKUSR <sup>(107)</sup>	PS and FPP	125	
	AS	100	
DCLK	PS and FPP	125	

## Configuration Files

**Table 1-72: Uncompressed .rbf Sizes for Arria V Devices**

Use this table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (.hex) or tabular text file (.ttf) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Quartus Prime software. However, for a specific version of the Quartus Prime software, any design targeted for the same device has the same uncompressed configuration file size.

The IOCSR raw binary file (.rbf) size is specifically for the Configuration via Protocol (CvP) feature.

<sup>(107)</sup> To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus Prime software from the **General** panel of the **Device and Pin Options** dialog box.

Term	Definition
PLL specifications	<p>Diagram of PLL specifications</p> <p><b>Legend</b> Reconfigurable in User Mode</p> <p><b>Note:</b> (1) Core Clock can only be fed by dedicated clock input pins or PLL outputs.</p>
R <sub>L</sub>	Receiver differential input discrete resistor (external to the Arria V device).
Sampling window (SW)	<p>Timing diagram—The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown:</p> <p>Bit Time</p> <p>0.5 x TCCS   RSKM   Sampling Window (SW)   RSKM   0.5 x TCCS</p>

Date	Version	Changes
June 2012	2.0	<ul style="list-style-type: none"><li>• Updated for the Quartus II software v12.0 release:</li><li>• Restructured document.</li><li>• Updated “Supply Current and Power Consumption” section.</li><li>• Updated Table 20, Table 21, Table 24, Table 25, Table 26, Table 35, Table 39, Table 43, and Table 52.</li><li>• Added Table 22, Table 23, and Table 33.</li><li>• Added Figure 1–1 and Figure 1–2.</li><li>• Added “Initialization” and “Configuration Files” sections.</li></ul>
February 2012	1.3	<ul style="list-style-type: none"><li>• Updated Table 2–1.</li><li>• Updated Transceiver-FPGA Fabric Interface rows in Table 2–20.</li><li>• Updated <math>V_{CCP}</math> description.</li></ul>
December 2011	1.2	Updated Table 2–1 and Table 2–3.
November 2011	1.1	<ul style="list-style-type: none"><li>• Updated Table 2–1, Table 2–19, Table 2–26, and Table 2–36.</li><li>• Added Table 2–5.</li><li>• Added Figure 2–4.</li></ul>
August 2011	1.0	Initial release.

Symbol	Description	Condition	Minimum <sup>(114)</sup>	Typical	Maximum <sup>(114)</sup>	Unit
V <sub>I</sub>	DC input voltage	—	−0.5	—	3.6	V
V <sub>O</sub>	Output voltage	—	0	—	V <sub>CCIO</sub>	V
T <sub>J</sub>	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	−40	—	100	°C
t <sub>RAMP</sub>	Power supply ramp time	Standard POR	200 μs	—	100 ms	—
		Fast POR	200 μs	—	4 ms	—

### Recommended Transceiver Power Supply Operating Conditions

**Table 2-6: Recommended Transceiver Power Supply Operating Conditions for Arria V GZ Devices**

Symbol	Description	Minimum <sup>(118)</sup>	Typical	Maximum <sup>(118)</sup>	Unit
V <sub>CCA_GXBL</sub> (119), (120)	Transceiver channel PLL power supply (left side)	2.85	3.0	3.15	V
		2.375	2.5	2.625	
V <sub>CCA_GXBR</sub> (119), (120)	Transceiver channel PLL power supply (right side)	2.85	3.0	3.15	V
		2.375	2.5	2.625	
V <sub>CCHIP_L</sub>	Transceiver hard IP power supply (left side)	0.82	0.85	0.88	V
V <sub>CCHSSL_L</sub>	Transceiver PCS power supply (left side)	0.82	0.85	0.88	V
V <sub>CCHSSL_R</sub>	Transceiver PCS power supply (right side)	0.82	0.85	0.88	V

<sup>(114)</sup> The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

<sup>(118)</sup> This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

<sup>(119)</sup> This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

<sup>(120)</sup> When using ATX PLLs, the supply must be 3.0 V.

## I/O Standard Specifications

The  $V_{OL}$  and  $V_{OH}$  values are valid at the corresponding  $I_{OH}$  and  $I_{OL}$ , respectively.

Table 2-16: Single-Ended I/O Standards for Arria V GZ Devices

I/O Standard	$V_{CCIO}$ (V)			$V_{IL}$ (V)		$V_{IH}$ (V)		$V_{OL}$ (V)	$V_{OH}$ (V)	$I_{OL}$ (mA)	$I_{OH}$ (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVC MOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	0.45	$V_{CCIO} - 0.45$	2	-2
1.5 V	1.425	1.5	1.575	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
1.2 V	1.14	1.2	1.26	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2

Table 2-17: Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V GZ Devices

I/O Standard	$V_{CCIO}$ (V)			$V_{REF}$ (V)			$V_{TT}$ (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$V_{REF} - 0.04$	$V_{REF}$	$V_{REF} + 0.04$
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	$V_{REF} - 0.04$	$V_{REF}$	$V_{REF} + 0.04$
SSTL-15 Class I, II	1.425	1.5	1.575	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$

I/O Standard	$V_{CCIO}$ (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	$V_{CCIO} + 0.3$	—	$0.5 \times V_{CCIO}$	—	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$	0.3	$V_{CCIO} + 0.48$
HSUL-12	1.14	1.2	1.3	0.26	0.26	$0.5 \times V_{CCIO} - 0.12$	$0.5 \times V_{CCIO}$	$0.5 \times V_{CCIO} + 0.12$	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$	0.44	0.44

Table 2-21: Differential I/O Standard Specifications for Arria V GZ Devices

I/O Standard	$V_{CCIO}$ (V) <sup>(128)</sup>			$V_{ID}$ (mV) <sup>(129)</sup>			$V_{ICM(DC)}$ (V)			$V_{OD}$ (V) <sup>(130)</sup>			$V_{OCM}$ (V) <sup>(130)</sup>		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to the "Transceiver Performance Specifications" section.														
2.5 V LVDS <sup>(131)</sup>	2.375	2.5	2.625	100	$V_{CM} = 1.25$ V	—	0.05	$D_{MAX} \leq 700$ Mbps	1.8	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	$D_{MAX} > 700$ Mbps	1.55	0.247	—	0.6	1.125	1.25	1.375
BLVDS <sup>(132)</sup>	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—	—

<sup>(128)</sup> Differential inputs are powered by VCCPD which requires 2.5 V.

<sup>(129)</sup> The minimum  $V_{ID}$  value is applicable over the entire common mode range,  $V_{CM}$ .

<sup>(130)</sup> RL range:  $90 \leq RL \leq 110 \Omega$ .

<sup>(131)</sup> For optimized LVDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.

<sup>(132)</sup> There are no fixed  $V_{ICM}$ ,  $V_{OD}$ , and  $V_{OCM}$  specifications for BLVDS. They depend on the system topology.

## Switching Characteristics

### Transceiver Performance Specifications

#### Reference Clock

**Table 2-22: Reference Clock Specifications for Arria V GZ Devices**

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Clock								
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL						
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS						
Input Reference Clock Frequency (CMU PLL) <sup>(137)</sup>	—	40	—	710	40	—	710	MHz
Input Reference Clock Frequency (ATX PLL) <sup>(137)</sup>	—	100	—	710	100	—	710	MHz

<sup>(137)</sup> The input reference clock frequency options depend on the data rate and the device speed grade.



Symbol	V <sub>OD</sub> Setting	V <sub>OD</sub> Value (mV)	V <sub>OD</sub> Setting	V <sub>OD</sub> Value (mV)
V <sub>OD</sub> differential peak to peak typical	15	300	47	940
	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260

## Core Performance Specifications

### Clock Tree Specifications

**Table 2-33: Clock Tree Performance for Arria V GZ Devices**

Symbol	Performance		Unit
	C3, I3L	C4, I4	
Global and Regional Clock	650	580	MHz
Periphery Clock	500	500	MHz

### PLL Specifications

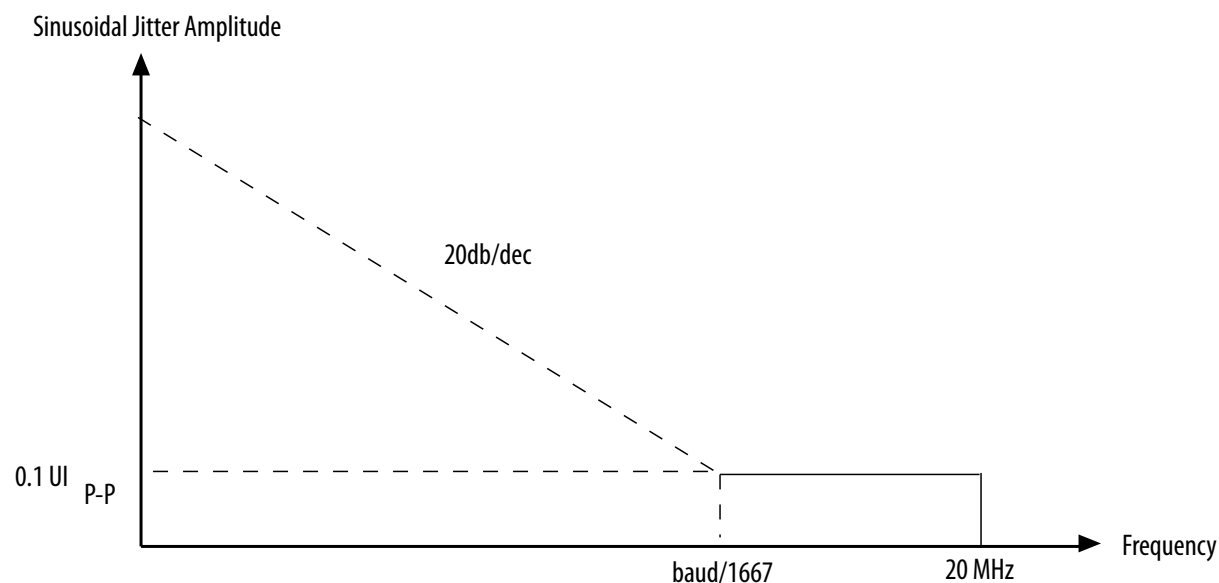
**Table 2-34: PLL Specifications for Arria V GZ Devices**

Symbol	Parameter	Min	Typ	Max	Unit
$f_{IN}^{(167)}$	Input clock frequency (C3, I3L speed grade)	5	—	800	MHz
	Input clock frequency (C4, I4 speed grade)	5	—	650	MHz
$f_{INPFD}$	Input frequency to the PFD	5	—	325	MHz
$f_{FINPFD}$	Fractional Input clock frequency to the PFD	50	—	160	MHz
$f_{VCO}^{(168)}$	PLL VCO operating range (C3, I3L speed grade)	600	—	1600	MHz
	PLL VCO operating range (C4, I4 speed grade)	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%

<sup>(167)</sup> This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

<sup>(168)</sup> The VCO frequency reported by the Quartus II software in the **PLL Usage Summary** section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the  $f_{VCO}$  specification.

Figure 2-5: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate &lt; 1.25 Gbps



## Non DPA Mode High-Speed I/O Specifications

Table 2-46: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

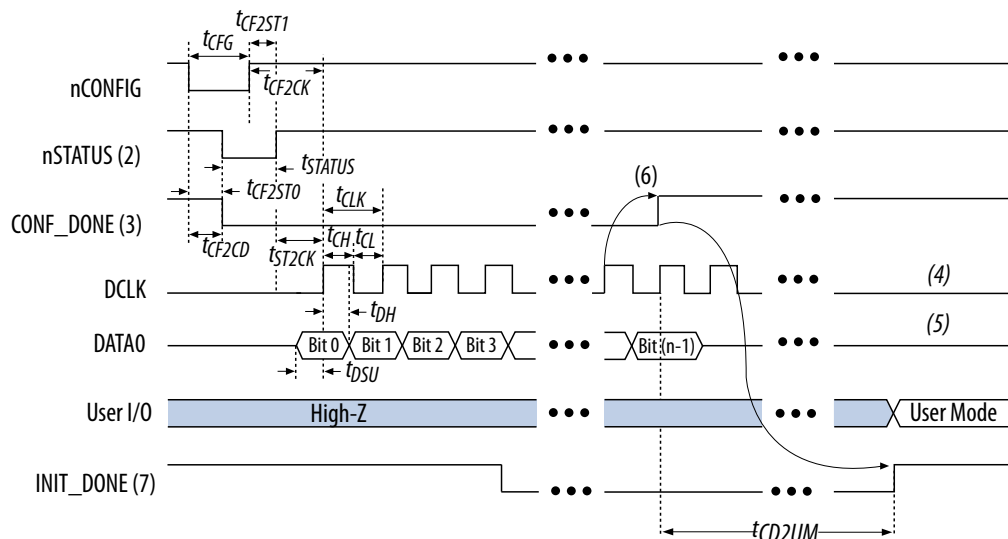
When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Sampling Window	—	—	—	300	—	—	300	ps

## Passive Serial Configuration Timing

Figure 2-10: PS Configuration Timing Waveform

Timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.



### Notes:

1. The beginning of this waveform shows the device in user mode. In user mode, **nCONFIG**, **nSTATUS**, and **CONF\_DONE** are at logic high levels. When **nCONFIG** is pulled low, a reconfiguration cycle begins.
2. After power-up, the Arria V GZ device holds **nSTATUS** low for the time of the POR delay.
3. After power-up, before and during configuration, **CONF\_DONE** is low.
4. Do not leave **DCLK** floating after configuration. **DCLK** is ignored after configuration is complete. It can toggle high or low if required.
5. **DATA0** is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the Device and Pins Option.
6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. **CONF\_DONE** is released high after the Arria V GZ device receives all the configuration data successfully. After **CONF\_DONE** goes high, send two additional falling edges on **DCLK** to begin initialization and enter user mode.
7. After the option bit to enable the **INIT\_DONE** pin is configured into the device, the **INIT\_DONE** goes low.

Term	Definition
$V_{OCM}$	Output common mode voltage—The common mode of the differential signal at the transmitter.
$V_{OD}$	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
$V_{SWING}$	Differential input voltage
$V_X$	Input differential cross point voltage
$V_{OX}$	Output differential cross point voltage
W	High-speed I/O block—clock boost factor

## Document Revision History

Date	Version	Changes
February 2017	2017.02.10	<ul style="list-style-type: none"> <li>Changed the minimum value for <math>t_{CD2UMC}</math> in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1" table.</li> <li>Changed the minimum value for <math>t_{CD2UMC}</math> in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is &gt;1" table.</li> <li>Changed the minimum value for <math>t_{CD2UMC}</math> in the "AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices" table.</li> <li>Changed the minimum value for <math>t_{CD2UMC}</math> in the "PS Timing Parameters for Arria V GZ Devices" table.</li> <li>Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices" table.</li> </ul>