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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	8962
Number of Logic Elements/Cells	190000
Total RAM Bits	13284352
Number of I/O	544
Number of Gates	-
Voltage - Supply	1.12V ~ 1.18V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxfa5h4f35i3g

Symbol	Description	Minimum	Maximum	Unit
V _{CCPLL_HPS}	HPS PLL analog power supply	–0.50	3.25	V
V _{CC_AUX_SHARED}	HPS auxiliary power supply	–0.50	3.25	V
I _{OUT}	DC output current per pin	–25	40	mA
T _J	Operating junction temperature	–55	125	°C
T _{STG}	Storage temperature (no bias)	–65	150	°C

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 4.00 V can only be at 4.00 V for ~15% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 1.5 years.

Table 1-2: Maximum Allowed Overshoot During Transitions for Arria V Devices

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
Vi (AC)	AC input voltage	3.8	100	%
		3.85	68	%
		3.9	45	%
		3.95	28	%
		4	15	%
		4.05	13	%
		4.1	11	%
		4.15	9	%
		4.2	8	%
		4.25	7	%
		4.3	5.4	%
		4.35	3.2	%
		4.4	1.9	%
		4.45	1.1	%
		4.5	0.6	%
		4.55	0.4	%
		4.6	0.2	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Arria V devices.

Recommended Operating Conditions

Table 1-3: Recommended Operating Conditions for Arria V Devices

This table lists the steady-state voltage values expected from Arria V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum ⁽⁷⁾	Typical	Maximum ⁽⁷⁾	Unit
V _{CC_AUX_SHARED}	HPS auxiliary power supply	—	2.375	2.5	2.625	V

Related Information

Recommended Operating Conditions on page 1-4

Provides the steady-state voltage values for the FPGA portion of the device.

DC Characteristics**Supply Current and Power Consumption**

Altera offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the Quartus® Prime PowerPlay Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the resources you use.

The Quartus Prime PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

Related Information

- **PowerPlay Early Power Estimator User Guide**
Provides more information about power estimation tools.
- **PowerPlay Power Analysis chapter, Quartus Prime Handbook**
Provides more information about power estimation tools.

⁽⁷⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Parameter	Symbol	Condition	V _{CCIO} (V)												Unit
			1.2		1.5		1.8		2.5		3.0		3.3		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold trip point	V _{TRIP}	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 1-8: OCT Calibration Accuracy Specifications for Arria V Devices

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (V)	Calibration Accuracy			Unit
			-I3, -C4	-I5, -C5	-C6	
25- Ω R_S	Internal series termination with calibration (25- Ω setting)	$V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2$	± 15	± 15	± 15	%
50- Ω R_S	Internal series termination with calibration (50- Ω setting)	$V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2$	± 15	± 15	± 15	%
34- Ω and 40- Ω R_S	Internal series termination with calibration (34- Ω and 40- Ω setting)	$V_{CCIO} = 1.5, 1.35, 1.25, 1.2$	± 15	± 15	± 15	%
48- Ω , 60- Ω , and 80- Ω R_S	Internal series termination with calibration (48- Ω , 60- Ω , and 80- Ω setting)	$V_{CCIO} = 1.2$	± 15	± 15	± 15	%
50- Ω R_T	Internal parallel termination with calibration (50- Ω setting)	$V_{CCIO} = 2.5, 1.8, 1.5, 1.2$	-10 to +40	-10 to +40	-10 to +40	%
20- Ω , 30- Ω , 40- Ω , 60- Ω , and 120- Ω R_T	Internal parallel termination with calibration (20- Ω , 30- Ω , 40- Ω , 60- Ω , and 120- Ω setting)	$V_{CCIO} = 1.5, 1.35, 1.25$	-10 to +40	-10 to +40	-10 to +40	%

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	$I_{OL}^{(14)}$ (mA)	$I_{OH}^{(14)}$ (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
HSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-12 Class I	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	16	-16
HSUL-12	—	$V_{REF} - 0.13$	$V_{REF} + 0.13$	—	$V_{REF} - 0.22$	$V_{REF} + 0.22$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	—	—

Differential SSTL I/O Standards

Table 1-17: Differential SSTL I/O Standards for Arria V Devices

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.62	$V_{CCIO} + 0.6$
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	$V_{CCIO} + 0.6$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	⁽¹⁵⁾	$V_{CCIO}/2 - 0.15$	—	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$
SSTL-135	1.283	1.35	1.45	0.18	⁽¹⁵⁾	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$

⁽¹⁴⁾ To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

⁽¹⁵⁾ The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Transceiver Specifications for Arria V GT and ST Devices

Table 1-26: Reference Clock Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O standards	1.2 V PCML, 1.4 VPCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL ⁽⁴⁰⁾ , HCSL, and LVDS				
Input frequency from REFCLK input pins	—	27	—	710	MHz
Rise time	Measure at ±60 mV of differential signal ⁽⁴¹⁾	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal ⁽⁴¹⁾	—	—	400	ps
Duty cycle	—	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	300 ⁽⁴²⁾ /2000	mV
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	Ω
V _{ICM} (AC coupled)	—	—	1.2	—	V
V _{ICM} (DC coupled)	HCSL I/O standard for the PCIe reference clock	250	—	550	mV

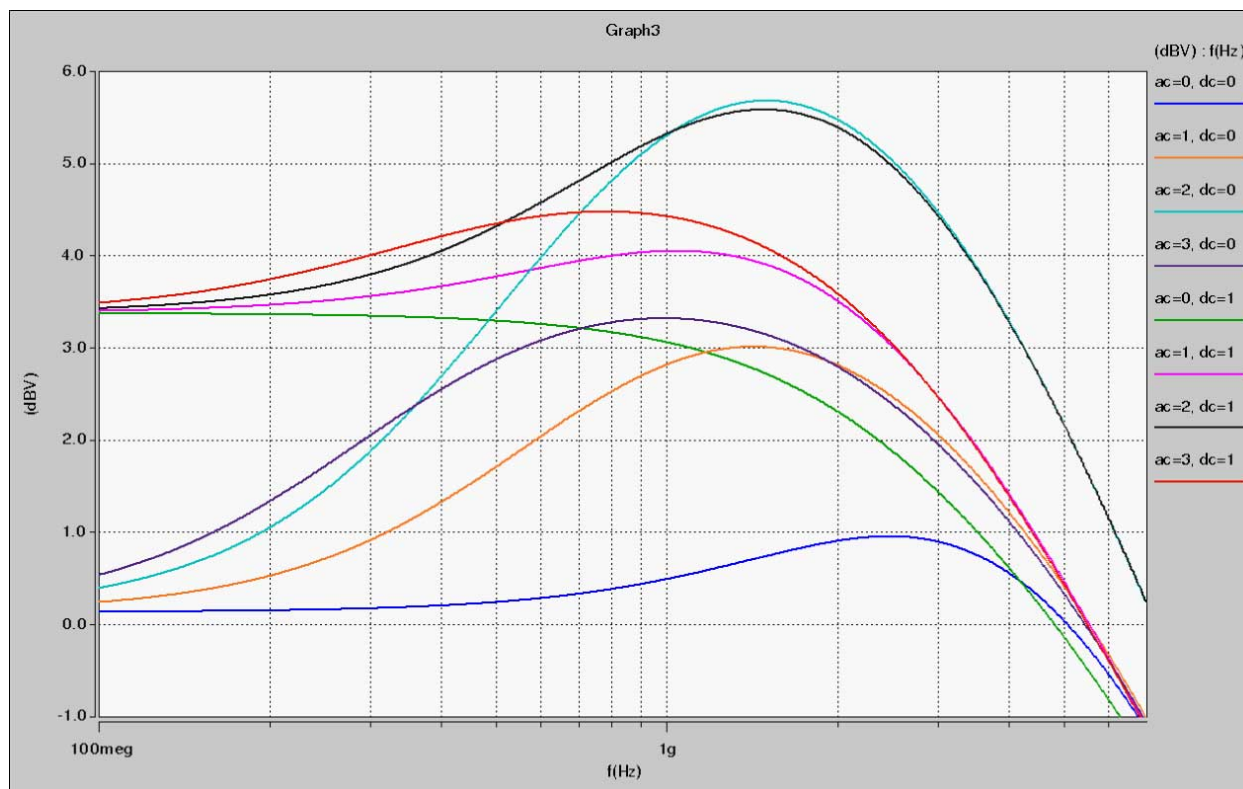
⁽⁴⁰⁾ Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

⁽⁴¹⁾ REFCLK performance requires to meet transmitter REFCLK phase noise specification.

⁽⁴²⁾ The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain

Figure 1-3: CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices



Symbol	V _{OD} Setting ⁽⁵⁸⁾	V _{OD} Value (mV)	V _{OD} Setting ⁽⁵⁸⁾	V _{OD} Value (mV)
	25	500	53	1060
	26	520	54	1080
	27	540	55	1100
	28	560	56	1120
	29	580	57	1140
	30	600	58	1160
	31	620	59	1180
	32	640	60	1200
	33	660		

Transmitter Pre-Emphasis Levels

The following table lists the simulation data on the transmitter pre-emphasis levels in dB for the first post tap under the following conditions:

- Low-frequency data pattern—five 1s and five 0s
- Data rate—2.5 Gbps

The levels listed are a representation of possible pre-emphasis levels under the specified conditions only and the pre-emphasis levels may change with data pattern and data rate.

Arria V devices only support 1st post tap pre-emphasis with the following conditions:

- The 1st post tap pre-emphasis settings must satisfy $|B| + |C| \leq 60$ where $|B| = V_{OD}$ setting with termination value, $R_{TERM} = 100 \Omega$ and $|C| = 1st$ post tap pre-emphasis setting.
- $|B| - |C| > 5$ for data rates < 5 Gbps and $|B| - |C| > 8.25$ for data rates > 5 Gbps.
- $(V_{MAX}/V_{MIN} - 1)\% < 600\%$, where $V_{MAX} = |B| + |C|$ and $V_{MIN} = |B| - |C|$.

Exception for PCIe Gen2 design: V_{OD} setting = 43 and pre-emphasis setting = 19 are allowed for PCIe Gen2 design with transmit de-emphasis – 6dB setting (pipe_txdeemp = 1'b0) using Altera PCIe Hard IP and PIPE IP cores.

⁽⁵⁸⁾ Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

Protocol	Sub-protocol	Data Rate (Mbps)
Common Public Radio Interface (CPRI)	CPRI E6LV	614.4
	CPRI E6HV	614.4
	CPRI E6LVII	614.4
	CPRI E12LV	1,228.8
	CPRI E12HV	1,228.8
	CPRI E12LVII	1,228.8
	CPRI E24LV	2,457.6
	CPRI E24LVII	2,457.6
	CPRI E30LV	3,072
	CPRI E30LVII	3,072
	CPRI E48LVII	4,915.2
	CPRI E60LVII	6,144
	CPRI E96LVIII ⁽⁶⁰⁾	9,830.4
Gbps Ethernet (GbE)	GbE 1250	1,250
OBSAI	OBSAI 768	768
	OBSAI 1536	1,536
	OBSAI 3072	3,072
	OBSAI 6144	6,144
Serial digital interface (SDI)	SDI 270 SD	270
	SDI 1485 HD	1,485
	SDI 2970 3G	2,970

⁽⁶⁰⁾ You can achieve compliance with TX channel restriction of one HSSI channel per six-channel transceiver bank.

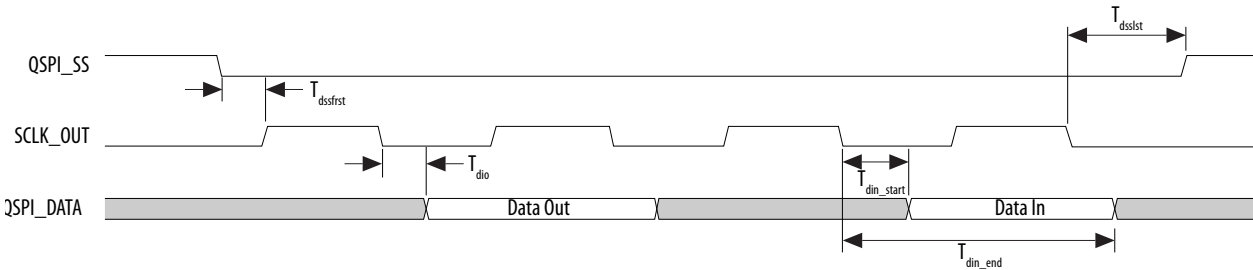
Symbol		Condition	-I3, -C4			-I5, -C5			-C6			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	TCCS	True Differential I/O Standards	—	—	150	—	—	150	—	—	150	ps
		Emulated Differential I/O Standards	—	—	300	—	—	300	—	—	300	ps
Receiver	True Differential I/O Standards - f_{HSDRDPA} (data rate)	SERDES factor J = 3 to 10 ⁽⁷⁶⁾	150	—	1250	150	—	1250	150	—	1050	Mbps
		SERDES factor J ≥ 8 with DPA ⁽⁷⁶⁾⁽⁷⁸⁾	150	—	1600	150	—	1500	150	—	1250	Mbps
	f_{HSDR} (data rate)	SERDES factor J = 3 to 10	⁽⁷⁷⁾	—	⁽⁸³⁾	⁽⁷⁷⁾	—	⁽⁸³⁾	⁽⁷⁷⁾	—	⁽⁸³⁾	Mbps
		SERDES factor J = 1 to 2, uses DDR registers	⁽⁷⁷⁾	—	⁽⁷⁹⁾	⁽⁷⁷⁾	—	⁽⁷⁹⁾	⁽⁷⁷⁾	—	⁽⁷⁹⁾	Mbps
DPA Mode	DPA run length	—	—	—	10000	—	—	10000	—	—	10000	UI
Soft-CDR Mode	Soft-CDR ppm tolerance	—	—	—	300	—	—	300	—	—	300	±ppm
Non-DPA Mode	Sampling Window	—	—	—	300	—	—	300	—	—	300	ps

⁽⁸³⁾ You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

Symbol	Description	Min	Typ	Max	Unit
T_{din_end}	Input data valid end	$(2 + R_{delay}) \times T_{qspi_clk} - 1.21^{(85)}$	—	—	ns

Figure 1-8: Quad SPI Flash Timing Diagram

This timing diagram illustrates clock polarity mode 0 and clock phase mode 0.



Related Information

[Quad SPI Flash Controller Chapter, Arria V Hard Processor System Technical Reference Manual](#)

Provides more information about Rdelay.

SPI Timing Characteristics

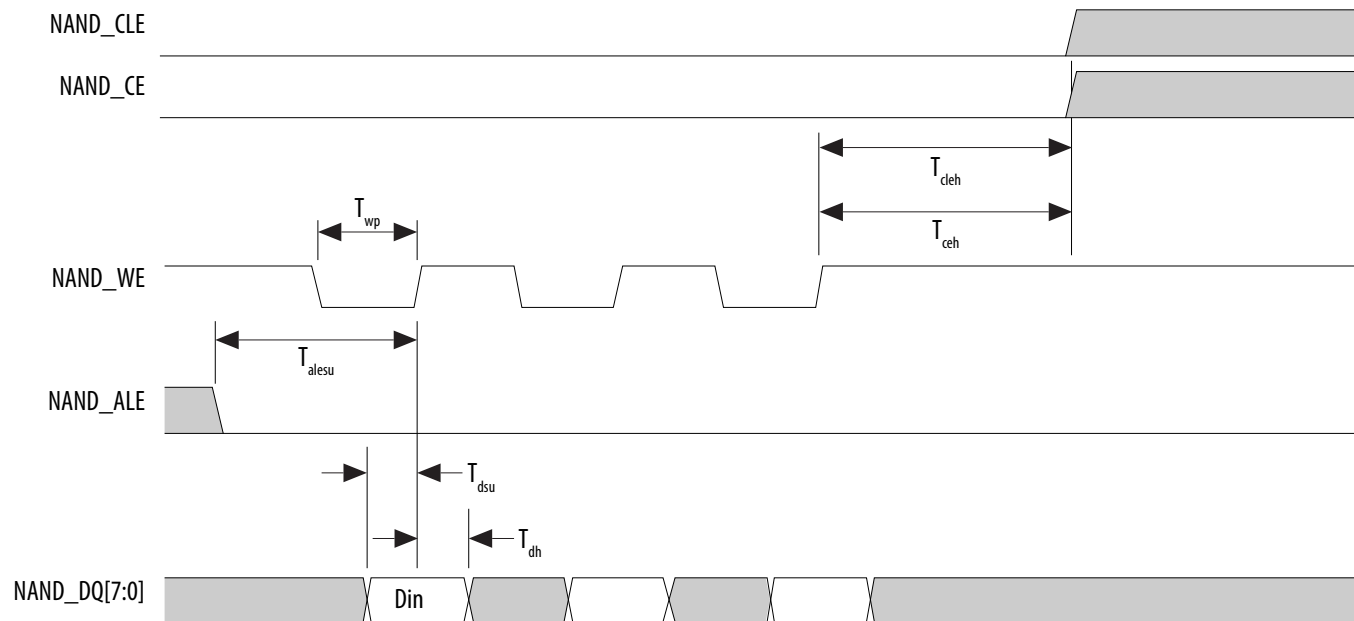
Table 1-52: SPI Master Timing Requirements for Arria V Devices

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

Symbol	Description	Min	Max	Unit
T_{clk}	CLK clock period	16.67	—	ns
T_{su}	SPI Master-in slave-out (MISO) setup time	8.35 ⁽⁸⁶⁾	—	ns

⁽⁸⁵⁾ R_{delay} is set by programming the register `qspiregs.rddatacap`. For the SoC EDS software version 13.1 and later, Altera provides automatic Quad SPI calibration in the preloader. For more information about R_{delay} , refer to the Quad SPI Flash Controller chapter in the Arria V Hard Processor System Technical Reference Manual.

Figure 1-19: NAND Data Write Timing Diagram



FPP Configuration Timing

DCLK-to-DATA[] Ratio (r) for FPP Configuration

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP $\times 16$ where the r is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

Table 1-65: DCLK-to-DATA[] Ratio for Arria V Devices

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
FPP (8-bit wide)	Off	Off	1
	On	Off	1
	Off	On	2
	On	On	2
FPP (16-bit wide)	Off	Off	1
	On	Off	2
	Off	On	4
	On	On	4

FPP Configuration Timing when DCLK-to-DATA[] = 1

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP $\times 8$ and FPP $\times 16$. For the respective DCLK-to-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Arria V Devices table.

Table 1-66: FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Arria V Devices

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	μ s

Date	Version	Changes
December 2015	2015.12.16	<ul style="list-style-type: none">Updated Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices table.<ul style="list-style-type: none">Updated F_{clk}, $T_{duty\ cycle}$, and $T_{dss\ first}$ specifications.Added T_{qspi_clk}, T_{din_start}, and T_{din_end} specifications.Removed $T_{din\ max}$ specifications.Updated the minimum specification for T_{clk} to 16.67 ns and removed the maximum specification in SPI Master Timing Requirements for Arria V Devices table.Updated Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices table.<ul style="list-style-type: none">Updated T_{clk} to $T_{sdmmc_clk_out}$ symbol.Updated $T_{sdmmc_clk_out}$ and T_d specifications.Added T_{sdmmc_clk}, T_{su}, and T_h specifications.Removed $T_{din\ max}$ specifications.Updated the following diagrams:<ul style="list-style-type: none">Quad SPI Flash Timing DiagramSD/MMC Timing DiagramUpdated configuration .rbf sizes for Arria V devices.Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.

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AV-51002



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This document covers the electrical and switching characteristics for Arria V GZ devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, core, and periphery performance. This document also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

Related Information**[Arria V Device Overview](#)**

For information regarding the densities and packages of devices in the Arria V GZ family.

Electrical Characteristics

Operating Conditions

When you use Arria V GZ devices, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Arria V GZ devices, you must consider the operating requirements described in this datasheet.

Arria V GZ devices are offered in commercial and industrial temperature grades.

Commercial devices are offered in –3 (fastest) and –4 core speed grades. Industrial devices are offered in –3L and –4 core speed grades. Arria V GZ devices are offered in –2 and –3 transceiver speed grades.

Table 2-1: Commercial and Industrial Speed Grade Offering for Arria V GZ Devices

C = Commercial temperature grade; I = Industrial temperature grade.

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Table 2-19: Differential SSTL I/O Standards for Arria V GZ Devices

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.62	$V_{CCIO} + 0.6$
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	$V_{CCIO} + 0.6$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	⁽¹²⁷⁾	$V_{CCIO}/2 - 0.15$	—	$V_{CCIO}/2 + 0.15$	0.35	—
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	⁽¹²⁷⁾	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	⁽¹²⁷⁾	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	—
SSTL-12 Class I, II	1.14	1.2	1.26	0.18	—	$V_{REF} - 0.15$	$V_{CCIO}/2$	$V_{REF} + 0.15$	-0.30	0.30

Table 2-20: Differential HSTL and HSUL I/O Standards for Arria V GZ Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—

⁽¹²⁷⁾ The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Typical VOD Settings

Table 2-32: Typical V_{OD} Setting for Arria V GZ Channel, TX Termination = 100 Ω

The tolerance is +/-20% for all VOD settings except for settings 2 and below.

Symbol	V_{OD} Setting	V_{OD} Value (mV)	V_{OD} Setting	V_{OD} Value (mV)
V_{OD} differential peak to peak typical	0 ⁽¹⁶⁶⁾	0	32	640
	1 ⁽¹⁶⁶⁾	20	33	660
	2 ⁽¹⁶⁶⁾	40	34	680
	3 ⁽¹⁶⁶⁾	60	35	700
	4 ⁽¹⁶⁶⁾	80	36	720
	5 ⁽¹⁶⁶⁾	100	37	740
	6	120	38	760
	7	140	39	780
	8	160	40	800
	9	180	41	820
	10	200	42	840
	11	220	43	860
	12	240	44	880
	13	260	45	900
	14	280	46	920

⁽¹⁶⁶⁾ If TX termination resistance = 100 Ω , this VOD setting is illegal.

Description	Min	Typ	Max	Unit
Diode ideality factor	1.006	1.008	1.010	—

Periphery Performance

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

Note: The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

High-Speed Clock Specifications

Table 2-39: High-Speed Clock Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

Arria V GZ devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 230 Mbps
- True mini-LVDS output standard with data rates of up to 340 Mbps

Figure 2-4: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate ≥ 1.25 Gbps

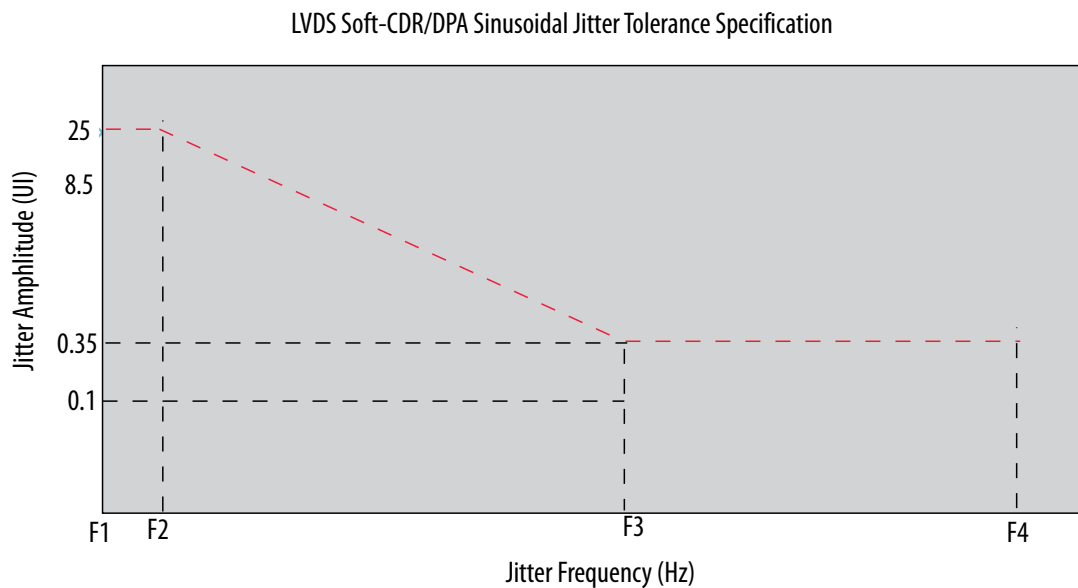


Table 2-45: LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate ≥ 1.25 Gbps

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Date	Version	Changes
June 2016	2016.06.20	<ul style="list-style-type: none">Changed column heading from "Value" to "Maximum" in the "Pin Capacitance for Arria V GZ Devices" table.Changed the minimum supported data rate range values from "1000" to "2000" in the "ATX PLL Specifications for Arria V GZ Devices" table.Added the supported data rates for the following output standards using true LVDS output buffer types in the "High-Speed Clock Specifications for Arria V GZ Devices" table:<ul style="list-style-type: none">True RSDS output standard: data rates of up to 230 MbpsTrue mini-LVDS output standard: data rates of up to 340 Mbps
December 2015	2015.12.16	<ul style="list-style-type: none">Removed the CDR ppm tolerance specification from the "Receiver Specifications for Arria V GZ Devices" table.Removed transmitter rise and fall time specifications from the "Transmitter Specifications for Arria V GZ Devices" table.Changed the .rbf sizes in the "Uncompressed .rbf Sizes for Arria V GZ Devices" table.Added a footnote to the "Transmitter High-Speed I/O Specifications for Arria V GZ Devices" table.
June 2015	2015.06.16	<ul style="list-style-type: none">Changed the conditions for the reference clock rise and fall time and added a note to the condition in the "Reference Clock Specifications for Arria V GZ Devices" table.Added a note to the "Minimum differential eye opening at receiver serial input pins" specification in the "Receiver Specifications for Arria V GZ Devices" table.
January 2015	2015.01.30	<ul style="list-style-type: none">Added 240-Ω to the "OCT Calibration Accuracy Specifications for Arria V GZ Devices" table.Changed the CDR PPM tolerance spec in the "Receiver Specifications for Arria V GZ Devices" table.Added additional max data rate for fPLL in the "Fractional PLL Specifications for Arria V GZ Devices" table.