Intel - 5AGXFA7H4F35C5N Datasheet





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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

2014.10	
Product Status	Obsolete
Number of LABs/CLBs	11460
Number of Logic Elements/Cells	242000
Total RAM Bits	15470592
Number of I/O	544
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxfa7h4f35c5n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

AV-51002 2017.02.10

1-5

Symbol	Description	Condition	Minimum ⁽¹⁾	Typical	Maximum ⁽¹⁾	Unit
V	Core voltage power supply	-C4, -I5, -C5, -C6	1.07	1.1	1.13	V
V CC	Core voltage power suppry	-I3	1.12	1.15	1.18	V
V	Periphery circuitry, PCIe hard IP block,	-C4, -I5, -C5, -C6	1.07	1.1	1.13	V
V CCP	and transceiver PCS power supply	-I3	1.12	1.15	1.18	V
		3.3 V	3.135	3.3	3.465	V
37	Configuration pins power supply	3.0 V	2.85	3.0	3.15	V
V CCPGM		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
V _{CC_AUX}	Auxiliary supply	_	2.375	2.5	2.625	V
V _{CCBAT} ⁽²⁾	Battery back-up power supply	_	1.2	—	3.0	V
	(For design security volatile key register)					
		3.3 V	3.135	3.3	3.465	V
V _{CCPD} ⁽³⁾	I/O pre-driver power supply	3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V

⁽¹⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(2) If you do not use the design security feature in Arria V devices, connect V_{CCBAT} to a 1.5-V, 2.5-V, or 3.0-V power supply. Arria V power-on reset (POR) circuitry monitors V_{CCBAT}. Arria V devices do not exit POR if V_{CCBAT} is not powered up.



⁽³⁾ V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25, or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V. V_{CCPD} must be 3.3 V when V_{CCIO} is 3.3 V.

Figure 1-1: Equation for OCT Variation Without Recalibration

$$R_{OCT} = R_{SCAL} \left(1 + \left(\frac{dR}{dT} \times \Delta T \right) \pm \left(\frac{dR}{dV} \times \Delta V \right) \right)$$

The definitions for the equation are as follows:

- The R_{OCT} value calculated shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
- R_{SCAL} is the OCT resistance value at power-up.
- ΔT is the variation of temperature with respect to the temperature at power up.
- ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
- dR/dT is the percentage change of R_{SCAL} with temperature.
- dR/dV is the percentage change of R_{SCAL} with voltage.

OCT Variation after Power-Up Calibration

Table 1-10: OCT Variation after Power-Up Calibration for Arria V Devices

This table lists OCT variation with temperature and voltage after power-up calibration. The OCT variation is valid for a V_{CCIO} range of $\pm 5\%$ and a temperature range of 0°C to 85°C.

Symbol	Description	V _{CCIO} (V)	Value	Unit
dR/dV		3.0	0.100	
		2.5	0.100	
	OCT variation with voltage without recalibration	1.8	0.100	
		1.5	0.100	%/mV
		1.35	0.150	
		1.25	0.150	
		1.2	0.150	



Symbol	Description	Maximum	Unit
I _{XCVR-RX (DC)}	DC current per transceiver receiver (RX) pin	50	mA

Internal Weak Pull-Up Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up.

Table 1-13: Internal Weak Pull-Up Resistor Values for Arria V Devices

Symbol	Description	Condition (V) ⁽¹¹⁾	Value ⁽¹²⁾	Unit
		$V_{CCIO} = 3.3 \pm 5\%$	25	kΩ
		$V_{CCIO} = 3.0 \pm 5\%$	25	kΩ
		$V_{CCIO} = 2.5 \pm 5\%$	25	kΩ
D	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	$V_{CCIO} = 1.8 \pm 5\%$	25	kΩ
кру		$V_{CCIO} = 1.5 \pm 5\%$	25	kΩ
		$V_{CCIO} = 1.35 \pm 5\%$	25	kΩ
		$V_{CCIO} = 1.25 \pm 5\%$	25	kΩ
		$V_{CCIO} = 1.2 \pm 5\%$	25	kΩ

Related Information

Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines

Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.



⁽¹⁰⁾ The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

 $^{^{(11)}}$ Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

⁽¹²⁾ Valid with $\pm 10\%$ tolerances to cover changes over PVT.

I/O Standard	V _{IL}	_(DC) (V)	V _{IH(D}	_{C)} (V)	V _{IL(AC)} (V)	V _{IH(AC)} (V)	V _{OL} (V)	V _{OH} (V)	I _{OL} ⁽¹⁴⁾	I_{a} (mA)
	Min	Max	Min	Мах	Max	Min	Мах	Min	(mA) ^{•On}	
HSTL-15 Class II	—	V _{REF} – 0.1	$V_{REF} + 0.1$	_	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	V _{CCIO} – 0.4	16	-16
HSTL-12 Class I	-0.15	V _{REF} – 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	V _{REF} – 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	16	-16
HSUL-12	_	V _{REF} – 0.13	$V_{REF} + 0.13$	_	V _{REF} - 0.22	V _{REF} + 0.22	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	_	_

Differential SSTL I/O Standards

Table 1-17: Differential SSTL I/O Standards for Arria V Devices

I/O Standard	V _{CCIO} (V)		V _{SWING(DC)} (V)		V _{X(AC)} (V)			V _{SWING(AC)} (V)		
	Min	Тур	Max	Min	Мах	Min	Тур	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V _{CCIO} + 0.6	V _{CCIO} /2 – 0.2	—	V _{CCIO} /2 + 0.2	0.62	$V_{CCIO} + 0.6$
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V _{CCIO} + 0.6	V _{CCIO} /2 – 0.175	—	V _{CCIO} /2 + 0.175	0.5	$V_{CCIO} + 0.6$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(15)	V _{CCIO} /2 – 0.15	—	V _{CCIO} /2 + 0.15	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$
SSTL-135	1.283	1.35	1.45	0.18	(15)	V _{CCIO} /2 – 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} – V _{REF})	$2(V_{IL(AC)} - V_{REF})$

⁽¹⁴⁾ To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.



 $^{^{(15)}}$ The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

• Transceiver Specifications for Arria V GT and ST Devices on page 1-29 Provides the specifications for transmitter, receiver, and reference clock I/O pin.

Switching Characteristics

This section provides performance characteristics of Arria V core and periphery blocks.

Transceiver Performance Specifications

Transceiver Specifications for Arria V GX and SX Devices

Table 1-20: Reference Clock Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
Symbol/Description	Condition	Min	Тур	Max	Min	Тур	Max	Onit
Supported I/O standards	1.2 V PCM	1.2 V PCML, 1.4 V PCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL ⁽²³⁾ , HCSL, and LVDS						
Input frequency from REFCLK input pins	—	27	—	710	27		710	MHz
Rise time	Measure at $\pm 60 \text{ mV of}$ differential signal ⁽²⁴⁾			400			400	ps
Fall time	Measure at $\pm 60 \text{ mV of}$ differential signal ⁽²⁴⁾	_		400	_		400	ps
Duty cycle	_	45	_	55	45	_	55	%
Peak-to-peak differential input voltage	—	200		300 ⁽²⁵⁾ / 2000	200	_	300 ⁽²⁵⁾ / 2000	mV



⁽²³⁾ Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

REFCLK performance requires to meet transmitter REFCLK phase noise specification. (24)

⁽²⁵⁾ The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

Sumbol/Decertistics	Condition	Т	115.4			
Symbol/Description	Condition	Min	Тур	Мах	onit	
Data rate (10-Gbps transceiver) ⁽⁴⁴⁾	—	0.611	0.611 —		Gbps	
Absolute $\mathrm{V}_{\mathrm{MAX}}$ for a receiver $\mathrm{pin}^{\scriptscriptstyle{(45)}}$	—	_		1.2	V	
Absolute $\mathrm{V}_{\mathrm{MIN}}$ for a receiver pin	—	-0.4		—	V	
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	Maximum peak-to-peak differential — input voltage V _{ID} (diff p-p) before device configuration		_	1.6	V	
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	_	_	_	2.2	V	
Minimum differential eye opening at the receiver serial input pins ⁽⁴⁶⁾	—	100		_	mV	
V _{ICM} (AC coupled)	—	_	750 ⁽⁴⁷⁾ /800	—	mV	
V _{ICM} (DC coupled)	\leq 3.2Gbps ⁽⁴⁸⁾	670	700	730	mV	
	85- Ω setting		85		Ω	
Differential on-chip termination	100- Ω setting		100		Ω	
resistors	120- Ω setting		120		Ω	
	150-Ω setting		Ω			
$t_{LTR}^{(49)}$	_	_		10	μs	
$t_{LTD}^{(50)}$	—	4	—	—	μs	

⁽⁴⁵⁾ The device cannot tolerate prolonged operation at this absolute maximum.



⁽⁴⁶⁾ The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

 $^{^{(47)}}$ The AC coupled $V_{\rm ICM}$ is 750 mV for PCIe mode only.

⁽⁴⁸⁾ For standard protocol compliance, use AC coupling.

 $^{^{(49)}}$ t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

⁽⁵⁰⁾ t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.

Symbol/Description	Condition	Tran	sceiver Speed Gra	Unit	
Symbol/Description	Condition	Min	Тур	Max	Ont
	85- Ω setting	—	85	—	Ω
Differential on-chip termination	100- Ω setting	—	100	—	Ω
resistors	120-Ω setting	—	120	—	Ω
	150-Ω setting		150	_	Ω
Intra-differential pair skew	TX V_{CM} = 0.65 V (AC coupled) and slew rate of 15 ps			15	ps
Intra-transceiver block transmitter channel-to-channel skew	×6 PMA bonded mode			180	ps
Inter-transceiver block transmitter channel-to-channel skew ⁽⁵⁵⁾	× <i>N</i> PMA bonded mode			500	ps

Table 1-30: CMU PLL Specifications for Arria V GT and ST Devices

Symbol/Description	Transceiver S	peed Grade 3	Unit
Symbol Description	Min	Max	onit
Supported data range	0.611	10.3125	Gbps
fPLL supported data range	611	3125	Mbps

⁽⁵⁵⁾ This specification is only applicable to channels on one side of the device across two transceiver banks.



Table 1-38: Memory Block Performance Specifications for Arria V Devices

Momory	Mada	Resourc	es Used	Performance			Unit
Memory	Mode	ALUTs	Memory	-I3, -C4	-I5, -C5	-C6	onit
MLAB	Single port, all supported widths	0	1	500	450	400	MHz
	Simple dual-port, all supported widths	0	1	500	450	400	MHz
	Simple dual-port with read and write at the same address	0	1	400	350	300	MHz
	ROM, all supported width	_		500	450	400	MHz
	Single-port, all supported widths	0	1	400	350	285	MHz
	Simple dual-port, all supported widths	0	1	400	350	285	MHz
M10K Block	Simple dual-port with the read-during- write option set to Old Data , all supported widths	0	1	315	275	240	MHz
	True dual port, all supported widths	0	1	400	350	285	MHz
	ROM, all supported widths	0	1	400	350	285	MHz

Internal Temperature Sensing Diode Specifications

Table 1-39: Internal Temperature Sensing Diode Specifications for Arria V Devices

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
-40 to 100°C	±8°C	No	1 MHz	< 100 ms	8 bits	8 bits

Periphery Performance

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.



Symbol		Condition		-I3, -C4			-l5, -C5			-C6		Unit
	Symbol	Condition	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
		True Differential I/O Standards		_	150		-	150	_	_	150	ps
		Emulated Differential I/O Standards			300		_	300		_	300	ps
True Differentia Standards - f _{HSI} (data rate)	True Differential I/O Standards - freepopp	SERDES factor J =3 to $10^{(76)}$	150		1250	150		1250	150		1050	Mbps
	(data rate)	SERDES factor $J \ge 8$ with DPA ⁽⁷⁶⁾⁽⁷⁸⁾	150	_	1600	150	_	1500	150	_	1250	Mbps
Receiver		SERDES factor J = 3 to 10	(77)	_	(83)	(77)	_	(83)	(77)	_	(83)	Mbps
	f _{HSDR} (data rate)	SERDES factor J = 1 to 2, uses DDR registers	(77)		(79)	(77)	_	(79)	(77)	_	(79)	Mbps
DPA Mode	DPA run length		_	_	10000	_	_	10000	_	_	10000	UI
Soft-CDR Mode	Soft-CDR ppm tolerance			_	300		_	300		_	300	±ppm
Non-DPA Mode	Sampling Window				300		_	300		_	300	ps

Arria V GX, GT, SX, and ST Device Datasheet



⁽⁸³⁾ You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

1-62 SPI Timing Characteristics

Symbol	Description	Min	Max	Unit
T _h	SPI MISO hold time	1	_	ns
T _{dutycycle}	SPI_CLK duty cycle	45	55	%
T _{dssfrst}	Output delay SPI_SS valid before first clock edge	8		ns
T _{dsslst}	Output delay SPI_SS valid after last clock edge	8		ns
T _{dio}	Master-out slave-in (MOSI) output delay	-1	1	ns

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Arria V GX, GT, SX, and ST Device Datasheet



⁽⁸⁶⁾ This value is based on rx_sample_dly = 1 and spi_m_clk = 120 MHz. spi_m_clk is the internal clock that is used by SPI Master to derive it's SCLK_OUT. These timings are based on rx_sample_dly of 1. This delay can be adjusted as needed to accommodate slower response times from the slave. Note that a delay of 0 is not allowed. The setup time can be used as a reference starting point. It is very crucial to do a calibration to get the correct rx_sample_dly value because each SPI slave device may have different output delay and each application board may have different path delay. For more information about rx_sample_delay, refer to the SPI Controller chapter in the Hard Processor System Technical Reference Manual.

Date	Version	Changes
January 2015	2015.01.30	Updated the description for V _{CC_AUX_SHARED} to "HPS auxiliary power supply" in the following tables:
		 Absolute Maximum Ratings for Arria V Devices HPS Power Supply Operating Conditions for Arria V SX and ST Devices
		• Added statement in I/O Standard Specifications: You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.
		• Updated the conditions for transceiver reference clock rise time and fall time: Measure at ±60 mV of differential signal. Added a note to the conditions: REFCLK performance requires to meet transmitter REFCLK phase noise specification.
		• Updated the description in Periphery Performance Specifications to mention that proper timing closure is required in design.
		• Updated HPS Clock Performance main_base_clk specifications from 525 MHz (for -I3 speed grade) and 462 MHz (for -C4 speed grade) to 400 MHz.
		• Updated HPS PLL VCO maximum frequency to 1,600 MHz (for -C5, -I5, and -C6 speed grades), 1,850 MHz (for -C4 speed grade), and 2,100 MHz (for -I3 speed grade).
		Changed the symbol for HPS PLL input jitter divide value from NR to N.
		• Removed "Slave select pulse width (Texas Instruments SSP mode)" parameter from the following tables:
		 SPI Master Timing Requirements for Arria V Devices SPI Slave Timing Requirements for Arria V Devices
		 Added descriptions to USB Timing Characteristics section in HPS Specifications: PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board.
		Added HPS JTAG timing specifications.
		• Updated FPGA JTAG timing specifications note as follows: A 1-ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, $t_{JPCO} = 13$ ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.
		• Updated the value in the V _{ICM} (AC Coupled) row and in note 6 from 650 mV to 750 mV in the Transceiver Specifications for Arria V GT and ST Devices table.



Symbol	Description	Minimum	Maximum	Unit
V _I	DC input voltage	-0.5	3.8	V
T _J	Operating junction temperature		125	°C
T _{STG}	Storage temperature (No bias)	-65	150	°C
I _{OUT}	DC output current per pin	-25	40	mA

Table 2-3: Transceiver Power Supply Absolute Conditions for Arria V GZ Devices

Symbol	Description	Minimum	Maximum	Unit
V _{CCA_GXBL}	Transceiver channel PLL power supply (left side)	-0.5	3.75	V
V _{CCA_GXBR}	Transceiver channel PLL power supply (right side)	-0.5	3.75	V
V _{CCHIP_L}	Transceiver hard IP power supply (left side)	-0.5	1.35	V
V _{CCHSSI_L}	Transceiver PCS power supply (left side)	-0.5	1.35	V
V _{CCHSSI_R}	Transceiver PCS power supply (right side)	-0.5	1.35	V
V _{CCR_GXBL}	Receiver analog power supply (left side)	-0.5	1.35	V
V _{CCR_GXBR}	Receiver analog power supply (right side)	-0.5	1.35	V
V _{CCT_GXBL}	Transmitter analog power supply (left side)	-0.5	1.35	V
V _{CCT_GXBR}	_GXBR Transmitter analog power supply (right side)		1.35	V
V _{CCH_GXBL}	CH_GXBL Transmitter output buffer power supply (left side)		1.8	V
V _{CCH_GXBR}	Transmitter output buffer power supply (right side)	-0.5	1.8	V

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in the following table. They may also undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.



2-28	Transmitter
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Sumbol/Description	Conditions	Transceiver Speed Grade 2			Transc	Unit			
Symbol/Description	Conditions	Min	Тур	Мах	Min	Тур	Max		
	85- Ω setting	—	85 ± 20%	_	_	85 ± 20%	—	Ω	
Differential on-chip termination	100- Ω setting		100 ± 20%			100 ± 20%	_	Ω	
resistors	120- Ω setting	—	120 ± 20%			120 ± 20%	_	Ω	
	150-Ω setting	_	150 ± 20%			150 ± 20%	_	Ω	
V _{OCM} (AC coupled)	0.65-V setting	—	650			650	_	mV	
V _{OCM} (DC coupled)	_	—	650			650	—	mV	
Intra-differential pair skew	Tx V _{CM} = 0.5 V and slew rate of 15 ps	—		15	_	_	15	ps	
Intra-transceiver block transmitter channel-to-channel skew	x6 PMA bonded mode			120			120	ps	
Inter-transceiver block transmitter channel-to-channel skew	xN PMA bonded mode			500			500	ps	

Related Information

Arria V Device Overview

For more information about device ordering codes.



2-44 Periphery Performance

Description	Min	Тур	Мах	Unit
Diode ideality factor	1.006	1.008	1.010	—

Periphery Performance

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

Note: The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

High-Speed Clock Specifications

Table 2-39: High-Speed Clock Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

Arria V GZ devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 230 Mbps
- True mini-LVDS output standard with data rates of up to 340 Mbps



Symbol	Conditions		C3, I3L			C4, I4	Unit	
Symbol	Conditions	Min	Тур	Мах	Min	Тур	Max	Onic
	SERDES factor J = 3 to 10 (192), (193), (194), (195), (196), (197)	150	_	1250	150	—	1050	Mbps
True Differential I/O Standards - f _{HSDRDPA} (data rate)	SERDES factor $J \ge 4$ LVDS RX with DPA (193), (195), (196), (197)	150	_	1600	150		1250	Mbps
(uata fate)	SERDES factor J = 2, uses DDR Registers	(198)	_	(199)	(198)		(199)	Mbps
	SERDES factor J = 1, uses SDR Register	(198)	_	(199)	(198)		(199)	Mbps
	SERDES factor $J = 3$ to 10	(198)	—	(200)	(198)	—	(200)	Mbps
f _{HSDR} (data rate)	SERDES factor J = 2, uses DDR Registers	(198)	—	(199)	(198)		(199)	Mbps
	SERDES factor J = 1, uses SDR Register	(198)	—	(199)	(198)	—	(199)	Mbps

 $^{(192)}$ The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

⁽¹⁹³⁾ Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.

⁽¹⁹⁴⁾ Arria V GZ LVDS serialization and de-serialization factor needs to be x4 and above.

⁽¹⁹⁵⁾ Requires package skew compensation with PCB trace length.

⁽¹⁹⁶⁾ Do not mix single-ended I/O buffer within LVDS I/O bank.

⁽¹⁹⁷⁾ Chip-to-chip communication only with a maximum load of 5 pF.

⁽¹⁹⁸⁾ The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

⁽¹⁹⁹⁾ The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.

⁽²⁰⁰⁾ You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.



OCT Calibration Block Specifications

Table 2-51: OCT Calibration Block Specifications for Arria V GZ Devices

Symbol	Description	Min	Тур	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
T _{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT R_S/R_T calibration		1000		Cycles
T _{OCTSHIFT}	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	_	32	—	Cycles
T _{RS_RT}	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between OCT R_S and R_T (See the figure below.)		2.5		ns

Figure 2-6: Timing Diagram for oe and dyn_term_ctrl Signals





2-70 Remote System Upgrades Circuitry Timing Specification

Table 2-62: Uncompressed .rbf Sizes for Arria V GZ Devices

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ⁽²²³⁾	
	E1	137,598,880	562,208	
Arria V CZ	E3	137,598,880	562,208	
Arria V GZ	E5	213,798,880	561,760	
	E7	213,798,880	561,760	

Table 2-63: Minimum Configuration Time Estimation for Arria V GZ Devices

Variant	Member Code	Active Serial ⁽²²⁴⁾			Fast Passive Parallel ⁽²²⁵⁾		
		Width	DCLK (MHz)	Min Config Time (ms)	Width	DCLK (MHz)	Min Config Time (ms)
Arria V GZ	E1	4	100	344	32	100	43
	E3	4	100	344	32	100	43
	E5	4	100	534	32	100	67
	E7	4	100	534	32	100	67

Remote System Upgrades Circuitry Timing Specification

Table 2-64: Remote System Upgrade Circuitry Timing Specifications

Parameter	Minimum	Maximum	Unit
t _{RU_nCONFIG} ⁽²²⁶⁾	250	_	ns
t _{RU_nRSTIMER} ⁽²²⁷⁾	250	_	ns

⁽²²³⁾ The IOCSR **.rbf** size is specifically for the Configuration via Protocol (CvP) feature.

⁽²²⁴⁾ DCLK frequency of 100 MHz using external CLKUSR.

⁽²²⁵⁾ Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.



Glossary

Table 2-68: Glossary





Term	Definition				
	Single-Ended WaveformVODPositive Channel (p) = VOHVCMNegative Channel (n) = VOLGroundGround				
	Differential Waveform V_{0D} V_{0D} V_{0D} V_{0D}				
f _{HSCLK}	Left and right PLL input clock frequency.				
f _{HSDR}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDR} = 1/TUI), non-DPA.				
f _{hsdrdpa}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDRDPA} = 1/TUI), DPA.				
J	High-speed I/O block—Deserialization factor (width of parallel data bus).				





Term	Definition
t _C	High-speed receiver and transmitter input and output clock period.
TCCS (channel-to- channel-skew)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t _{DUTY}	High-speed I/O block—Duty cycle on the high-speed transmitter output clock.
t _{FALL}	Signal high-to-low transition time (80-20%)
t _{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.
t _{OUTPJ_IO}	Period jitter on the general purpose I/O driven by a PLL.
t _{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL.
t _{RISE}	Signal low-to-high transition time (20-80%)
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = $1/(\text{receiver input clock frequency multiplication factor}) = t_C/w)$
V _{CM(DC)}	DC common mode input voltage.
V _{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.
V _{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
V _{DIF(AC)}	AC differential input voltage—Minimum AC input differential voltage required for switching.
V _{DIF(DC)}	DC differential input voltage— Minimum DC input differential voltage required for switching.
V _{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
V _{IH(AC)}	High-level AC input voltage
V _{IH(DC)}	High-level DC input voltage
V _{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
V _{IL(AC)}	Low-level AC input voltage
V _{IL(DC)}	Low-level DC input voltage

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