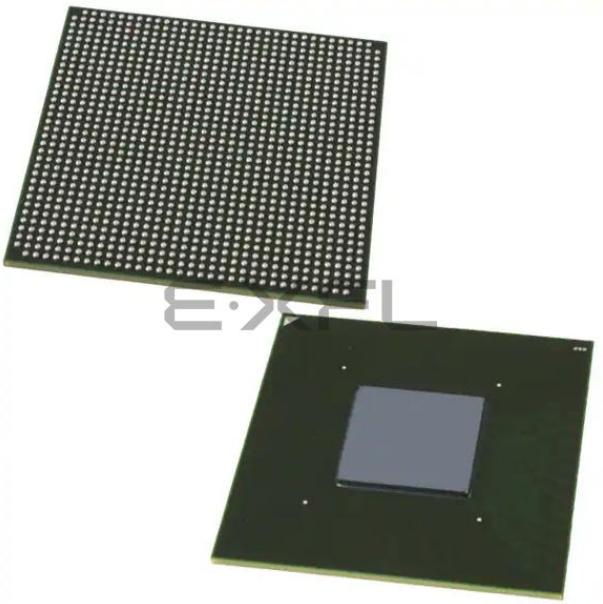


Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	11460
Number of Logic Elements/Cells	242000
Total RAM Bits	15470592
Number of I/O	544
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxfa7h6f35c6n

Contents

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Inter-transceiver block transmitter channel-to-channel skew[39]	×*N* PMA bonded mode	—	—	500	—	—	500	ps

Table 1-24: CMU PLL Specifications for Arria V GX and SX Devices

Symbol/Description	Transceiver Speed Grade 4		Transceiver Speed Grade 6		Unit
	Min	Max	Min	Max	
Supported data range	611	6553.6	611	3125	Mbps
fPLL supported data range	611	3125	611	3125	Mbps

Table 1-25: Transceiver-FPGA Fabric Interface Specifications for Arria V GX and SX Devices

Symbol/Description	Transceiver Speed Grade 4 and 6		Unit
	Min	Max	
Interface speed (single-width mode)	25	187.5	MHz
Interface speed (double-width mode)	25	163.84	MHz

Related Information

- **CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain** on page 1-35
- **CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain** on page 1-36
- **Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines**
  Provides more information about the power supply connection for different data rates.

[39] This specification is only applicable to channels on one side of the device across two transceiver banks.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Transmitter REFCLK phase noise(43)	10 Hz	—	—	–50	dBc/Hz
	100 Hz	—	—	–80	dBc/Hz
	1 KHz	—	—	–110	dBc/Hz
	10 KHz	—	—	–120	dBc/Hz
	100 KHz	—	—	–120	dBc/Hz
	≥ 1 MHz	—	—	–130	dBc/Hz
R_{REF}	—	—	2000 ±1%	—	Ω

Table 1-27: Transceiver Clocks Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
fixedclk clock frequency	PCIe Receiver Detect	—	125	—	MHz
Transceiver Reconfiguration Controller IP (mgmt_clk_clk) clock frequency	—	75	—	125	MHz

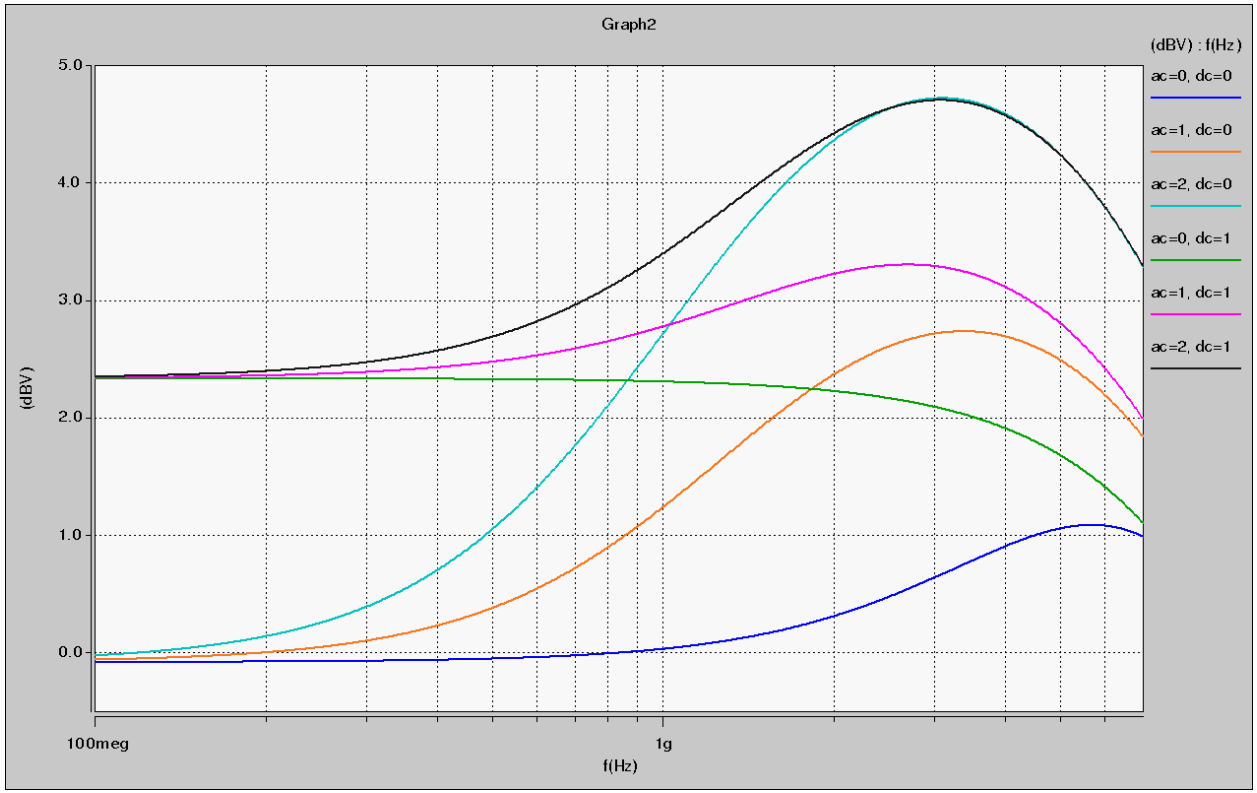
Table 1-28: Receiver Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS				
Data rate (6-Gbps transceiver)(44)	—	611	—	6553.6	Mbps

(43) The transmitter REFCLK phase jitter is 30 ps p-p (5 ps RMS) with bit error rate (BER) 10^{-12}, equivalent to 14 sigma.
(44) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain

Figure 1-2: Continuous Time-Linear Equalizer (CTLE) Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices



Symbol	V_{OD} Setting[58]	V_{OD} Value (mV)	V_{OD} Setting[58]	V_{OD} Value (mV)
	25	500	53	1060
	26	520	54	1080
	27	540	55	1100
	28	560	56	1120
	29	580	57	1140
	30	600	58	1160
	31	620	59	1180
	32	640	60	1200
	33	660		

Transmitter Pre-Emphasis Levels

The following table lists the simulation data on the transmitter pre-emphasis levels in dB for the first post tap under the following conditions:

- Low-frequency data pattern—five 1s and five 0s
- Data rate—2.5 Gbps

The levels listed are a representation of possible pre-emphasis levels under the specified conditions only and the pre-emphasis levels may change with data pattern and data rate.

Arria V devices only support 1st post tap pre-emphasis with the following conditions:

- The 1st post tap pre-emphasis settings must satisfy $|B| + |C| \leq 60$ where $|B| = V_{OD}$ setting with termination value, $R_{TERM} = 100\ \Omega$ and $|C|$ = 1st post tap pre-emphasis setting.
- $|B| - |C| > 5$ for data rates < 5 Gbps and $|B| - |C| > 8.25$ for data rates > 5 Gbps.
- $(V_{MAX}/V_{MIN} - 1)\% < 600\%$, where $V_{MAX} = |B| + |C|$ and $V_{MIN} = |B| - |C|$.

Exception for PCIe Gen2 design: V_{OD} setting = 43 and pre-emphasis setting = 19 are allowed for PCIe Gen2 design with transmit de-emphasis – 6dB setting (`pipe_txdeemp` = 1'b0) using Altera PCIe Hard IP and PIPE IP cores.

[58] Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

Quartus Prime 1st Post Tap Pre-Emphasis Setting	Quartus Prime V_{OD} Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
16	—	—	9.56	7.73	6.49	—	—	dB
17	—	—	10.43	8.39	7.02	—	—	dB
18	—	—	11.23	9.03	7.52	—	—	dB
19	—	—	12.18	9.7	8.02	—	—	dB
20	—	—	13.17	10.34	8.59	—	—	dB
21	—	—	14.2	11.1	—	—	—	dB
22	—	—	15.38	11.87	—	—	—	dB
23	—	—	—	12.67	—	—	—	dB
24	—	—	—	13.48	—	—	—	dB
25	—	—	—	14.37	—	—	—	dB
26	—	—	—	—	—	—	—	dB
27	—	—	—	—	—	—	—	dB
28	—	—	—	—	—	—	—	dB
29	—	—	—	—	—	—	—	dB
30	—	—	—	—	—	—	—	dB
31	—	—	—	—	—	—	—	dB

Related Information

SPICE Models for Altera Devices
Provides the Arria V HSSI HSPICE models.

Transceiver Compliance Specification

The following table lists the physical medium attachment (PMA) specification compliance of all supported protocol for Arria V GX, GT, SX, and ST devices. For more information about the protocol parameter details and compliance specifications, contact your Altera Sales Representative.

Protocol	Sub-protocol	Data Rate (Mbps)
SONET	SONET 155	155.52
	SONET 622	622.08
	SONET 2488	2,488.32
Gigabit-capable passive optical network (GPON)	GPON 155	155.52
	GPON 622	622.08
	GPON 1244	1,244.16
	GPON 2488	2,488.32
QSGMII	QSGMII 5000	5,000

Core Performance Specifications

Clock Tree Specifications

Table 1-35: Clock Tree Specifications for Arria V Devices

Parameter	Performance			Unit
	–I3, –C4	–I5, –C5	–C6	
Global clock and Regional clock	625	625	525	MHz
Peripheral clock	450	400	350	MHz

PLL Specifications

Table 1-36: PLL Specifications for Arria V Devices

This table lists the Arria V PLL block specifications. Arria V PLL block does not include HPS PLL.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{CASC\_OUTPJ\_DC}$ (67)(71)	Period jitter for dedicated clock output in cascaded PLLs	$F_{OUT} \geq 100$ MHz	—	—	175	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	17.5	mUI (p-p)
t_{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 µs	—	—	—	±10	%
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	8	24	32	bits
k_{VALUE}	Numerator of fraction	—	128	8388608	2147483648	—
f_{RES}	Resolution of VCO frequency	f_{INPFD} = 100 MHz	390625	5.96	0.023	Hz

Related Information

Memory Output Clock Jitter Specifications on page 1-57
Provides more information about the external memory interface clock output jitter specifications.

(71) The cascaded PLL specification is only applicable with the following conditions:
- Upstream PLL: 0.59 MHz ≤ Upstream PLL BW < 1 MHz
- Downstream PLL: Downstream PLL BW > 2 MHz

DSP Block Performance Specifications

Table 1-37: DSP Block Performance Specifications for Arria V Devices

Mode		Performance			Unit
		–I3, –C4	–I5, –C5	–C6	
Modes using One DSP Block	Independent 9 × 9 multiplication	370	310	220	MHz
	Independent 18 × 19 multiplication	370	310	220	MHz
	Independent 18 × 25 multiplication	370	310	220	MHz
	Independent 20 × 24 multiplication	370	310	220	MHz
	Independent 27 × 27 multiplication	310	250	200	MHz
	Two 18 × 19 multiplier adder mode	370	310	220	MHz
	18 × 18 multiplier added summed with 36-bit input	370	310	220	MHz
Modes using Two DSP Blocks	Complex 18 × 19 multiplication	370	310	220	MHz

Memory Block Performance Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to 50% output duty cycle. Use the Quartus Prime software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX}.

Symbol		Condition	–I3, –C4			–I5, –C5			–C6			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	TCCS	True Differential I/O Standards	—	—	150	—	—	150	—	—	150	ps
		Emulated Differential I/O Standards	—	—	300	—	—	300	—	—	300	ps
Receiver	True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J =3 to 10(76)	150	—	1250	150	—	1250	150	—	1050	Mbps
		SERDES factor J ≥ 8 with DPA(76)(78)	150	—	1600	150	—	1500	150	—	1250	Mbps
	f_{HSDR} (data rate)	SERDES factor J = 3 to 10	(77)	—	(83)	(77)	—	(83)	(77)	—	(83)	Mbps
		SERDES factor J = 1 to 2, uses DDR registers	(77)	—	(79)	(77)	—	(79)	(77)	—	(79)	Mbps
DPA Mode	DPA run length	—	—	—	10000	—	—	10000	—	—	10000	UI
Soft-CDR Mode	Soft-CDR ppm tolerance	—	—	—	300	—	—	300	—	—	300	±ppm
Non-DPA Mode	Sampling Window	—	—	—	300	—	—	300	—	—	300	ps

(83) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

DPA Lock Time Specifications

Figure 1-4: Dynamic Phase Alignment (DPA) Lock Time Specifications with DPA PLL Calibration Enabled

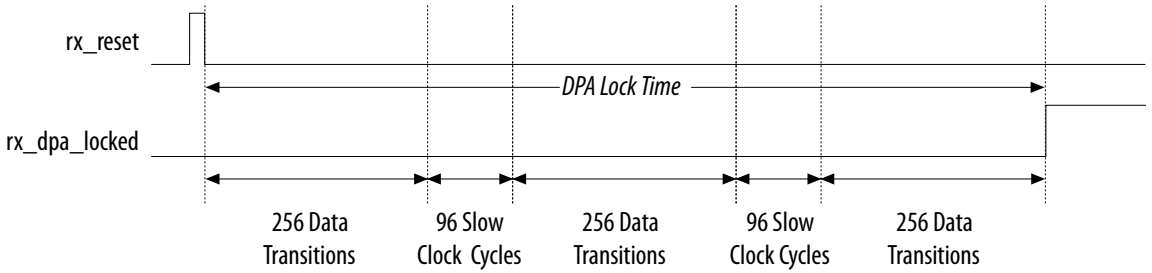


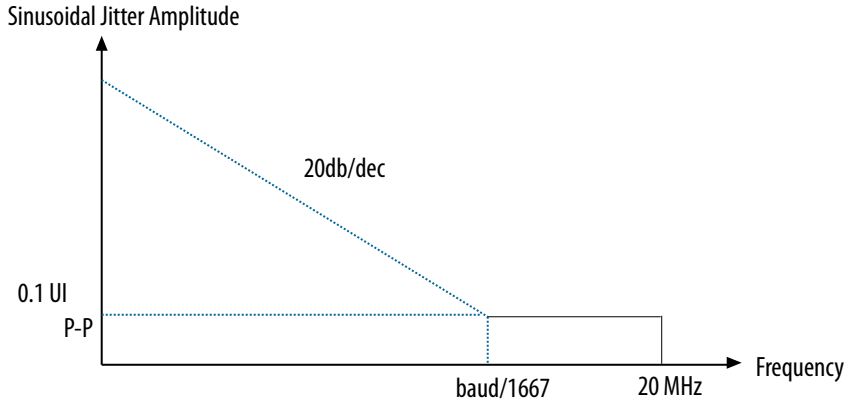
Table 1-41: DPA Lock Time Specifications for Arria V Devices

The specifications are applicable to both commercial and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions(84)	Maximum Data Transition
SPI-4	00000000001111111111	2	128	640
Parallel Rapid I/O	00001111	2	128	640
	10010000	4	64	640
Miscellaneous	10101010	8	32	640
	01010101	8	32	640

(84) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 1-6: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Less than 1.25 Gbps



DLL Frequency Range Specifications

Table 1-43: DLL Frequency Range Specifications for Arria V Devices

Parameter	–I3, –C4	–I5, –C5	–C6	Unit
DLL operating frequency range	200 – 667	200 – 667	200 – 667	MHz

DQS Logic Block Specifications

Table 1-44: DQS Phase Shift Error Specifications for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria V Devices

This error specification is the absolute maximum and minimum error.

Number of DQS Delay Buffer	–I3, –C4	–I5, –C5	–C6	Unit
2	40	80	80	ps

HPS Clock Performance

Table 1-48: HPS Clock Performance for Arria V Devices

Symbol/Description	–I3	–C4	–C5, –I5	–C6	Unit
mpu_base_clk (microprocessor unit clock)	1050	925	800	700	MHz
main_base_clk (L3/L4 interconnect clock)	400	400	400	350	MHz
h2f_user0_clk	100	100	100	100	MHz
h2f_user1_clk	100	100	100	100	MHz
h2f_user2_clk	200	200	200	160	MHz

HPS PLL Specifications

HPS PLL VCO Frequency Range

Table 1-49: HPS PLL VCO Frequency Range for Arria V Devices

Description	Speed Grade	Minimum	Maximum	Unit
VCO range	–C5, –I5, –C6	320	1,600	MHz
	–C4	320	1,850	MHz
	–I3	320	2,100	MHz

HPS PLL Input Clock Range

The HPS PLL input clock range is 10 – 50 MHz. This clock range applies to both HPS_CLK1 and HPS_CLK2 inputs.

Related Information

Clock Select, Booting and Configuration chapter
Provides more information about the clock range for different values of clock select (CSEL).

FPP Configuration Timing

DCLK-to-DATA[] Ratio (r) for FPP Configuration

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is *r* times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP ×16 where the *r* is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

Table 1-65: DCLK-to-DATA[] Ratio for Arria V Devices

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
FPP (8-bit wide)	Off	Off	1
	On	Off	1
	Off	On	2
	On	On	2
FPP (16-bit wide)	Off	Off	1
	On	Off	2
	Off	On	4
	On	On	4

FPP Configuration Timing when DCLK-to-DATA[] = 1

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8 and FPP ×16. For the respective DCLK-to-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Arria V Devices table.

Table 1-66: FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Arria V Devices

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs

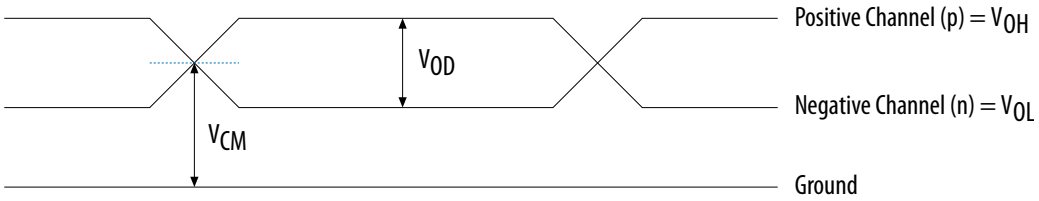
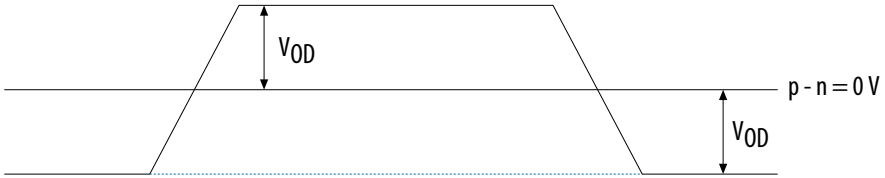
Symbol	Parameter	Minimum	Maximum	Unit
t_{STATUS}	nSTATUS low pulse width	268	1506(94)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506(95)	µs
t_{CF2CK}(96)	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}(96)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/ ×16)	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode(97)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4× maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} × CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

FPP Configuration Timing

Provides the FPP configuration timing waveforms.

(94) You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.
(95) You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.
(96) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.
(97) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Term	Definition
	Transmitter Output Waveforms **Single-Ended Waveform**  **Differential Waveform** 
f_{HSCLK}	Left/right PLL input clock frequency.
f_{HSDR}	High-speed I/O block—Maximum/minimum LVDS data transfer rate (f_{HSDR} =1/TUI), non-DPA.
$f_{HSDRDPA}$	High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ =1/TUI), DPA.
J	High-speed I/O block—Deserialization factor (width of parallel data bus).

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle.

For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

Table 2-4: Maximum Allowed Overshoot During Transitions for Arria V GZ Devices

Symbol	Description	Condition (V)	Overshoot Duration as % @ T_J = 100°C	Unit
Vi (AC)	AC input voltage	3.8	100	%
		3.85	64	%
		3.9	36	%
		3.95	21	%
		4	12	%
		4.05	7	%
		4.1	4	%
		4.15	2	%
		4.2	1	%

Recommended Operating Conditions

Table 2-5: Recommended Operating Conditions for Arria V GZ Devices

Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum(114)	Typical	Maximum (114)	Unit
V_{CC}	Core voltage and periphery circuitry power supply (115)	—	0.82	0.85	0.88	V

(114) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(115) The V_{CC} core supply must be set to 0.9 V if the Partial Reconfiguration (PR) feature is used.

Transceiver Power Supply Requirements

Table 2-7: Transceiver Power Supply Voltage Requirements for Arria V GZ Devices

Conditions	VCCR_GXB and VCCT_GXB (122)	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true: • Data rate > 10.3 Gbps. • DFE is used.	1.05	3.0	1.5	V
If ANY of the following conditions are true (123) : • ATX PLL is used. • Data rate > 6.5Gbps. • DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used.	1.0			
If ALL of the following conditions are true: • ATX PLL is not used. • Data rate ≤ 6.5Gbps. • DFE, AEQ, and EyeQ are not used.	0.85	2.5		

DC Characteristics

Supply Current

Standby current is the current drawn from the respective power rails used for power budgeting.

Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

(122) If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to 0.85 V, they can be shared with the VCC core supply.

(123) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

Hot Socketing

Table 2-14: Hot Socketing Specifications for Arria V GZ Devices

Symbol	Description	Maximum
$I_{IOPIN\ (DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN\ (AC)}$	AC current per I/O pin	8 mA (124)
$I_{XCVR\text{-}TX\ (DC)}$	DC current per transceiver transmitter pin	100 mA
$I_{XCVR\text{-}RX\ (DC)}$	DC current per transceiver receiver pin	50 mA

Internal Weak Pull-Up Resistor

Table 2-15: Internal Weak Pull-Up Resistor for Arria V GZ Devices

All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins. The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ .

Symbol	Description	V_{CCIO} Conditions (V) (125)	Value (126)	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option.	3.0 ±5%	25	k Ω
		2.5 ±5%	25	k Ω
		1.8 ±5%	25	k Ω
		1.5 ±5%	25	kΩ
		1.35 ±5%	25	k Ω
		1.25 ±5%	25	k Ω
		1.2 ±5%	25	k Ω

(124) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C\ dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.
(125) The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
(126) These specifications are valid with a ±10% tolerance to cover changes over PVT.

Related Information

- **Configuration, Design Security, and Remote System Upgrades in Arria V Devices**
  For more information about the reconfiguration input for the ALTREMOTE_UPDATE IP core, refer to the "User Watchdog Timer" section.
- **Configuration, Design Security, and Remote System Upgrades in Arria V Devices**
  For more information about the `reset_timer` input for the ALTREMOTE_UPDATE IP core, refer to the "Remote System Upgrade State Machine" section.

User Watchdog Internal Oscillator Frequency Specification

Table 2-65: User Watchdog Internal Oscillator Frequency Specifications

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

Arria V Devices Documentation page
For the Excel-based I/O Timing spreadsheet

(226) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification. For more information, refer to the "Remote System Upgrade State Machine" section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

(227) This is equivalent to strobing the reset_timer input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification. For more information, refer to the "User Watchdog Timer" section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.