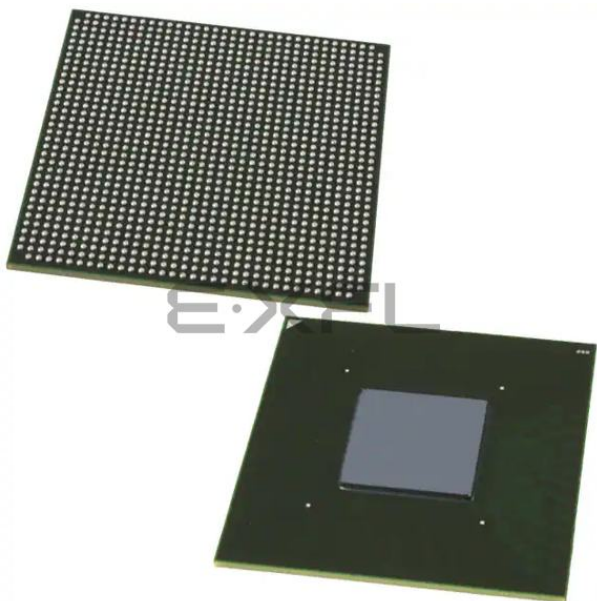




Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	14151
Number of Logic Elements/Cells	300000
Total RAM Bits	17358848
Number of I/O	544
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxfb1h4f35c4n

Operating Conditions	2-1
Switching Characteristics	2-21
Transceiver Performance Specifications	2-21
Core Performance Specifications	2-37
Periphery Performance	2-44
Configuration Specification	2-56
POR Specifications	2-56
JTAG Configuration Specifications	2-57
Fast Passive Parallel (FPP) Configuration Timing	2-57
Active Serial Configuration Timing	2-65
Passive Serial Configuration Timing	2-67
Initialization	2-69
Configuration Files	2-69
Remote System Upgrades Circuitry Timing Specification	2-70
User Watchdog Internal Oscillator Frequency Specification	2-71
I/O Timing	2-71
Programmable IOE Delay	2-72
Programmable Output Buffer Delay	2-72
Glossary	2-73
Document Revision History	2-78

Symbol	Description	Condition	Minimum ⁽¹⁾	Typical	Maximum ⁽¹⁾	Unit
V _{CCIO}	I/O buffers power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	1.283	1.35	1.418	V
		1.25 V	1.19	1.25	1.31	V
		1.2 V	1.14	1.2	1.26	V
V _{CCD_FPLL}	PLL digital voltage regulator power supply	—	1.425	1.5	1.575	V
V _{CCA_FPLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V _I	DC input voltage	—	−0.5	—	3.6	V
V _O	Output voltage	—	0	—	V _{CCIO}	V
T _J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	−40	—	100	°C
t _{RAMP} ⁽⁴⁾	Power supply ramp time	Standard POR	200 μs	—	100 ms	—
		Fast POR	200 μs	—	4 ms	—

⁽¹⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁴⁾ This is also applicable to HPS power supply. For HPS power supply, refer to t_{RAMP} specifications for standard POR when HPS_PORSEL = 0 and t_{RAMP} specifications for fast POR when HPS_PORSEL = 1.

Symbol	Description	V _{CCIO} (V)	Value	Unit
dR/dT	OCT variation with temperature without recalibration	3.0	0.189	%/°C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.35	0.200	
		1.25	0.200	
		1.2	0.317	

Pin Capacitance

Table 1-11: Pin Capacitance for Arria V Devices

Symbol	Description	Maximum	Unit
C _{IOTB}	Input capacitance on top/bottom I/O pins	6	pF
C _{IOLR}	Input capacitance on left/right I/O pins	6	pF
C _{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins	6	pF
C _{IOVREF}	Input capacitance on V _{REF} pins	48	pF

Hot Socketing

Table 1-12: Hot Socketing Specifications for Arria V Devices

Symbol	Description	Maximum	Unit
I _{IOPIN} (DC)	DC current per I/O pin	300	μA
I _{IOPIN} (AC)	AC current per I/O pin	8 ⁽¹⁰⁾	mA
I _{XCVR-TX} (DC)	DC current per transceiver transmitter (TX) pin	100	mA

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 1-15: Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-15 Class I, II	1.425	1.5	1.575	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
SSTL-135 Class I, II	1.283	1.35	1.418	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
SSTL-125 Class I, II	1.19	1.25	1.26	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	$V_{CCIO}/2$	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	$V_{CCIO}/2$	—
HSTL-12 Class I, II	1.14	1.2	1.26	$0.47 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.53 \times V_{CCIO}$	—	$V_{CCIO}/2$	—
HSUL-12	1.14	1.2	1.3	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	—	—	—

Transceiver Specifications for Arria V GT and ST Devices

Table 1-26: Reference Clock Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O standards	1.2 V PCML, 1.4 VPCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL ⁽⁴⁰⁾ , HCSL, and LVDS				
Input frequency from REFCLK input pins	—	27	—	710	MHz
Rise time	Measure at ±60 mV of differential signal ⁽⁴¹⁾	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal ⁽⁴¹⁾	—	—	400	ps
Duty cycle	—	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	300 ⁽⁴²⁾ /2000	mV
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	Ω
V _{ICM} (AC coupled)	—	—	1.2	—	V
V _{ICM} (DC coupled)	HCSL I/O standard for the PCIe reference clock	250	—	550	mV

⁽⁴⁰⁾ Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.⁽⁴¹⁾ REFCLK performance requires to meet transmitter REFCLK phase noise specification.⁽⁴²⁾ The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Data rate (10-Gbps transceiver) ⁽⁴⁴⁾	—	0.611	—	10.3125	Gbps
Absolute V_{MAX} for a receiver pin ⁽⁴⁵⁾	—	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	—	—	—	2.2	V
Minimum differential eye opening at the receiver serial input pins ⁽⁴⁶⁾	—	100	—	—	mV
V_{ICM} (AC coupled)	—	—	750 ⁽⁴⁷⁾ /800	—	mV
V_{ICM} (DC coupled)	$\leq 3.2\text{Gbps}$ ⁽⁴⁸⁾	670	700	730	mV
Differential on-chip termination resistors	85- Ω setting	85			Ω
	100- Ω setting	100			Ω
	120- Ω setting	120			Ω
	150- Ω setting	150			Ω
t_{LTR} ⁽⁴⁹⁾	—	—	—	10	μs
t_{LTD} ⁽⁵⁰⁾	—	4	—	—	μs

⁽⁴⁵⁾ The device cannot tolerate prolonged operation at this absolute maximum.

⁽⁴⁶⁾ The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

⁽⁴⁷⁾ The AC coupled V_{ICM} is 750 mV for PCIe mode only.

⁽⁴⁸⁾ For standard protocol compliance, use AC coupling.

⁽⁴⁹⁾ t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

⁽⁵⁰⁾ t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedto data signal goes high.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{\text{CASC_OUTPJ_DC}}^{(67)(71)}$	Period jitter for dedicated clock output in cascaded PLLs	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	175	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	17.5	mUI (p-p)
t_{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 μs	—	—	—	± 10	%
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	8	24	32	bits
k_{VALUE}	Numerator of fraction	—	128	8388608	2147483648	—
f_{RES}	Resolution of VCO frequency	$f_{\text{INPFD}} = 100 \text{ MHz}$	390625	5.96	0.023	Hz

Related Information

[Memory Output Clock Jitter Specifications](#) on page 1-57

Provides more information about the external memory interface clock output jitter specifications.

⁽⁷¹⁾ The cascaded PLL specification is only applicable with the following conditions:

- Upstream PLL: $0.59 \text{ MHz} \leq \text{Upstream PLL BW} < 1 \text{ MHz}$
- Downstream PLL: $\text{Downstream PLL BW} > 2 \text{ MHz}$

HPS Clock Performance

Table 1-48: HPS Clock Performance for Arria V Devices

Symbol/Description	–I3	–C4	–C5, –I5	–C6	Unit
mpu_base_clk (microprocessor unit clock)	1050	925	800	700	MHz
main_base_clk (L3/L4 interconnect clock)	400	400	400	350	MHz
h2f_user0_clk	100	100	100	100	MHz
h2f_user1_clk	100	100	100	100	MHz
h2f_user2_clk	200	200	200	160	MHz

HPS PLL Specifications

HPS PLL VCO Frequency Range

Table 1-49: HPS PLL VCO Frequency Range for Arria V Devices

Description	Speed Grade	Minimum	Maximum	Unit
VCO range	–C5, –I5, –C6	320	1,600	MHz
	–C4	320	1,850	MHz
	–I3	320	2,100	MHz

HPS PLL Input Clock Range

The HPS PLL input clock range is 10 – 50 MHz. This clock range applies to both HPS_CLK1 and HPS_CLK2 inputs.

Related Information

[Clock Select, Booting and Configuration chapter](#)

Provides more information about the clock range for different values of clock select (CSEL).

After the Boot ROM code exits and control is passed to the preloader, software can adjust the value of `drvsel` and `smp1sel` via the system manager. `drvsel` can be set from 1 to 7 and `smp1sel` can be set from 0 to 7. While the preloader is executing, the values for `SDMMC_CLK` and `SDMMC_CLK_OUT` increase to a maximum of 200 MHz and 50 MHz respectively.

The SD/MMC interface calibration support will be available in a future release of the preloader through the SoC EDS software update.

Symbol	Description	Min	Max	Unit
$T_{\text{sdmmc_clk}}$ (internal reference clock)	SDMMC_CLK clock period (Identification mode)	20	—	ns
	SDMMC_CLK clock period (Default speed mode)	5	—	ns
	SDMMC_CLK clock period (High speed mode)	5	—	ns
$T_{\text{sdmmc_clk_out}}$ (interface output clock)	SDMMC_CLK_OUT clock period (Identification mode)	2500	—	ns
	SDMMC_CLK_OUT clock period (Default speed mode)	40	—	ns
	SDMMC_CLK_OUT clock period (High speed mode)	20	—	ns
$T_{\text{duty cycle}}$	SDMMC_CLK_OUT duty cycle	45	55	%
T_d	SDMMC_CMD/SDMMC_D output delay	$(T_{\text{sdmmc_clk}} \times \text{drvsel})/2 - 1.23^{(87)}$	$(T_{\text{sdmmc_clk}} \times \text{drvsel})/2 + 1.69^{(87)}$	ns
T_{su}	Input setup time	$1.05 - (T_{\text{sdmmc_clk}} \times \text{smp1sel})/2^{(88)}$	—	ns
T_h	Input hold time	$(T_{\text{sdmmc_clk}} \times \text{smp1sel})/2^{(88)}$	—	ns

⁽⁸⁷⁾ `drvsel` is the drive clock phase shift select value.

⁽⁸⁸⁾ `smp1sel` is the sample clock phase shift select value.

Symbol	Parameter	Minimum	Maximum	Unit
$t_{CF2CK}^{(105)}$	nCONFIG high to first rising edge on DCLK	1506	—	μs
$t_{ST2CK}^{(105)}$	nSTATUS high to first rising edge of DCLK	2	—	μs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode ⁽¹⁰⁶⁾	175	437	μs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times \text{CLKUSR period})$	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information**PS Configuration Timing**

Provides the PS configuration timing waveform.

⁽¹⁰⁵⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

⁽¹⁰⁶⁾ The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)
Arria V GX	A1	71,015,712	439,960
	A3	71,015,712	439,960
	A5	101,740,800	446,360
	A7	101,740,800	446,360
	B1	137,785,088	457,368
	B3	137,785,088	457,368
	B5	185,915,808	463,128
	B7	185,915,808	463,128
Arria V GT	C3	71,015,712	439,960
	C7	101,740,800	446,360
	D3	137,785,088	457,368
	D7	185,915,808	463,128
Arria V SX	B3	185,903,680	450,968
	B5	185,903,680	450,968
Arria V ST	D3	185,903,680	450,968
	D5	185,903,680	450,968

Minimum Configuration Time Estimation

Table 1-73: Minimum Configuration Time Estimation for Arria V Devices

The estimated values are based on the configuration .rbf sizes in Uncompressed .rbf Sizes for Arria V Devices table.

Date	Version	Changes
November 2012	3.0	- Updated Table 2, Table 4, Table 9, Table 14, Table 16, Table 17, Table 20, Table 21, Table 25, Table 29, Table 36, Table 56, Table 57, and Table 60. - Removed table: Transceiver Block Jitter Specifications for Arria V Devices. - Added HPS information: - Added “HPS Specifications” section. - Added Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, and Table 50. - Added Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19. - Updated Table 3 and Table 5.
October 2012	2.4	- Updated Arria V GX $V_{CCR_GXBL/R}$, $V_{CCT_GXBL/R}$, and $V_{CCL_GXBL/R}$ minimum and maximum values, and data rate in Table 4. - Added receiver V_{ICM} (AC coupled) and V_{ICM} (DC coupled) values, and transmitter V_{OCM} (AC coupled) and V_{OCM} (DC coupled) values in Table 20 and Table 21.
August 2012	2.3	Updated the SERDES factor condition in Table 30.
July 2012	2.2	- Updated the maximum voltage for V_I (DC input voltage) in Table 1. - Updated Table 20 to include the Arria V GX -I3 speed grade. - Updated the minimum value of the fixedclk clock frequency in Table 20 and Table 21. - Updated the SERDES factor condition in Table 30. - Updated Table 50 to include the IOE programmable delay settings for the Arria V GX -I3 speed grade.
June 2012	2.1	Updated $V_{CCR_GXBL/R}$, $V_{CCT_GXBL/R}$, and $V_{CCL_GXBL/R}$ values in Table 4.

I/O Standard Specifications

The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL} , respectively.

Table 2-16: Single-Ended I/O Standards for Arria V GZ Devices

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVC MOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	0.45	$V_{CCIO} - 0.45$	2	-2
1.5 V	1.425	1.5	1.575	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
1.2 V	1.14	1.2	1.26	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2

Table 2-17: Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V GZ Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-15 Class I, II	1.425	1.5	1.575	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$

I/O Standard	V_{CCIO} (V) ⁽¹²⁸⁾			V_{ID} (mV) ⁽¹²⁹⁾			$V_{ICM(DC)}$ (V)			V_{OD} (V) ⁽¹³⁰⁾			V_{OCM} (V) ⁽¹³⁰⁾		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
RSDS (HIO) ⁽¹³³⁾	2.375	2.5	2.625	100	$V_{CM} = 1.25$ V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO) ⁽¹³⁴⁾	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	1	1.2	1.4
LVPECL ^{(135), (136)}	—	—	—	300	—	—	0.6	$D_{MAX} \leq 700$ Mbps	1.8	—	—	—	—	—	—
	—	—	—	300	—	—	1	$D_{MAX} > 700$ Mbps	1.6	—	—	—	—	—	—

Related Information[Glossary](#) on page 2-73⁽¹²⁸⁾ Differential inputs are powered by VCCPD which requires 2.5 V.⁽¹²⁹⁾ The minimum VID value is applicable over the entire common mode range, VCM.⁽¹³⁰⁾ RL range: $90 \leq RL \leq 110 \Omega$.⁽¹³³⁾ For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.⁽¹³⁴⁾ For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.⁽¹³⁵⁾ LVPECL is only supported on dedicated clock input pins.⁽¹³⁶⁾ For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

Core Performance Specifications

Clock Tree Specifications

Table 2-33: Clock Tree Performance for Arria V GZ Devices

Symbol	Performance		Unit
	C3, I3L	C4, I4	
Global and Regional Clock	650	580	MHz
Periphery Clock	500	500	MHz

PLL Specifications

Table 2-34: PLL Specifications for Arria V GZ Devices

Symbol	Parameter	Min	Typ	Max	Unit
$f_{IN}^{(167)}$	Input clock frequency (C3, I3L speed grade)	5	—	800	MHz
	Input clock frequency (C4, I4 speed grade)	5	—	650	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{FINPFD}	Fractional Input clock frequency to the PFD	50	—	160	MHz
$f_{VCO}^{(168)}$	PLL VCO operating range (C3, I3L speed grade)	600	—	1600	MHz
	PLL VCO operating range (C4, I4 speed grade)	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%

⁽¹⁶⁷⁾ This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

⁽¹⁶⁸⁾ The VCO frequency reported by the Quartus II software in the **PLL Usage Summary** section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
$t_{x \text{ Jitter}}$ - True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	UI
$t_{x \text{ Jitter}}$ - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	300	—	—	325	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.2	—	—	0.25	UI
t_{DUTY}	Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	%
$t_{\text{RISE}} \& t_{\text{FALL}}$	True Differential I/O Standards	—	—	200	—	—	200	ps
	Emulated Differential I/O Standards with three external output resistor networks	—	—	250	—	—	300	ps
TCCS	True Differential I/O Standards	—	—	150	—	—	150	ps
	Emulated Differential I/O Standards	—	—	300	—	—	300	ps

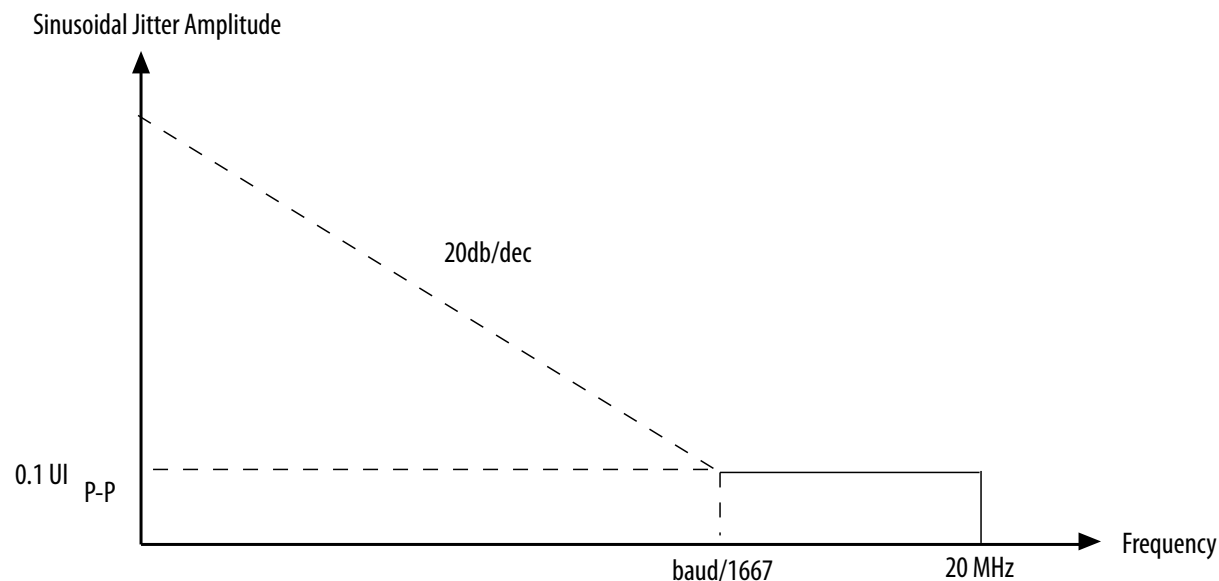
Receiver High-Speed I/O Specifications

Table 2-41: Receiver High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Figure 2-5: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate < 1.25 Gbps



Non DPA Mode High-Speed I/O Specifications

Table 2-46: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

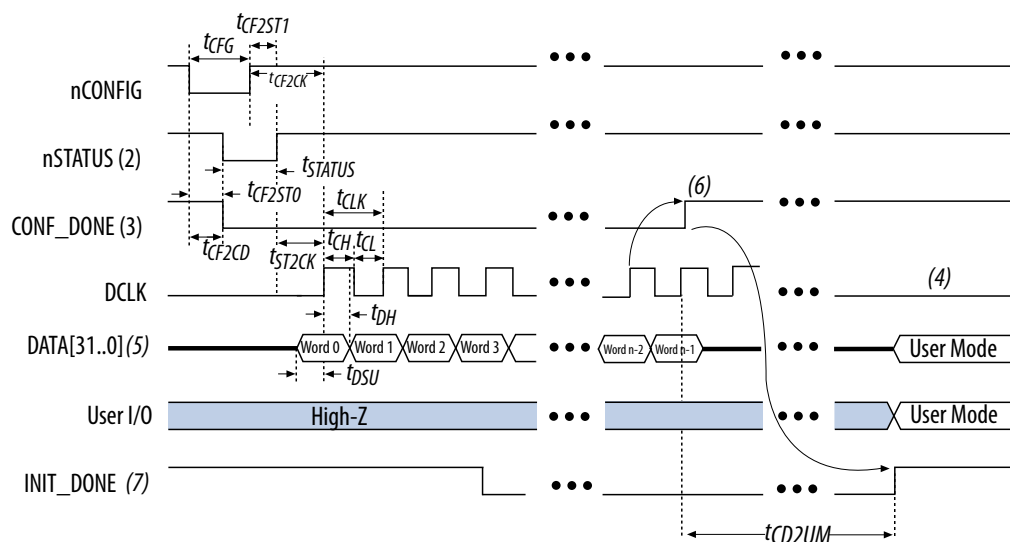
When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Sampling Window	—	—	—	300	—	—	300	ps

FPP Configuration Timing when DCLK to DATA[] = 1

Figure 2-7: FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1

Timing waveform for FPP configuration when using a MAX[®] II or MAX V device as an external host.



Notes:

1. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
2. After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.
3. After power-up, before and during configuration, CONF_DONE is low.
4. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
5. For FPP $\times 16$, use DATA[15..0]. For FPP $\times 8$, use DATA[7..0]. DATA[31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high when the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
7. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 2-60: PS Timing Parameters for Arria V GZ Devices

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	μ s
t_{STATUS}	nSTATUS low pulse width	268	1,506 ⁽²¹⁷⁾	μ s
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽²¹⁸⁾	μ s
t_{CF2CK} (219)	nCONFIG high to first rising edge on DCLK	1,506	—	μ s
t_{ST2CK} ⁽²¹⁹⁾	nSTATUS high to first rising edge of DCLK	2	—	μ s
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode ⁽²²⁰⁾	175	437	μ s
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times$ maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (8576 \times \text{CLKUSR period})$ ⁽²²¹⁾	—	—

⁽²¹⁷⁾ This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

⁽²¹⁸⁾ This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

⁽²¹⁹⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

⁽²²⁰⁾ The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

Table 2-62: Uncompressed .rbf Sizes for Arria V GZ Devices

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ⁽²²³⁾
Arria V GZ	E1	137,598,880	562,208
	E3	137,598,880	562,208
	E5	213,798,880	561,760
	E7	213,798,880	561,760

Table 2-63: Minimum Configuration Time Estimation for Arria V GZ Devices

Variant	Member Code	Active Serial ⁽²²⁴⁾			Fast Passive Parallel ⁽²²⁵⁾		
		Width	DCLK (MHz)	Min Config Time (ms)	Width	DCLK (MHz)	Min Config Time (ms)
Arria V GZ	E1	4	100	344	32	100	43
	E3	4	100	344	32	100	43
	E5	4	100	534	32	100	67
	E7	4	100	534	32	100	67

Remote System Upgrades Circuitry Timing Specification

Table 2-64: Remote System Upgrade Circuitry Timing Specifications

Parameter	Minimum	Maximum	Unit
$t_{RU_nCONFIG}$ ⁽²²⁶⁾	250	—	ns
$t_{RU_nRSTIMER}$ ⁽²²⁷⁾	250	—	ns

⁽²²³⁾ The IOCSR .rbf size is specifically for the Configuration via Protocol (CvP) feature.

⁽²²⁴⁾ DCLK frequency of 100 MHz using external CLKUSR.

⁽²²⁵⁾ Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.