Intel - 5AGXFB1H4F35I3N Datasheet





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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	14151
Number of Logic Elements/Cells	300000
Total RAM Bits	17358848
Number of I/O	544
Number of Gates	· .
Voltage - Supply	1.12V ~ 1.18V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxfb1h4f35i3n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1-1: Absolute Maximum Ratings for Arria V Devices

Symbol	Description	Minimum	Maximum	Unit
V _{CC}	Core voltage power supply	-0.50	1.43	V
V _{CCP}	Periphery circuitry, PCIe [®] hardIP block, and transceiver physical coding sublayer (PCS) power supply	-0.50	1.43	V
V _{CCPGM}	Configuration pins power supply	-0.50	3.90	V
V _{CC_AUX}	Auxiliary supply	-0.50	3.25	V
V _{CCBAT}	Battery back-up power supply for design security volatile key register	-0.50	3.90	V
V _{CCPD}	I/O pre-driver power supply	-0.50	3.90	V
V _{CCIO}	I/O power supply	-0.50	3.90	V
V _{CCD_FPLL}	Phase-locked loop (PLL) digital power supply	-0.50	1.80	V
V _{CCA_FPLL}	PLL analog power supply	-0.50	3.25	V
V _{CCA_GXB}	Transceiver high voltage power	-0.50	3.25	V
V _{CCH_GXB}	Transmitter output buffer power	-0.50	1.80	V
V _{CCR_GXB}	Receiver power	-0.50	1.50	V
V _{CCT_GXB}	Transmitter power	-0.50	1.50	V
V _{CCL_GXB}	Transceiver clock network power	-0.50	1.50	V
VI	DC input voltage	-0.50	3.80	V
V _{CC_HPS}	HPS core voltage and periphery circuitry power supply	-0.50	1.43	V
V _{CCPD_HPS}	HPS I/O pre-driver power supply	-0.50	3.90	V
V _{CCIO_HPS}	HPS I/O power supply	-0.50	3.90	V
V _{CCRSTCLK_HPS}	HPS reset and clock input pins power supply	-0.50	3.90	V



Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

1/O Standard	V _{IL(DC)} (V)		V _{IH(DC)} (V)		V _{IL(AC)} (V)	V _{IH(AC)} (V)	V _{OL} (V)	V _{OH} (V)	I _{OL} ⁽¹⁴⁾	(14)(mA)
	Min	Мах	Min	Мах	Max	Min	Мах	Min	(mA)	IOH. (IIIIM)
SSTL-2 Class I	-0.3	V _{REF} - 0.15	V _{REF} + 0.15	$V_{CCIO} + 0.3$	V _{REF} - 0.31	V _{REF} + 0.31	V _{TT} – 0.608	V _{TT} + 0.608	8.1	-8.1
SSTL-2 Class II	-0.3	V _{REF} – 0.15	V _{REF} + 0.15	$V_{CCIO} + 0.3$	V _{REF} – 0.31	V _{REF} + 0.31	V _{TT} – 0.81	V _{TT} + 0.81	16.2	-16.2
SSTL-18 Class I	-0.3	V _{REF} - 0.125	V _{REF} + 0.125	$V_{CCIO} + 0.3$	V _{REF} – 0.25	V _{REF} + 0.25	V _{TT} – 0.603	V _{TT} + 0.603	6.7	-6.7
SSTL-18 Class II	-0.3	V _{REF} – 0.125	V _{REF} + 0.125	$V_{CCIO} + 0.3$	V _{REF} – 0.25	V _{REF} + 0.25	0.28	V _{CCIO} – 0.28	13.4	-13.4
SSTL-15 Class I	_	V _{REF} – 0.1	$V_{REF} + 0.1$	_	V _{REF} - 0.175	V _{REF} + 0.175	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	8	-8
SSTL-15 Class II	—	V _{REF} – 0.1	$V_{REF} + 0.1$	—	V _{REF} - 0.175	V _{REF} + 0.175	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	16	-16
SSTL-135	—	V _{REF} - 0.09	$V_{REF} + 0.09$	_	V _{REF} - 0.16	$V_{REF} + 0.16$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$		
SSTL-125	—	V _{REF} - 0.85	$V_{REF} + 0.85$	—	V _{REF} – 0.15	$V_{REF} + 0.15$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$		
HSTL-18 Class I	—	V _{REF} – 0.1	V _{REF} + 0.1	—	V _{REF} – 0.2	V _{REF} + 0.2	0.4	V _{CCIO} – 0.4	8	-8
HSTL-18 Class II		V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} – 0.2	$V_{REF} + 0.2$	0.4	V _{CCIO} – 0.4	16	-16
HSTL-15 Class I	_	V _{REF} – 0.1	$V_{REF} + 0.1$		V _{REF} – 0.2	V _{REF} + 0.2	0.4	$V_{CCIO} - 0.4$	8	-8



⁽¹⁴⁾ To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

1/O Standard	V _{IL(DC)} (V)		V _{IH(DC)} (V)		V _{IL(AC)} (V)	V _{IH(AC)} (V)	V _{OL} (V)	V _{OH} (V)	I _{OL} ⁽¹⁴⁾	I_{a} (mA)
	Min	Max	Min	Мах	Max	Min	Мах	Min	(mA)	
HSTL-15 Class II	—	V _{REF} – 0.1	$V_{REF} + 0.1$	_	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	V _{CCIO} – 0.4	16	-16
HSTL-12 Class I	-0.15	V _{REF} – 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	V _{REF} – 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	16	-16
HSUL-12	_	V _{REF} – 0.13	$V_{REF} + 0.13$	_	V _{REF} - 0.22	V _{REF} + 0.22	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	_	_

Differential SSTL I/O Standards

Table 1-17: Differential SSTL I/O Standards for Arria V Devices

I/O Standard	V _{CCIO} (V)		V _{SWING(DC)} (V)		V _{X(AC)} (V)			V _{SWING(AC)} (V)		
	Min	Тур	Max	Min	Мах	Min	Тур	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V _{CCIO} + 0.6	V _{CCIO} /2 – 0.2	—	V _{CCIO} /2 + 0.2	0.62	$V_{CCIO} + 0.6$
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V _{CCIO} + 0.6	V _{CCIO} /2 – 0.175	—	V _{CCIO} /2 + 0.175	0.5	$V_{CCIO} + 0.6$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(15)	V _{CCIO} /2 – 0.15	—	V _{CCIO} /2 + 0.15	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$
SSTL-135	1.283	1.35	1.45	0.18	(15)	V _{CCIO} /2 – 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} – V _{REF})	$2(V_{IL(AC)} - V_{REF})$

⁽¹⁴⁾ To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.



 $^{^{(15)}}$ The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

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Symbol/Description	Condition	Transc	eiver Speed G	irade 4	Transc	Unit		
Symbol/Description		Min	Тур	Max	Min	Тур	Max	onit
Run length	—	—	_	200	—		200	UI
Programmable equaliza- tion AC and DC gain	AC gain setting = 0 to $3^{(38)}$ DC gain setting = 0 to 1	Refer to C Gain and Response G	TLE Respons DC Gain for at Data Rates ain for Arria	e at Data Rat Arria V GX, s ≤ 3.25 Gbps V GX, GT, S2	es > 3.25 Gbj GT, SX, and across Supp K, and ST De	ps across Sup ST Devices a orted AC Gai vices diagram	ported AC nd CTLE n and DC ns.	dB

Table 1-23: Transmitter Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transc	eiver Speed G	irade 4	Transceiver Speed Grade 6			Unit
Symbol/Description	Condition	Min	Тур	Max	Min	Тур	Max	Onic
Supported I/O standards		1.5 V PCML						
Data rate	_	611		6553.6	611	_	3125	Mbps
V _{OCM} (AC coupled)	_	_	650	_		650	_	mV
V _{OCM} (DC coupled)	\leq 3.2Gbps ⁽³²⁾	670	700	730	670	700	730	mV
	85- Ω setting	_	85	_		85	_	Ω
Differential on-chip	100- Ω setting	—	100	—	_	100	_	Ω
termination resistors	120- Ω setting		120			120		Ω
	150-Ω setting	_	150	—		150	_	Ω
Intra-differential pair skew	TX V_{CM} = 0.65 V (AC coupled) and slew rate of 15 ps	—	_	15	_	_	15	ps
Intra-transceiver block transmitter channel-to- channel skew	×6 PMA bonded mode	_	_	180	_	—	180	ps

⁽³⁷⁾ The rate match FIFO supports only up to ±300 parts per million (ppm).
⁽³⁸⁾ The Quartus Prime software allows AC gain setting = 3 for design with data rate between 611 Mbps and 1.25 Gbps only.



CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain

Figure 1-3: CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices







DLL Frequency Range Specifications

Table 1-43: DLL Frequency Range Specifications for Arria V Devices

Parameter	-I3, -C4	-I5, -C5	-C6	Unit	
DLL operating frequency range	200 - 667	200 - 667	200 - 667	MHz	

DQS Logic Block Specifications

Table 1-44: DQS Phase Shift Error Specifications for DLL-Delayed Clock (t_{DOS PSERR}) for Arria V Devices

This error specification is the absolute maximum and minimum error.

Number of DQS Delay Buffer	–I3, –C4	–I5, –C5	-C6	Unit
2	40	80	80	ps



Memory Output Clock Jitter Specifications

Table 1-45: Memory Output Clock Jitter Specifications for Arria V Devices

The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard. The memory output clock jitter is applicable when an input jitter of 30 ps (p-p) is applied with bit error rate (BER) 10^{-12} , equivalent to 14 sigma. Altera recommends using the UniPHY intellectual property (IP) with PHYCLK connections for better jitter performance.

Parameter	Clock Notwork	Symbol	-I3, -C4		–I5, –C5		-C6		Unit	
		Symbol	Min	Max	Min	Max	Min	Max	Onit	
Clock period jitter	PHYCLK	t _{JIT(per)}	-41	41	-50	50	-55	55	ps	
Cycle-to-cycle period jitter	PHYCLK	t _{JIT(cc)}	6	3	9	0	9	94	ps	

OCT Calibration Block Specifications

Table 1-46: OCT Calibration Block Specifications for Arria V Devices

Symbol	Description	Min	Тур	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	_		20	MHz
T _{OCTCAL}	Number of octus RCLK clock cycles required for $R_{\rm S}$ OCT/R_T OCT calibration		1000		Cycles
T _{OCTSHIFT}	Number of OCTUSRCLK clock cycles required for OCT code to shift out		32	_	Cycles
T _{RS_RT}	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	_	2.5		ns



After the Boot ROM code exits and control is passed to the preloader, software can adjust the value of drvsel and smplsel via the system manager. drvsel can be set from 1 to 7 and smplsel can be set from 0 to 7. While the preloader is executing, the values for SDMMC_CLK and SDMMC_CLK_OUT increase to a maximum of 200 MHz and 50 MHz respectively.

The SD/MMC interface calibration support will be available in a future release of the preloader through the SoC EDS software update.

Symbol	Description	Min	Мах	Unit
	SDMMC_CLK clock period (Identification mode)	20	_	ns
T _{sdmmc_clk} (internal reference clock)	SDMMC_CLK clock period (Default speed mode)	5	—	ns
	SDMMC_CLK clock period (High speed mode)	5	_	ns
	SDMMC_CLK_OUT clock period (Identification mode)	2500	—	ns
T _{sdmmc_clk_out} (interface output clock)	SDMMC_CLK_OUT clock period (Default speed mode)	40	_	ns
	SDMMC_CLK_OUT clock period (High speed mode)	20	—	ns
T _{dutycycle}	SDMMC_CLK_OUT duty cycle	45	55	%
T _d	SDMMC_CMD/SDMMC_D output delay	$\frac{(T_{sdmmc_clk} \times drvsel)/2}{-1.23}$	$\begin{array}{l}(\mathrm{T}_{sdmmc_clk}\times\texttt{drvsel})/2\\+1.69^{\ (87)}\end{array}$	ns
T _{su}	Input setup time	$1.05 - (T_{sdmmc_clk} \times smplsel)/2^{(88)}$	_	ns
T _h	Input hold time	$\frac{(T_{sdmmc_clk} \times smplsel)}{2^{(88)}}$	_	ns



⁽⁸⁷⁾ drvsel is the drive clock phase shift select value.

⁽⁸⁸⁾ smplsel is the sample clock phase shift select value.

Symbol	Description	Min	Max	Unit
$T_{dh}^{(89)}$	Data to write enable hold time	5	—	ns
T _{cea}	Chip enable to data access time		25	ns
T _{rea}	Read enable to data access time		16	ns
T _{rhz}	Read enable to data high impedance		100	ns
T _{rr}	Ready to read enable low	20	—	ns

Figure 1-17: NAND Command Latch Timing Diagram





1-80 AS Configuration Timing

Symbol	Parameter	Minimum	Maximum	Unit
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times maximum$ DCLK period	—	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + ($T_{init} \times CLKUSR$ period)		
T _{init}	Number of clock cycles required for device initialization	8,576		Cycles

Related Information

FPP Configuration Timing

Provides the FPP configuration timing waveforms.

AS Configuration Timing

Table 1-68: AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices

The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

The t_{CF2CD} , t_{CF2ST0} , t_{CFG} , t_{STATUS} , and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in PS Timing Parameters for Arria V Devices table. You can obtain the t_{CF2ST1} value if you do not delay configuration by externally holding nSTATUS low.

Symbol	Parameter	Minimum	Maximum	Unit
t _{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	2	ns
t _{SU}	Data setup time before the falling edge on DCLK	1.5		ns
t _{DH}	Data hold time after the falling edge on DCLK	0	_	ns
t _{CD2UM}	CONF_DONE high to user mode	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	_	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + ($T_{init} \times CLKUSR$ period)	_	—
T _{init}	Number of clock cycles required for device initialization	8,576		Cycles



Related Information

- PowerPlay Early Power Estimator User Guide For more information about the EPE tool.
- **PowerPlay Power Analysis** ٠ For more information about PowerPlay power analysis.

Power Consumption

Altera offers two ways to estimate power consumption for a design-the Excel-based Early Power Estimator and the Quartus II PowerPlay Power Analyzer feature.

Note: You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

Related Information

- PowerPlay Early Power Estimator User Guide For more information about the EPE tool.
- PowerPlay Power Analysis For more information about PowerPlay power analysis.

I/O Pin Leakage Current

Table 2-8: I/O Pin Leakage Current for Arria V GZ Devices

If $V_O = V_{CCIO}$ to $V_{CCIOMax}$, 100 µA of leakage current per I/O is expected.

Symbol	Description	Conditions	Min	Тур	Max	Unit
II	Input pin	$V_{I} = 0 V$ to $V_{CCIOMAX}$	-30	—	30	μΑ
I _{OZ}	Tri-stated I/O pin	$V_{O} = 0 V$ to $V_{CCIOMAX}$	-30	_	30	μΑ



1/O Standard	V _{CCIO} (V) ⁽¹²⁸⁾		V _{ID} (mV) ⁽¹²⁹⁾		V _{ICM(DC)} (V)		V _{OD} (V) ⁽¹³⁰⁾		V _{OCM} (V) ⁽¹³⁰⁾						
	Min	Тур	Мах	Min	Condition	Max	Min	Condition	Max	Min	Тур	Max	Min	Тур	Мах
RSDS (HIO) (133)	2.375	2.5	2.625	100	V _{CM} = 1.25 V		0.3		1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini- LVDS (HIO) (134)	2.375	2.5	2.625	200	_	600	0.4	_	1.325	0.25		0.6	1	1.2	1.4
LVPECL		_	_	300		_	0.6	D _{MAX} ≤ 700 Mbps	1.8	_	_		_	_	
(135), (136)	_	_	_	300			1	D _{MAX} > 700 Mbps	1.6	_	_		_		

Related Information

Glossary on page 2-73



⁽¹²⁸⁾ Differential inputs are powered by VCCPD which requires 2.5 V.

⁽¹²⁹⁾ The minimum VID value is applicable over the entire common mode range, VCM.

RL range: $90 \le RL \le 110 \Omega$. (130)

⁽¹³³⁾ For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.

⁽¹³⁴⁾ For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.

⁽¹³⁵⁾ LVPECL is only supported on dedicated clock input pins.

⁽¹³⁶⁾ For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

2-44 Periphery Performance

Description	Min	Тур	Мах	Unit
Diode ideality factor	1.006	1.008	1.010	—

Periphery Performance

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

Note: The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

High-Speed Clock Specifications

Table 2-39: High-Speed Clock Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

Arria V GZ devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 230 Mbps
- True mini-LVDS output standard with data rates of up to 340 Mbps



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Symbol	Conditions	C3, I3L			C4, I4			Unit
Symbol	Conditions	Min	Тур	Мах	Min	Тур	Max	Onic
f _{HSCLK_in} (input clock frequency) True Differential I/O Standards ⁽¹⁷⁹⁾	Clock boost factor W = 1 to 40 $^{(180)}$	5	_	625	5	_	525	MHz
f _{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 $^{(180)}$	5		625	5		525	MHz
f _{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 $^{(180)}$	5		420	5		420	MHz
f _{HSCLK_OUT} (output clock frequency)	—	5		625 (181)	5		525 (181)	MHz

Transmitter High-Speed I/O Specifications

Table 2-40: Transmitter High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.



 $^{^{(179)}\,}$ This only applies to DPA and soft-CDR modes.

⁽¹⁸⁰⁾ Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.

⁽¹⁸¹⁾ This is achieved by using the LVDS clock network.

Symbol	Conditions		C4, I4			Unit		
Symbol	Conditions	Min	Тур	Мах	Min	Тур	Max	Onic
True Differential I/O Standards - f _{HSDRDPA} (data rate)	SERDES factor J = 3 to 10 (192), (193), (194), (195), (196), (197)	150	_	1250	150	—	1050	Mbps
	SERDES factor $J \ge 4$ LVDS RX with DPA (193), (195), (196), (197)	150	_	1600	150		1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(198)	_	(199)	(198)		(199)	Mbps
	SERDES factor J = 1, uses SDR Register	(198)	_	(199)	(198)		(199)	Mbps
	SERDES factor $J = 3$ to 10	(198)	—	(200)	(198)	—	(200)	Mbps
f _{HSDR} (data rate)	SERDES factor J = 2, uses DDR Registers	(198)	—	(199)	(198)		(199)	Mbps
	SERDES factor J = 1, uses SDR Register	(198)	—	(199)	(198)	—	(199)	Mbps

 $^{(192)}$ The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

⁽¹⁹³⁾ Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.

⁽¹⁹⁴⁾ Arria V GZ LVDS serialization and de-serialization factor needs to be x4 and above.

⁽¹⁹⁵⁾ Requires package skew compensation with PCB trace length.

⁽¹⁹⁶⁾ Do not mix single-ended I/O buffer within LVDS I/O bank.

⁽¹⁹⁷⁾ Chip-to-chip communication only with a maximum load of 5 pF.

⁽¹⁹⁸⁾ The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

⁽¹⁹⁹⁾ The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.

⁽²⁰⁰⁾ You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.





Non DPA Mode High-Speed I/O Specifications

Table 2-46: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions -		C3, I3I			Unit		
		Min	Тур	Max	Min	Тур	Max	Unit
Sampling Window	—	_		300	_		300	ps



Table 2-55: DCLK-to-DATA[] Ratio for Arria V GZ Devices

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the data rate in bytes per second (Bps), or words per second (Wps). For example, in FPP ×16 when the DCLK-to-DATA[] ratio is 2, the DCLK frequency must be 2 times the data rate in Wps. Arria V GZ devices use the additional clock cycles to decrypt and decompress the configuration data.

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
	Disabled	Disabled	1
FDD V8	Disabled	Enabled	1
111 ×0	Enabled	Disabled	2
	Enabled	Enabled	2
	Disabled	Disabled	1
FDD v16	Disabled	Enabled	2
111 ×10	Enabled	Disabled	4
	Enabled	Enabled	4
	Disabled	Disabled	1
FDD ~32	Disabled	Enabled	4
111 ~52	Enabled	Disabled	8
	Enabled	Enabled	8





Symbol	Parameter	Minimum	Maximum	Unit
t _{CO}	DCLK falling edge to AS_DATA0/ASDO output	-	4	ns
t _{SU}	Data setup time before falling edge on DCLK	1.5		ns
t _H	Data hold time after falling edge on DCLK	0	—	ns
t _{CD2UM}	CONF_DONE high to user mode ⁽²¹⁶⁾	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK}$ period	_	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (8576 × clkusr period)	_	_

Table 2-59: DCLK Frequency Specification in the AS Configuration Scheme

This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

The AS multi-device configuration scheme does not support ${\tt DCLK}$ frequency of 100 MHz.

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

Related Information

- Passive Serial Configuration Timing on page 2-67
- Configuration, Design Security, and Remote System Upgrades in Arria V Devices





⁽²¹⁶⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

2-70 Remote System Upgrades Circuitry Timing Specification

Table 2-62: Uncompressed .rbf Sizes for Arria V GZ Devices

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ⁽²²³⁾
Arria V GZ	E1	137,598,880	562,208
	E3	137,598,880	562,208
	E5	213,798,880	561,760
	E7	213,798,880	561,760

Table 2-63: Minimum Configuration Time Estimation for Arria V GZ Devices

Variant	Member Code	Active Serial ⁽²²⁴⁾		Fast Passive Parallel ⁽²²⁵⁾			
		Width	DCLK (MHz)	Min Config Time (ms)	Width	DCLK (MHz)	Min Config Time (ms)
Arria V GZ	E1	4	100	344	32	100	43
	E3	4	100	344	32	100	43
	E5	4	100	534	32	100	67
	E7	4	100	534	32	100	67

Remote System Upgrades Circuitry Timing Specification

Table 2-64: Remote System Upgrade Circuitry Timing Specifications

Parameter	Minimum	Maximum	Unit
t _{RU_nCONFIG} ⁽²²⁶⁾	250	_	ns
t _{RU_nRSTIMER} ⁽²²⁷⁾	250	_	ns

⁽²²³⁾ The IOCSR **.rbf** size is specifically for the Configuration via Protocol (CvP) feature.

⁽²²⁴⁾ DCLK frequency of 100 MHz using external CLKUSR.

⁽²²⁵⁾ Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.



Term	Definition
t _C	High-speed receiver and transmitter input and output clock period.
TCCS (channel-to- channel-skew)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t _{DUTY}	High-speed I/O block—Duty cycle on the high-speed transmitter output clock.
t _{FALL}	Signal high-to-low transition time (80-20%)
t _{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.
t _{OUTPJ_IO}	Period jitter on the general purpose I/O driven by a PLL.
t _{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL.
t _{RISE}	Signal low-to-high transition time (20-80%)
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = $1/(\text{receiver input clock frequency multiplication factor}) = t_C/w)$
V _{CM(DC)}	DC common mode input voltage.
V _{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.
V _{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
V _{DIF(AC)}	AC differential input voltage—Minimum AC input differential voltage required for switching.
V _{DIF(DC)}	DC differential input voltage— Minimum DC input differential voltage required for switching.
V _{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
V _{IH(AC)}	High-level AC input voltage
V _{IH(DC)}	High-level DC input voltage
V _{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
V _{IL(AC)}	Low-level AC input voltage
V _{IL(DC)}	Low-level DC input voltage

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