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Intel - 5AGXFB1H4F40C4N Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Details	
Product Status	Obsolete
Number of LABs/CLBs	14151
Number of Logic Elements/Cells	300000
Total RAM Bits	17358848
Number of I/O	704
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxfb1h4f40c4n

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Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1-1: Absolute Maximum Ratings for Arria V Devices

Symbol	Description	Minimum	Maximum	Unit
V _{CC}	Core voltage power supply	-0.50	1.43	V
V _{CCP}	Periphery circuitry, PCIe [®] hardIP block, and transceiver physical coding sublayer (PCS) power supply	-0.50	1.43	V
V _{CCPGM}	Configuration pins power supply	-0.50	3.90	V
V _{CC_AUX}	Auxiliary supply	-0.50	3.25	V
V _{CCBAT}	Battery back-up power supply for design security volatile key register	-0.50	3.90	V
V _{CCPD}	I/O pre-driver power supply	-0.50	3.90	V
V _{CCIO}	I/O power supply	-0.50	3.90	V
V _{CCD_FPLL}	Phase-locked loop (PLL) digital power supply	-0.50	1.80	V
V _{CCA_FPLL}	PLL analog power supply	-0.50	3.25	V
V _{CCA_GXB}	Transceiver high voltage power	-0.50	3.25	V
V _{CCH_GXB}	Transmitter output buffer power	-0.50	1.80	V
V _{CCR_GXB}	Receiver power	-0.50	1.50	V
V _{CCT_GXB}	Transmitter power	-0.50	1.50	V
V _{CCL_GXB}	Transceiver clock network power	-0.50	1.50	V
VI	DC input voltage	-0.50	3.80	V
V _{CC_HPS}	HPS core voltage and periphery circuitry power supply	-0.50	1.43	V
V _{CCPD_HPS}	HPS I/O pre-driver power supply	-0.50	3.90	V
V _{CCIO_HPS}	HPS I/O power supply	-0.50	3.90	V
V _{CCRSTCLK_HPS}	HPS reset and clock input pins power supply	-0.50	3.90	V



1-4 Recommended Operating Conditions

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
		3.8	100	%
		3.85	68	%
		3.9	45	%
		3.95	28	%
		4	15	%
		4.05	13	%
		4.1	11	%
Vi (AC) AC input voltage	4.15	9	%	
	AC input voltage	4.2	8	%
		4.25	7	%
		4.3	Overshoot Duration as % of High Time 100 68 45 28 15 13 11 9 8 7 5.4 3.2 1.9 1.1 0.6 0.4 0.2	%
		Condition (V) Overshoot Duration as % of 3.8 100 3.85 68 3.9 45 3.95 28 4 15 4.05 13 4.1 11 4.15 9 4.2 8 4.25 7 4.3 5.4 4.35 3.2 4.4 1.9 4.45 1.1 4.5 0.6 4.55 0.4 4.6 0.2	3.2	%
		4.4	1.9	%
		4.45	1.1	%
		4.5	0.6	%
		4.55	0.4	%
		4.6	0.2	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Arria V devices.

Recommended Operating Conditions

Table 1-3: Recommended Operating Conditions for Arria V Devices

This table lists the steady-state voltage values expected from Arria V devices. Power supply ramps must all be strictly monotonic, without plateaus.



Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
Symbol/Description	Condition	Min	Тур	Max	Min	Тур	Max	Onic
Minimum differential eye opening at the receiver serial input pins ⁽³⁰⁾	_	100	_	_	100	_	_	mV
V _{ICM} (AC coupled)	—	_	0.7/0.75/ 0.8 ⁽³¹⁾			0.7/0.75/ 0.8 ⁽³¹⁾	—	mV
V _{ICM} (DC coupled)	\leq 3.2Gbps ⁽³²⁾	670	700	730	670	700	730	mV
	85- Ω setting		85			85	—	Ω
Differential on-chip	100- Ω setting		100			100		Ω
termination resistors	120-Ω setting		120			120	—	Ω
	150-Ω setting		150			150	—	Ω
$t_{LTR}^{(33)}$	_			10		—	10	μs
$t_{LTD}^{(34)}$		4	_		4	_	—	μs
t _{LTD_manual} ⁽³⁵⁾		4			4	—		μs
$t_{LTR_LTD_manual}^{(36)}$		15			15	—	—	μs
Programmable ppm detector ⁽³⁷⁾	_		±62.5, 100, 125, 200, 250, 300, 500, and 1000					ppm

⁽³⁰⁾ The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(31) The AC coupled $V_{ICM} = 700 \text{ mV}$ for Arria V GX and SX in PCIe mode only. The AC coupled $V_{ICM} = 750 \text{ mV}$ for Arria V GT and ST in PCIe mode only.

⁽³²⁾ For standard protocol compliance, use AC coupling.

 $^{(33)}$ t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

 $^{(34)}$ t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.

 $^{(35)}$ t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.

 $t_{\text{LTR_LTD_manual}}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.



Transceiver Specifications for Arria V GT and ST Devices

Table 1-26: Reference Clock Specifications	for Arria V GT and ST Devices
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Symbol/Description	Condition	Tran	sceiver Speed Gra	Unit	
Symbol/Description	Condition	Min	Тур	Мах	Onic
Supported I/O standards	1.2 V PCML, 1.4 VPCML,	1.5 V PCML, 2.5	V PCML, Differe	ential LVPECL ⁽⁴⁰⁾	, HCSL, and LVDS
Input frequency from REFCLK input pins	_	27		710	MHz
Rise time	Measure at ±60 mV of differential signal ⁽⁴¹⁾			400	ps
Fall time	Measure at ±60 mV of differential signal ⁽⁴¹⁾			400	ps
Duty cycle	_	45		55	%
Peak-to-peak differential input voltage	—	200		300 ⁽⁴²⁾ /2000	mV
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30		33	kHz
Spread-spectrum downspread	PCIe		0 to -0.5%		_
On-chip termination resistors	—		100		Ω
V _{ICM} (AC coupled)	—	—	1.2		V
V _{ICM} (DC coupled)	HCSL I/O standard for the PCIe reference clock	250		550	mV



⁽⁴⁰⁾ Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

REFCLK performance requires to meet transmitter REFCLK phase noise specification. (41)

⁽⁴²⁾ The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain

Figure 1-3: CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices





High-Speed I/O Specifications

Table 1-40: High-Speed I/O Specifications for Arria V Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block. When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

The Arria V devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 360 Mbps
- True mini-LVDS output standard with data rates of up to 400 Mbps

Symbol		Condition	-I3, -C4		–I5, –C5		-C6			Unit		
	Symbol	Condition	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
f _{HSCLK_in} (inp Differential I	out clock frequency) True /O Standards	Clock boost factor W = 1 to $40^{(72)}$	5		800	5		750	5	_	625	MHz
f _{HSCLK_in} (inp Single-Ended	out clock frequency) I I/O Standards ⁽⁷³⁾	Clock boost factor W = 1 to $40^{(72)}$	5		625	5		625	5		500	MHz
f _{HSCLK_in} (inp Single-Ended	out clock frequency) I I/O Standards ⁽⁷⁴⁾	Clock boost factor W = 1 to $40^{(72)}$	5	_	420	5	_	420	5	—	420	MHz
f _{HSCLK_OUT} (output clock frequency)	_	5	_	625(75)	5	_	625(75)	5		500 ⁽⁷⁵⁾	MHz
Transmitter	True Differential I/O Standards - f _{HSDR} (data rate)	SERDES factor J =3 to $10^{(76)}$	(77)		1250	(77)		1250	(77)		1050	Mbps

⁽⁷³⁾ This applies to DPA and soft-CDR modes only.





⁽⁷²⁾ Clock boost factor (W) is the ratio between the input data rate and the input clock rate.

⁽⁷⁴⁾ This applies to non-DPA mode only.

⁽⁷⁵⁾ This is achieved by using the LVDS clock network.

 $^{^{(76)}}$ The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

⁽⁷⁷⁾ The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

Figure 1-7: Timing Diagram for oe and dyn_term_ctrl Signals



Duty Cycle Distortion (DCD) Specifications

Table 1-47: Worst-Case DCD on Arria V I/O Pins

The output DCD cycle only applies to the I/O buffer. It does not cover the system DCD.

Symbol	-I3,	-C4	-C5, -I5		-(Unit	
	Min	Max	Min	Max	Min	Max	Onic
Output Duty Cycle	45	55	45	55	45	55	%

HPS Specifications

This section provides HPS specifications and timing for Arria V devices.

For HPS reset, the minimum reset pulse widths for the HPS cold and warm reset signals (HPS_nRST and HPS_nPOR) are six clock cycles of HPS_CLK1.



Figure 1-15: MDIO Timing Diagram



I²C Timing Characteristics

Table 1-59: I²C Timing Requirements for Arria V Devices

Symbol	Description	Standar	d Mode	Fast I	Mode	Unit
Symbol	Description	Min	Max	Min	Max	Ont
T _{clk}	Serial clock (SCL) clock period	10	—	2.5		μs
T _{clkhigh}	SCL high time	4.7	—	0.6		μs
T _{clklow}	SCL low time	4	—	1.3		μs
T _s	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1		μs
T _h	Hold time for SCL to SDA data	0	3.45	0	0.9	μs
T _d	SCL to SDA output data delay	—	0.2		0.2	μs
T _{su_start}	Setup time for a repeated start condition	4.7	_	0.6		μs
T _{hd_start}	Hold time for a repeated start condition	4	_	0.6		μs
T _{su_stop}	Setup time for a stop condition	4	_	0.6	_	μs



FPP Configuration Timing

DCLK-to-DATA[] Ratio (r) for FPP Configuration

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP $\times 16$ where the *r* is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

Table 1-65: DCLK-to-DATA[] Ratio for Arria V Devices

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
	Off	Off	1
EDD (9 bit wide)	On	Off	1
frr (o-bit wide)	Off	On	2
	On	On	2
	Off	Off	1
EDD (16 bit wide)	On	CompressionOffOffOffOffOnOffOffOnOffOnOnOnOffOffOffOffOnOffOnOffOnOffOnOnOnOnOnOnOnOnOnOn	2
fif (lo-bit wide)	Off	On	4
	On	OffOffOffOffOnOffOffOnOffOnOnOnOffOffOffOffOffOffOnOffOnOffOnOffOnOnOffOnOnOn	4

FPP Configuration Timing when DCLK-to-DATA[] = 1

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8 and FPP ×16. For the respective DCLKto-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Arria V Devices table.

Table 1-66: FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Arria V Devices

Symbol	Parameter	Minimum	Maximum	Unit
t _{CF2CD}	nCONFIG low to CONF_DONE low	_	600	ns
t _{CF2ST0}	nconfig low to nstatus low	_	600	ns
t _{CFG}	nCONFIG low pulse width	2		μs

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1-80 AS Configuration Timing

Symbol	Parameter	Minimum	Maximum	Unit
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times maximum$ DCLK period	—	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + ($T_{init} \times CLKUSR$ period)		
T _{init}	Number of clock cycles required for device initialization	8,576		Cycles

Related Information

FPP Configuration Timing

Provides the FPP configuration timing waveforms.

AS Configuration Timing

Table 1-68: AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices

The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

The t_{CF2CD} , t_{CF2ST0} , t_{CFG} , t_{STATUS} , and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in PS Timing Parameters for Arria V Devices table. You can obtain the t_{CF2ST1} value if you do not delay configuration by externally holding nSTATUS low.

Symbol	Parameter	Minimum	Maximum	Unit
t _{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	2	ns
t _{SU}	Data setup time before the falling edge on DCLK	1.5		ns
t _{DH}	Data hold time after the falling edge on DCLK	0	_	ns
t _{CD2UM}	CONF_DONE high to user mode	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	_	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + ($T_{init} \times CLKUSR$ period)	_	—
T _{init}	Number of clock cycles required for device initialization	8,576		Cycles







Symbol	Description	Condition Minimum ⁽¹¹⁴⁾ Typical Maximum		Maximum ⁽¹¹⁴⁾	Unit	
VI	DC input voltage	_	-0.5	_	3.6	V
Vo	Output voltage		0	_	V _{CCIO}	V
Т.	Operating junction temperature	Commercial	0		85	°C
IJ	Operating junction temperature	Industrial	-40	_	100	°C
t	Power supply ramp time	Standard POR	200 µs	_	100 ms	
'RAMP		Fast POR	200 µs	—	4 ms	

Recommended Transceiver Power Supply Operating Conditions

Table 2-6: Recommended Transceiver Power Supply Operating Conditions for Arria V GZ Devices

Symbol	Description	Minimum ⁽¹¹⁸⁾	Typical	Maximum ⁽¹¹⁸⁾	Unit
V _{CCA_GXBL}	Transcaiver channel DLL newer supply (left side)	2.85	3.0	3.15	V
(119), (120)	Transceiver channel FLL power supply (left side)	2.375	2.5	2.625	V
V _{CCA} (10) (120) Transceiver channel PLL power supply (right side)	2.85	3.0	3.15	V	
GXBR ⁽¹¹⁹⁾ , ⁽¹²⁰⁾	GXBR ⁽¹¹⁹⁾ , ⁽¹²⁰⁾ (120) (Transceiver channel PLL power supply (right side)	2.375	2.5	2.625	v
V _{CCHIP_L}	Transceiver hard IP power supply (left side)	0.82	0.85	0.88	V
V _{CCHSSI_L}	Transceiver PCS power supply (left side)	0.82	0.85	0.88	V
V _{CCHSSI_R}	Transceiver PCS power supply (right side)	0.82	0.85	0.88	V

⁽¹¹⁴⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹¹⁸⁾ This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹²⁰⁾ When using ATX PLLs, the supply must be 3.0 V.



⁽¹¹⁹⁾ This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

Symbol	Parameter	Min	Тур	Max	Unit
k _{VALUE}	Numerator of Fraction	128	8388608	2147483648	—
f _{RES}	Resolution of VCO frequency ($f_{INPFD} = 100 \text{ MHz}$)	390625	5.96	0.023	Hz

Related Information

- Duty Cycle Distortion (DCD) Specifications on page 2-56
- DLL Range Specifications on page 2-53

DSP Block Specifications

Table 2-35: DSP Block Performance Specifications for Arria V GZ Devices

Mada	Performar	nce		Unit
Mode	C3, I3L	C4	14	Onit
Modes using One DSP Block				
Three 9 × 9	480	420		MHz
One 18 × 18	480	420	400	MHz
Two partial 18×18 (or 16×16)	480	420	400	MHz
One 27 × 27	400	35	50	MHz
One 36 × 18	400	35	350	
One sum of two 18×18 (One sum of two 16×16)	400	35	50	MHz
One sum of square	400	35	50	MHz
One 18×18 plus $36 (a \times b) + c$	400	35	50	MHz
Modes using Two DSP Blocks				
Three 18 × 18	400	35	50	MHz
One sum of four 18×18	380	30	00	MHz



Memory	Mode	Resources Used		Performance				Unit
wieniory	moue	ALUTs	Memory	C3	C4	I3L	14	
	Single-port, all supported widths	0	1	650	550	500	450	MHz
	Simple dual-port, all supported widths	0	1	650	550	500	450	MHz
MOOV	Simple dual-port with the read-during-write option set to Old Data , all supported widths	0	1	455	400	455	400	MHz
M20K Block	Simple dual-port with ECC enabled, 512×32	0	1	400	350	400	350	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	0	1	500	450	500	450	MHz
	True dual port, all supported widths	0	1	650	550	500	450	MHz
	ROM, all supported widths	0	1	650	550	500	450	MHz

Temperature Sensing Diode Specifications

Table 2-37: Internal Temperature Sensing Diode Specification

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
-40°C to 100°C	±8°C	No	1 MHz, 500 kHz	< 100 ms	8 bits	8 bits

Table 2-38: External Temperature Sensing Diode Specifications for Arria V GZ Devices

Description	Min	Тур	Max	Unit
I _{bias} , diode source current	8		200	μΑ
V _{bias,} voltage across diode	0.3		0.9	V
Series resistance		_	< 1	Ω



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Symbol	Conditions	C3, I3L		C4, I4			Unit	
Symbol	Conditions	Min	Тур	Мах	Min	Тур	Max	Onic
f _{HSCLK_in} (input clock frequency) True Differential I/O Standards ⁽¹⁷⁹⁾	Clock boost factor W = 1 to 40 $^{(180)}$	5	_	625	5	_	525	MHz
f _{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 $^{(180)}$	5		625	5		525	MHz
f _{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 $^{(180)}$	5		420	5		420	MHz
f _{HSCLK_OUT} (output clock frequency)	—	5		625 (181)	5		525 (181)	MHz

Transmitter High-Speed I/O Specifications

Table 2-40: Transmitter High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.



 $^{^{(179)}\,}$ This only applies to DPA and soft-CDR modes.

⁽¹⁸⁰⁾ Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.

⁽¹⁸¹⁾ This is achieved by using the LVDS clock network.

DPA Mode High-Speed I/O Specifications

Table 2-42: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions	C3, I3L		C4, I4			Unit	
		Min	Тур	Мах	Min	Тур	Мах	Unit
DPA run length	—	_	_	10000	_		10000	UI

Figure 2-3: DPA Lock Time Specification with DPA PLL Calibration Enabled



Table 2-43: DPA Lock Time Specifications for Arria V GZ Devices

The DPA lock time is for one channel.

One data transition is defined as a 0-to-1 or 1-to-0 transition.

The DPA lock time stated in this table applies to both commercial and industrial grade.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽²⁰¹⁾	Maximum
SPI-4	0000000001111111111	2	128	640 data transitions



⁽²⁰¹⁾ This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.



Non DPA Mode High-Speed I/O Specifications

Table 2-46: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions	C3, I3L				Unit		
		Min	Тур	Max	Min	Тур	Max	Unit
Sampling Window	—	_		300	_		300	ps



Table 2-57: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t _{CFG}	nCONFIG low pulse width	2	_	μs
t _{STATUS}	nSTATUS low pulse width	268	1,506 (210)	μs
t _{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 (211)	μs
t _{CF2CK} ⁽²¹²⁾	nCONFIG high to first rising edge on DCLK	1,506	_	μs
t _{ST2CK} ⁽²¹²⁾	nSTATUS high to first rising edge of DCLK	2	_	μs
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5	_	ns
t _{DH}	DATA[] hold time after rising edge on DCLK	N-1/f _{DCLK} ⁽²¹³⁾		S
t _{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	_	S
t _{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$		S
t _{CLK}	DCLK period	1/f _{MAX}	_	S
f _{MAX}	DCLK frequency (FPP ×8/×16)	—	125	MHz
	DCLK frequency (FPP ×32)	—	100	MHz
t _R	Input rise time	—	40	ns
t _F	Input fall time	—	40	ns
t _{CD2UM}	CONF_DONE high to user mode ⁽²¹⁴⁾	175	437	μs

⁽²¹⁰⁾ You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

⁽²¹¹⁾ You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

 $^{(212)}$ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

 $^{(213)}$ N is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.

⁽²¹⁴⁾ The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

Arria V GZ Device Datasheet

Altera Corporation



Passive Serial Configuration Timing

Figure 2-10: PS Configuration Timing Waveform

Timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.



Notes:

- 1. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- 2. After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.
- 3. After power-up, before and during configuration, CONF_DONE is low.
- 4. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- 5. DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the Device and Pins Option.
- 6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- 7. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.



Term	Definition		
	Single-Ended WaveformVODPositive Channel (p) = VOHVCMNegative Channel (n) = VOLGroundGround		
	Differential Waveform V_{0D} V_{0D} V_{0D} V_{0D}		
f _{HSCLK}	Left and right PLL input clock frequency.		
f _{HSDR}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDR} = 1/TUI), non-DPA.		
f _{hsdrdpa}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDRDPA} = 1/TUI), DPA.		
J	High-speed I/O block—Deserialization factor (width of parallel data bus).		



