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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	14151
Number of Logic Elements/Cells	300000
Total RAM Bits	17358848
Number of I/O	704
Number of Gates	-
Voltage - Supply	1.12V ~ 1.18V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/5agxfb1h4f40i3n">https://www.e-xfl.com/product-detail/intel/5agxfb1h4f40i3n</a>

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This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Arria® V devices.

Arria V devices are offered in commercial and industrial grades. Commercial devices are offered in –C4 (fastest), –C5, and –C6 speed grades. Industrial grade devices are offered in the –I3 and –I5 speed grades.

## Related Information

### [Arria V Device Overview](#)

Provides more information about the densities and packages of devices in the Arria V family.

## Electrical Characteristics

The following sections describe the operating conditions and power consumption of Arria V devices.

### Operating Conditions

Arria V devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Arria V devices, you must consider the operating requirements described in this section.

### Absolute Maximum Ratings

This section defines the maximum operating conditions for Arria V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms.

The functional operation of the device is not implied for these conditions.

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Symbol	Description	Condition	Minimum <sup>(7)</sup>	Typical	Maximum <sup>(7)</sup>	Unit
$V_{CCPD\_HPS}^{(8)}$	HPS I/O pre-driver power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
$V_{CCIO\_HPS}$	HPS I/O buffers power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V <sup>(9)</sup>	1.283	1.35	1.418	V
$V_{CCRSTCLK\_HPS}$	HPS reset and clock input pins power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
$V_{CCPLL\_HPS}$	HPS PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V

<sup>(7)</sup> The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

<sup>(8)</sup>  $V_{CCPD\_HPS}$  must be 2.5 V when  $V_{CCIO\_HPS}$  is 2.5, 1.8, 1.5, or 1.2 V.  $V_{CCPD\_HPS}$  must be 3.0 V when  $V_{CCIO\_HPS}$  is 3.0 V.  $V_{CCPD\_HPS}$  must be 3.3 V when  $V_{CCIO\_HPS}$  is 3.3 V.

<sup>(9)</sup>  $V_{CCIO\_HPS}$  1.35 V is supported for HPS row I/O bank only.

Symbol	Description	Condition	Minimum <sup>(7)</sup>	Typical	Maximum <sup>(7)</sup>	Unit
V <sub>CC_AUX_SHARED</sub>	HPS auxiliary power supply	—	2.375	2.5	2.625	V

**Related Information**

**Recommended Operating Conditions** on page 1-4

Provides the steady-state voltage values for the FPGA portion of the device.

**DC Characteristics****Supply Current and Power Consumption**

Altera offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the Quartus® Prime PowerPlay Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the resources you use.

The Quartus Prime PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

**Related Information**

- **PowerPlay Early Power Estimator User Guide**  
Provides more information about power estimation tools.
- **PowerPlay Power Analysis chapter, Quartus Prime Handbook**  
Provides more information about power estimation tools.

<sup>(7)</sup> The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

I/O Standard	$V_{CCIO}$ (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-125	1.19	1.25	1.31	0.18	<sup>(15)</sup>	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$

## Differential HSTL and HSUL I/O Standards

Table 1-18: Differential HSTL and HSUL I/O Standards for Arria V Devices

I/O Standard	$V_{CCIO}$ (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	$V_{CCIO} + 0.3$	—	$0.5 \times V_{CCIO}$	—	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$	0.3	$V_{CCIO} + 0.48$
HSUL-12	1.14	1.2	1.3	0.26	0.26	$0.5 \times V_{CCIO} - 0.12$	$0.5 \times V_{CCIO}$	$0.5 \times V_{CCIO} + 0.12$	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$	0.44	0.44

## Differential I/O Standard Specifications

Table 1-19: Differential I/O Standard Specifications for Arria V Devices

Differential inputs are powered by  $V_{CCPD}$  which requires 2.5 V.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Transmitter $\text{REFCLK}$ phase noise <sup>(43)</sup>	10 Hz	—	—	–50	dBc/Hz
	100 Hz	—	—	–80	dBc/Hz
	1 KHz	—	—	–110	dBc/Hz
	10 KHz	—	—	–120	dBc/Hz
	100 KHz	—	—	–120	dBc/Hz
	$\geq 1$ MHz	—	—	–130	dBc/Hz
$R_{\text{REF}}$	—	—	2000 $\pm$ 1%	—	$\Omega$

Table 1-27: Transceiver Clocks Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
$\text{fixedclk}$ clock frequency	PCIe Receiver Detect	—	125	—	MHz
Transceiver Reconfiguration Controller IP ( $\text{mgmt\_clk\_clk}$ ) clock frequency	—	75	—	125	MHz

Table 1-28: Receiver Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS				
Data rate (6-Gbps transceiver) <sup>(44)</sup>	—	611	—	6553.6	Mbps

<sup>(43)</sup> The transmitter  $\text{REFCLK}$  phase jitter is 30 ps p-p (5 ps RMS) with bit error rate (BER)  $10^{-12}$ , equivalent to 14 sigma.<sup>(44)</sup> To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Symbol	V <sub>OD</sub> Setting <sup>(58)</sup>	V <sub>OD</sub> Value (mV)	V <sub>OD</sub> Setting <sup>(58)</sup>	V <sub>OD</sub> Value (mV)
	25	500	53	1060
	26	520	54	1080
	27	540	55	1100
	28	560	56	1120
	29	580	57	1140
	30	600	58	1160
	31	620	59	1180
	32	640	60	1200
	33	660		

## Transmitter Pre-Emphasis Levels

The following table lists the simulation data on the transmitter pre-emphasis levels in dB for the first post tap under the following conditions:

- Low-frequency data pattern—five 1s and five 0s
- Data rate—2.5 Gbps

The levels listed are a representation of possible pre-emphasis levels under the specified conditions only and the pre-emphasis levels may change with data pattern and data rate.

Arria V devices only support 1st post tap pre-emphasis with the following conditions:

- The 1st post tap pre-emphasis settings must satisfy  $|B| + |C| \leq 60$  where  $|B| = V_{OD}$  setting with termination value,  $R_{TERM} = 100 \Omega$  and  $|C| = 1st$  post tap pre-emphasis setting.
- $|B| - |C| > 5$  for data rates  $< 5$  Gbps and  $|B| - |C| > 8.25$  for data rates  $> 5$  Gbps.
- $(V_{MAX}/V_{MIN} - 1)\% < 600\%$ , where  $V_{MAX} = |B| + |C|$  and  $V_{MIN} = |B| - |C|$ .

Exception for PCIe Gen2 design: V<sub>OD</sub> setting = 43 and pre-emphasis setting = 19 are allowed for PCIe Gen2 design with transmit de-emphasis – 6dB setting (pipe\_txdeemp = 1'b0) using Altera PCIe Hard IP and PIPE IP cores.

<sup>(58)</sup> Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

**Table 1-34: Transceiver Compliance Specification for All Supported Protocol for Arria V GX, GT, SX, and ST Devices**

Protocol	Sub-protocol	Data Rate (Mbps)
PCIe	PCIe Gen1	2,500
	PCIe Gen2	5,000
	PCIe Cable	2,500
XAUI	XAUI 2135	3,125
Serial RapidIO® (SRIO)	SRIO 1250 SR	1,250
	SRIO 1250 LR	1,250
	SRIO 2500 SR	2,500
	SRIO 2500 LR	2,500
	SRIO 3125 SR	3,125
	SRIO 3125 LR	3,125
	SRIO 5000 SR	5,000
	SRIO 5000 MR	5,000
	SRIO 5000 LR	5,000
	SRIO_6250_SR	6,250
	SRIO_6250_MR	6,250
	SRIO_6250_LR	6,250



Table 1-38: Memory Block Performance Specifications for Arria V Devices

Memory	Mode	Resources Used		Performance			Unit
		ALUTs	Memory	–I3, –C4	–I5, –C5	–C6	
MLAB	Single port, all supported widths	0	1	500	450	400	MHz
	Simple dual-port, all supported widths	0	1	500	450	400	MHz
	Simple dual-port with read and write at the same address	0	1	400	350	300	MHz
	ROM, all supported width	—	—	500	450	400	MHz
M10K Block	Single-port, all supported widths	0	1	400	350	285	MHz
	Simple dual-port, all supported widths	0	1	400	350	285	MHz
	Simple dual-port with the read-during-write option set to <b>Old Data</b> , all supported widths	0	1	315	275	240	MHz
	True dual port, all supported widths	0	1	400	350	285	MHz
	ROM, all supported widths	0	1	400	350	285	MHz

## Internal Temperature Sensing Diode Specifications

Table 1-39: Internal Temperature Sensing Diode Specifications for Arria V Devices

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
–40 to 100°C	±8°C	No	1 MHz	< 100 ms	8 bits	8 bits

## Periphery Performance

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

Symbol	Condition	-I3, -C4			-I5, -C5			-C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	SERDES factor $J \geq 8^{(76)(78)}$ , LVDS TX with RX DPA	<sup>(77)</sup>	—	1600	<sup>(77)</sup>	—	1500	<sup>(77)</sup>	—	1250	Mbps
	SERDES factor $J = 1$ to 2, Uses DDR Registers	<sup>(77)</sup>	—	<sup>(79)</sup>	<sup>(77)</sup>	—	<sup>(79)</sup>	<sup>(77)</sup>	—	<sup>(79)</sup>	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Network - $f_{HSDR}$ (data rate) <sup>(80)</sup>	SERDES factor $J = 4$ to $10^{(81)}$	<sup>(77)</sup>	—	945	<sup>(77)</sup>	—	945	<sup>(77)</sup>	—	945	Mbps
Emulated Differential I/O Standards with One External Output Resistor Network - $f_{HSDR}$ (data rate) <sup>(80)</sup>	SERDES factor $J = 4$ to $10^{(81)}$	<sup>(77)</sup>	—	200	<sup>(77)</sup>	—	200	<sup>(77)</sup>	—	200	Mbps
$t_{x \text{ Jitter}}$ - True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps – 1.25 Gbps	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	UI

<sup>(78)</sup> The  $V_{CC}$  and  $V_{CCP}$  must be on a separate power layer and a maximum load of 5 pF for chip-to-chip interface.

<sup>(79)</sup> The maximum ideal data rate is the SERDES factor ( $J$ ) x the PLL maximum output frequency ( $f_{OUT}$ ), provided you can close the design timing and the signal integrity simulation is clean.

<sup>(80)</sup> You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

<sup>(81)</sup> When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

Term	Definition
PLL specifications	<p>Diagram of PLL specifications</p> <p><b>Legend</b></p> <ul style="list-style-type: none"><li>Reconfigurable in User Mode</li></ul> <p><b>Note:</b> (1) Core Clock can only be fed by dedicated clock input pins or PLL outputs.</p>
R <sub>L</sub>	Receiver differential input discrete resistor (external to the Arria V device).
Sampling window (SW)	<p>Timing diagram—The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown:</p> <p>Bit Time</p> <p>0.5 x TCCS   RSKM   Sampling Window (SW)   RSKM   0.5 x TCCS</p>

**Related Information**

- [PowerPlay Early Power Estimator User Guide](#)  
For more information about the EPE tool.
- [PowerPlay Power Analysis](#)  
For more information about PowerPlay power analysis.

**Power Consumption**

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus II PowerPlay Power Analyzer feature.

**Note:** You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

**Related Information**

- [PowerPlay Early Power Estimator User Guide](#)  
For more information about the EPE tool.
- [PowerPlay Power Analysis](#)  
For more information about PowerPlay power analysis.

**I/O Pin Leakage Current****Table 2-8: I/O Pin Leakage Current for Arria V GZ Devices**

If  $V_O = V_{CCIO}$  to  $V_{CCIO_{MAX}}$ , 100  $\mu A$  of leakage current per I/O is expected.

Symbol	Description	Conditions	Min	Typ	Max	Unit
$I_I$	Input pin	$V_I = 0\text{ V to }V_{CCIO_{MAX}}$	-30	—	30	$\mu A$
$I_{OZ}$	Tri-stated I/O pin	$V_O = 0\text{ V to }V_{CCIO_{MAX}}$	-30	—	30	$\mu A$

Symbol	Description	Conditions	Calibration Accuracy		Unit
			C3, I3L	C4, I4	
25-Ω R <sub>S</sub>	Internal series termination with calibration (25-Ω setting)	V <sub>CCIO</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%
50-Ω R <sub>S</sub>	Internal series termination with calibration (50-Ω setting)	V <sub>CCIO</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%
34-Ω and 40-Ω R <sub>S</sub>	Internal series termination with calibration (34-Ω and 40-Ω setting)	V <sub>CCIO</sub> = 1.5, 1.35, 1.25, 1.2 V	±15	±15	%
48-Ω, 60-Ω, 80-Ω, and 240-Ω R <sub>S</sub>	Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting)	V <sub>CCIO</sub> = 1.2 V	±15	±15	%
50-Ω R <sub>T</sub>	Internal parallel termination with calibration (50-Ω setting)	V <sub>CCIO</sub> = 2.5, 1.8, 1.5, 1.2 V	-10 to +40	-10 to +40	%
20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω R <sub>T</sub>	Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V <sub>CCIO</sub> = 1.5, 1.35, 1.25 V	-10 to +40	-10 to +40	%
60-Ω and 120-Ω R <sub>T</sub>	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V <sub>CCIO</sub> = 1.2	-10 to +40	-10 to +40	%
25-Ω R <sub>S_left_shift</sub>	Internal left shift series termination with calibration (25-Ω R <sub>S_left_shift</sub> setting)	V <sub>CCIO</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%

Table 2-11: OCT Without Calibration Resistance Tolerance Specifications for Arria V GZ Devices

Symbol	Description	Conditions	Resistance Tolerance		Unit
			C3, I3L	C4, I4	
25-Ω R, 50-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCIO</sub> = 3.0 and 2.5 V	±40	±40	%

I/O Standard	V <sub>CCIO</sub> (V)			V <sub>DIF(DC)</sub> (V)		V <sub>X(AC)</sub> (V)			V <sub>CM(DC)</sub> (V)			V <sub>DIF(AC)</sub> (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V <sub>CCIO</sub> + 0.3	—	0.5 × V <sub>CCIO</sub>	—	0.4 × V <sub>CCIO</sub>	0.5 × V <sub>CCIO</sub>	0.6 × V <sub>CCIO</sub>	0.3	V <sub>CCIO</sub> + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5 × V <sub>CCIO</sub> - 0.12	0.5 × V <sub>CCIO</sub>	0.5 × V <sub>CCIO</sub> + 0.12	0.4 × V <sub>CCIO</sub>	0.5 × V <sub>CCIO</sub>	0.6 × V <sub>CCIO</sub>	0.44	0.44

Table 2-21: Differential I/O Standard Specifications for Arria V GZ Devices

I/O Standard	V <sub>CCIO</sub> (V) <sup>(128)</sup>			V <sub>ID</sub> (mV) <sup>(129)</sup>			V <sub>ICM(DC)</sub> (V)			V <sub>OD</sub> (V) <sup>(130)</sup>			V <sub>OCM</sub> (V) <sup>(130)</sup>		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to the "Transceiver Performance Specifications" section.														
2.5 V LVDS <sup>(131)</sup>	2.375	2.5	2.625	100	V <sub>CM</sub> = 1.25 V	—	0.05	D <sub>MAX</sub> ≤ 700 Mbps	1.8	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	D <sub>MAX</sub> > 700 Mbps	1.55	0.247	—	0.6	1.125	1.25	1.375
BLVDS <sup>(132)</sup>	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—	—

<sup>(128)</sup> Differential inputs are powered by VCCPD which requires 2.5 V.

<sup>(129)</sup> The minimum V<sub>ID</sub> value is applicable over the entire common mode range, V<sub>CM</sub>.

<sup>(130)</sup> RL range: 90 ≤ RL ≤ 110 Ω.

<sup>(131)</sup> For optimized LVDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.

<sup>(132)</sup> There are no fixed V<sub>ICM</sub>, V<sub>OD</sub>, and V<sub>OCM</sub> specifications for BLVDS. They depend on the system topology.

Clock Network	ATX PLL			CMU PLL <sup>(161)</sup>			fPLL		
	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span
xN (PCIe)	—	8.0	8	—	5.0	8	—	—	—
xN (Native PHY IP)	8.0	8.0	Up to 13 channels above and below PLL	7.99	7.99	Up to 13 channels above and below PLL	3.125	3.125	Up to 13 channels above and below PLL
	—	8.01 to 9.8304	Up to 7 channels above and below PLL						

## Standard PCS Data Rate

**Table 2-30: Standard PCS Approximate Maximum Date Rate (Gbps) for Arria V GZ Devices**

The maximum data rate is also constrained by the transceiver speed grade. Refer to the “Commercial and Industrial Speed Grade Offering for Arria V GZ Devices” table for the transceiver speed grade.

Mode <sup>(164)</sup>	Transceiver Speed Grade	PMA Width	20	20	16	16	10	10	8	8
		PCS/Core Width	40	20	32	16	20	10	16	8
FIFO	2	C3, I3L core speed grade	9.9	9	7.84	7.2	5.3	4.7	4.24	3.76
	3	C4, I4 core speed grade	8.8	8.2	7.2	6.56	4.8	4.3	3.84	3.44

<sup>(161)</sup> ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

<sup>(164)</sup> The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
$t_{x \text{ Jitter}}$ - True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	UI
$t_{x \text{ Jitter}}$ - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	300	—	—	325	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.2	—	—	0.25	UI
$t_{DUTY}$	Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	%
$t_{RISE}$ & $t_{FALL}$	True Differential I/O Standards	—	—	200	—	—	200	ps
	Emulated Differential I/O Standards with three external output resistor networks	—	—	250	—	—	300	ps
TCCS	True Differential I/O Standards	—	—	150	—	—	150	ps
	Emulated Differential I/O Standards	—	—	300	—	—	300	ps

### Receiver High-Speed I/O Specifications

**Table 2-41: Receiver High-Speed I/O Specifications for Arria V GZ Devices**

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.



Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions <sup>(201)</sup>	Maximum
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
	01010101	8	32	640 data transitions

### Soft CDR Mode High-Speed I/O Specifications

**Table 2-44: High-Speed I/O Specifications for Arria V GZ Devices**

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Soft-CDR ppm tolerance	—	—	—	300	—	—	300	± ppm

<sup>(201)</sup> This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 2-4: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate  $\geq 1.25$  Gbps

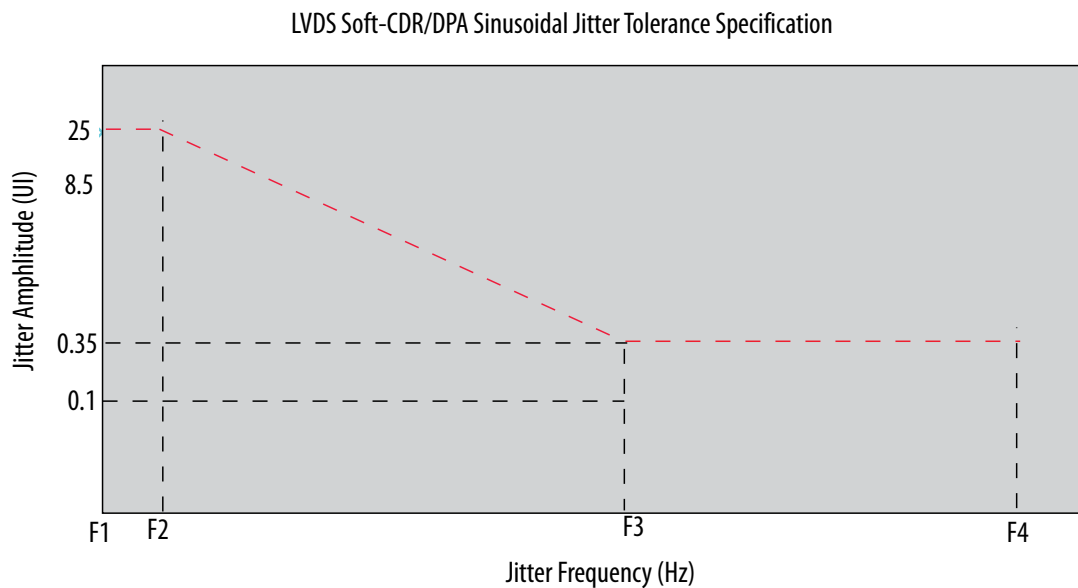


Table 2-45: LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate  $\geq 1.25$  Gbps

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Symbol	Parameter	Minimum	Maximum	Unit
$t_{CD2CU}$	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	—	—
$t_{CD2UMC}$	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (8576 \times \text{CLKUSR period})$ (209)	—	—

**Related Information**

- [DCLK-to-DATA\[\] Ratio \(r\) for FPP Configuration](#) on page 2-57
- [Configuration, Design Security, and Remote System Upgrades in Arria V Devices](#)

(208) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

(209) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the “Initialization” section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Table 2-62: Uncompressed .rbf Sizes for Arria V GZ Devices

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) <sup>(223)</sup>
Arria V GZ	E1	137,598,880	562,208
	E3	137,598,880	562,208
	E5	213,798,880	561,760
	E7	213,798,880	561,760

Table 2-63: Minimum Configuration Time Estimation for Arria V GZ Devices

Variant	Member Code	Active Serial <sup>(224)</sup>			Fast Passive Parallel <sup>(225)</sup>		
		Width	DCLK (MHz)	Min Config Time (ms)	Width	DCLK (MHz)	Min Config Time (ms)
Arria V GZ	E1	4	100	344	32	100	43
	E3	4	100	344	32	100	43
	E5	4	100	534	32	100	67
	E7	4	100	534	32	100	67

## Remote System Upgrades Circuitry Timing Specification

Table 2-64: Remote System Upgrade Circuitry Timing Specifications

Parameter	Minimum	Maximum	Unit
$t_{RU\_nCONFIG}$ <sup>(226)</sup>	250	—	ns
$t_{RU\_nRSTIMER}$ <sup>(227)</sup>	250	—	ns

<sup>(223)</sup> The IOCSR .rbf size is specifically for the Configuration via Protocol (CvP) feature.

<sup>(224)</sup> DCLK frequency of 100 MHz using external CLKUSR.

<sup>(225)</sup> Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Date	Version	Changes
July 2014	3.8	<ul style="list-style-type: none"> <li>Updated Table 21.</li> <li>Updated Table 22 <math>V_{OCM}</math> (DC Coupled) condition.</li> <li>Updated the DCLK note to Figure 6, Figure 7, and Figure 9.</li> <li>Added note to Table 5 and Table 6.</li> <li>Added the DCLK specification to Table 50.</li> <li>Added note to Table 51.</li> <li>Updated the list of parameters in Table 53.</li> </ul>
February 2014	3.7	Updated Table 28.
December 2013	3.6	<ul style="list-style-type: none"> <li>Updated Table 2, Table 13, Table 18, Table 19, Table 22, Table 30, Table 33, Table 37, Table 38, Table 45, Table 46, Table 47, Table 56, Table 49.</li> <li>Updated “PLL Specifications”.</li> </ul>
August 2013	3.5	Updated Table 28.
August 2013	3.4	<ul style="list-style-type: none"> <li>Removed Preliminary tags for Table 2, Table 4, Table 5, Table 14, Table 27, Table 28, Table 29, Table 31, Table 32, Table 43, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, and Table 54.</li> <li>Updated Table 2 and Table 28.</li> </ul>
June 2013	3.3	Updated Table 23, Table 28, Table 51, and Table 55.
May 2013	3.2	<ul style="list-style-type: none"> <li>Added Table 23.</li> <li>Updated Table 5, Table 22, Table 26, and Table 57.</li> <li>Updated Figure 6, Figure 7, Figure 8, and Figure 9.</li> </ul>
March 2013	3.1	<ul style="list-style-type: none"> <li>Updated Table 2, Table 6, Table 7, Table 8, Table 19, Table 22, Table 26, Table 29, Table 52.</li> <li>Updated “Maximum Allowed Overshoot and Undershoot Voltage”.</li> </ul>
December 2012	3.0	Initial release.