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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	14151
Number of Logic Elements/Cells	300000
Total RAM Bits	17358848
Number of I/O	704
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxfb1h4f40i5n

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
Vi (AC)	AC input voltage	3.8	100	%
		3.85	68	%
		3.9	45	%
		3.95	28	%
		4	15	%
		4.05	13	%
		4.1	11	%
		4.15	9	%
		4.2	8	%
		4.25	7	%
		4.3	5.4	%
		4.35	3.2	%
		4.4	1.9	%
		4.45	1.1	%
		4.5	0.6	%
		4.55	0.4	%
		4.6	0.2	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Arria V devices.

Recommended Operating Conditions

Table 1-3: Recommended Operating Conditions for Arria V Devices

This table lists the steady-state voltage values expected from Arria V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum(1)	Typical	Maximum(1)	Unit
V_{CCIO}	I/O buffers power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	1.283	1.35	1.418	V
		1.25 V	1.19	1.25	1.31	V
		1.2 V	1.14	1.2	1.26	V
V_{CCD_FPLL}	PLL digital voltage regulator power supply	—	1.425	1.5	1.575	V
V_{CCA_FPLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V_I	DC input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	–40	—	100	°C
t_{RAMP}(4)	Power supply ramp time	Standard POR	200 µs	—	100 ms	—
		Fast POR	200 µs	—	4 ms	—

(1) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(4) This is also applicable to HPS power supply. For HPS power supply, refer to t_{RAMP} specifications for standard POR when `HPS_PORSEL` = 0 and t_{RAMP} specifications for fast POR when `HPS_PORSEL` = 1.

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 1-15: Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-135 Class I, II	1.283	1.35	1.418	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-125 Class I, II	1.19	1.25	1.26	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}	—	V_{CCIO}/2	—
HSUL-12	1.14	1.2	1.3	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	—	—	—

Table 1-31: Transceiver-FPGA Fabric Interface Specifications for Arria V GT and ST Devices

Symbol/Description	Transceiver Speed Grade 3		Unit
	Min	Max	
Interface speed (PMA direct mode)	50	153.6[56], 161[57]	MHz
Interface speed (single-width mode)	25	187.5	MHz
Interface speed (double-width mode)	25	163.84	MHz

Related Information

- **CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain** on page 1-35
- **CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain** on page 1-36

[56] The maximum frequency when core transceiver local routing is selected.
[57] The maximum frequency when core transceiver network routing (GCLK, RCLK, or PCLK) is selected.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	–3 speed grade	5	—	800[61]	MHz
		–4 speed grade	5	—	800[61]	MHz
		–5 speed grade	5	—	750[61]	MHz
		–6 speed grade	5	—	625[61]	MHz
f_{INPFD}	Integer input clock frequency to the phase frequency detector (PFD)	—	5	—	325	MHz
f_{FINPFD}	Fractional input clock frequency to the PFD	—	50	—	160	MHz
f_{VCO}[62]	PLL voltage-controlled oscillator (VCO) operating range	–3 speed grade	600	—	1600	MHz
		–4 speed grade	600	—	1600	MHz
		–5 speed grade	600	—	1600	MHz
		–6 speed grade	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	—	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock	–3 speed grade	—	—	500[63]	MHz
		–4 speed grade	—	—	500[63]	MHz
		–5 speed grade	—	—	500[63]	MHz
		–6 speed grade	—	—	400[63]	MHz

(61) This specification is limited in the Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(62) The VCO frequency reported by the Quartus Prime software takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

(63) This specification is limited by the lower of the two: I/O f_{MAX} or F_{OUT} of the PLL.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{CASC\_OUTPJ\_DC}$ (67)(71)	Period jitter for dedicated clock output in cascaded PLLs	$F_{OUT} \geq 100$ MHz	—	—	175	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	17.5	mUI (p-p)
t_{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 µs	—	—	—	±10	%
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	8	24	32	bits
k_{VALUE}	Numerator of fraction	—	128	8388608	2147483648	—
f_{RES}	Resolution of VCO frequency	f_{INPFD} = 100 MHz	390625	5.96	0.023	Hz

Related Information

Memory Output Clock Jitter Specifications on page 1-57
Provides more information about the external memory interface clock output jitter specifications.

(71) The cascaded PLL specification is only applicable with the following conditions:
- Upstream PLL: 0.59 MHz ≤ Upstream PLL BW < 1 MHz
- Downstream PLL: Downstream PLL BW > 2 MHz

High-Speed I/O Specifications

Table 1-40: High-Speed I/O Specifications for Arria V Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block. When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

The Arria V devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 360 Mbps
- True mini-LVDS output standard with data rates of up to 400 Mbps

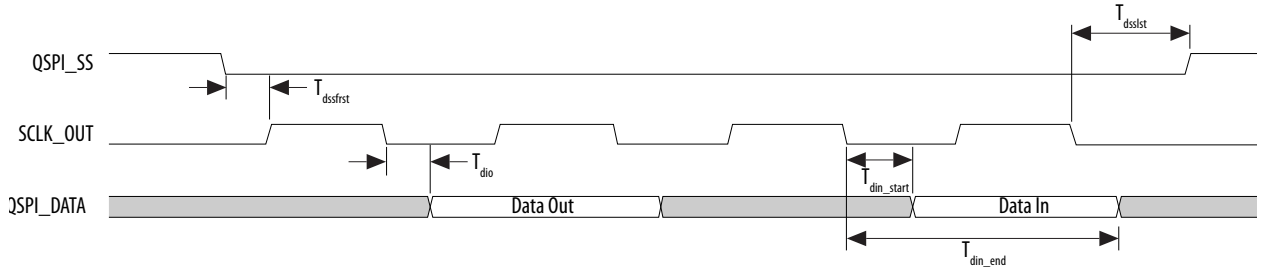
Symbol		Condition	–I3, –C4			–I5, –C5			–C6			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards		Clock boost factor W = 1 to 40[72]	5	—	800	5	—	750	5	—	625	MHz
f_{HSCLK_in} (input clock frequency) Single-Ended I/O Standards[73]		Clock boost factor W = 1 to 40[72]	5	—	625	5	—	625	5	—	500	MHz
f_{HSCLK_in} (input clock frequency) Single-Ended I/O Standards[74]		Clock boost factor W = 1 to 40[72]	5	—	420	5	—	420	5	—	420	MHz
f_{HSCLK_OUT} (output clock frequency)		—	5	—	625[75]	5	—	625[75]	5	—	500[75]	MHz
Transmitter	True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J =3 to 10[76]	[77]	—	1250	[77]	—	1250	[77]	—	1050	Mbps

[72] Clock boost factor (W) is the ratio between the input data rate and the input clock rate.
[73] This applies to DPA and soft-CDR modes only.
[74] This applies to non-DPA mode only.
[75] This is achieved by using the LVDS clock network.
[76] The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.
[77] The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

Symbol	Description	Min	Typ	Max	Unit
T_{din_end}	Input data valid end	$(2 + R_{delay}) \times T_{qspi\_clk} - 1.21$ (85)	—	—	ns

Figure 1-8: Quad SPI Flash Timing Diagram

This timing diagram illustrates clock polarity mode 0 and clock phase mode 0.



Related Information

Quad SPI Flash Controller Chapter, Arria V Hard Processor System Technical Reference Manual
Provides more information about Rdelay.

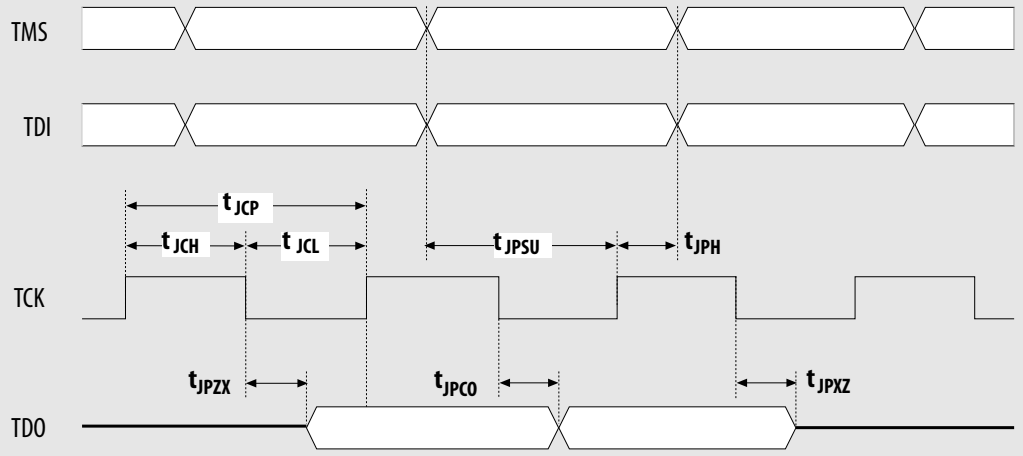
SPI Timing Characteristics

Table 1-52: SPI Master Timing Requirements for Arria V Devices

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

Symbol	Description	Min	Max	Unit
T_{clk}	CLK clock period	16.67	—	ns
T_{su}	SPI Master-in slave-out (MISO) setup time	8.35 (86)	—	ns

(85) R_{delay} is set by programming the register `qspiregs.rddatacap`. For the SoC EDS software version 13.1 and later, Altera provides automatic Quad SPI calibration in the preloader. For more information about R_{delay}, refer to the Quad SPI Flash Controller chapter in the Arria V Hard Processor System Technical Reference Manual.

Term	Definition
JTAG timing specifications	JTAG Timing Specifications 

Date	Version	Changes

December 2015	2015.12.16	• Updated Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices table.
		  • Updated F_{clk}, $T_{dutycycle}$, and $T_{dssfrst}$ specifications.
		  • Added T_{qspi_clk}, T_{din_start}, and T_{din_end} specifications.
		  • Removed T_{dinmax} specifications.
		• Updated the minimum specification for T_{clk} to 16.67 ns and removed the maximum specification in SPI Master Timing Requirements for Arria V Devices table.
		• Updated Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices table.
		  • Updated T_{clk} to $T_{sdmmc\_clk\_out}$ symbol.
		  • Updated $T_{sdmmc\_clk\_out}$ and T_{d} specifications.
		  • Added T_{sdmmc_clk}, T_{su}, and T_{h} specifications.
		  • Removed T_{dinmax} specifications.
		• Updated the following diagrams:
		  • Quad SPI Flash Timing Diagram
		  • SD/MMC Timing Diagram
		• Updated configuration .rbf sizes for Arria V devices.
		• Changed instances of *Quartus II* to *Quartus Prime*.

Symbol	Description	Conditions	Calibration Accuracy		Unit
			C3, I3L	C4, I4	
25-Ω R_S	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%
50-Ω R_S	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2 V	±15	±15	%
48-Ω, 60-Ω, 80-Ω, and 240-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting)	V_{CCIO} = 1.2 V	±15	±15	%
50-Ω R_T	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 2.5, 1.8, 1.5, 1.2 V	–10 to +40	–10 to +40	%
20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (20-Ω , 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25 V	–10 to +40	–10 to +40	%
60-Ω and 120-Ω R_T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V_{CCIO} = 1.2	–10 to +40	–10 to +40	%
25-Ω $R_{S\_left\_shift}$	Internal left shift series termination with calibration (25-Ω $R_{S\_left\_shift}$ setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%

Table 2-11: OCT Without Calibration Resistance Tolerance Specifications for Arria V GZ Devices

Symbol	Description	Conditions	Resistance Tolerance		Unit
			C3, I3L	C4, I4	
25-Ω R, 50-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.0 and 2.5 V	±40	±40	%

I/O Standard Specifications

The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

Table 2-16: Single-Ended I/O Standards for Arria V GZ Devices

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.4	2.4	2	–2
LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.6	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2

Table 2-17: Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V GZ Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × VCCIO	0.51 × V_{CCIO}

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Programmable DC gain	DC gain setting = 0	—	0	—	—	0	—	dB
	DC gain setting = 1	—	2	—	—	2	—	dB
	DC gain setting = 2	—	4	—	—	4	—	dB
	DC gain setting = 3	—	6	—	—	6	—	dB
	DC gain setting = 4	—	8	—	—	8	—	dB

Related Information

Arria V Device Overview
For more information about device ordering codes.

Transmitter

Table 2-25: Transmitter Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported I/O Standards	1.4-V and 1.5-V PCML							
Data rate (Standard PCS)	—	600	—	9900	600	—	8800	Mbps
Data rate (10G PCS)	—	600	—	12500	600	—	10312.5	Mbps

Clock Network	ATX PLL			CMU PLL [161]			fPLL		
	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span
xN (PCIe)	—	8.0	8	—	5.0	8	—	—	—
xN (Native PHY IP)	8.0	8.0	Up to 13 channels above and below PLL	7.99	7.99	Up to 13 channels above and below PLL	3.125	3.125	Up to 13 channels above and below PLL
	—	8.01 to 9.8304	Up to 7 channels above and below PLL						

Standard PCS Data Rate

Table 2-30: Standard PCS Approximate Maximum Date Rate (Gbps) for Arria V GZ Devices

The maximum data rate is also constrained by the transceiver speed grade. Refer to the "Commercial and Industrial Speed Grade Offering for Arria V GZ Devices" table for the transceiver speed grade.

Mode [164]	Transceiver Speed Grade	PMA Width	20	20	16	16	10	10	8	8
		PCS/Core Width	40	20	32	16	20	10	16	8
FIFO	2	C3, I3L core speed grade	9.9	9	7.84	7.2	5.3	4.7	4.24	3.76
	3	C4, I4 core speed grade	8.8	8.2	7.2	6.56	4.8	4.3	3.84	3.44

[161] ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

[164] The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 3 to 10 (192), (193), (194), (195), (196), (197)	150	—	1250	150	—	1050	Mbps
	SERDES factor J ≥ 4 LVDS RX with DPA (193), (195), (196), (197)	150	—	1600	150	—	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(198)	—	(199)	(198)	—	(199)	Mbps
	SERDES factor J = 1, uses SDR Register	(198)	—	(199)	(198)	—	(199)	Mbps
f_{HSDR} (data rate)	SERDES factor J = 3 to 10	(198)	—	(200)	(198)	—	(200)	Mbps
	SERDES factor J = 2, uses DDR Registers	(198)	—	(199)	(198)	—	(199)	Mbps
	SERDES factor J = 1, uses SDR Register	(198)	—	(199)	(198)	—	(199)	Mbps

(192) The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.
(193) Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.
(194) Arria V GZ LVDS serialization and de-serialization factor needs to be x4 and above.
(195) Requires package skew compensation with PCB trace length.
(196) Do not mix single-ended I/O buffer within LVDS I/O bank.
(197) Chip-to-chip communication only with a maximum load of 5 pF.
(198) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.
(199) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.
(200) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

Duty Cycle Distortion (DCD) Specifications

Table 2-52: Worst-Case DCD on Arria V GZ I/O Pins

The DCD numbers do not cover the core clock network.

Symbol	C3, I3L		C4, I4		Unit
	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	%

Configuration Specification

POR Specifications

Table 2-53: Fast and Standard POR Delay Specification for Arria V GZ Devices

Select the POR delay based on the MSEL setting as described in the "Configuration Schemes for Arria V Devices" table in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

POR Delay	Minimum (ms)	Maximum (ms)
Fast	4	12 (202)
Standard	100	300

Related Information

Configuration, Design Security, and Remote System Upgrades in Arria V Devices

(202) The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (8576 × CLKUSR period) (209)	—	—

Related Information

- **DCLK-to-DATA[] Ratio (r) for FPP Configuration** on page 2-57
- **Configuration, Design Security, and Remote System Upgrades in Arria V Devices**

(208) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

(209) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Table 2-62: Uncompressed .rbf Sizes for Arria V GZ Devices

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) (223)
Arria V GZ	E1	137,598,880	562,208
	E3	137,598,880	562,208
	E5	213,798,880	561,760
	E7	213,798,880	561,760

Table 2-63: Minimum Configuration Time Estimation for Arria V GZ Devices

Variant	Member Code	Active Serial (224)			Fast Passive Parallel (225)		
		Width	DCLK (MHz)	Min Config Time (ms)	Width	DCLK (MHz)	Min Config Time (ms)
Arria V GZ	E1	4	100	344	32	100	43
	E3	4	100	344	32	100	43
	E5	4	100	534	32	100	67
	E7	4	100	534	32	100	67

Remote System Upgrades Circuitry Timing Specification

Table 2-64: Remote System Upgrade Circuitry Timing Specifications

Parameter	Minimum	Maximum	Unit
$t_{RU\_nCONFIG}$ (226)	250	—	ns
$t_{RU\_nRSTIMER}$ (227)	250	—	ns

(223) The IOCSR **.rbf** size is specifically for the Configuration via Protocol (CvP) feature.
(224) DCLK frequency of 100 MHz using external CLKUSR.
(225) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Related Information

- **Configuration, Design Security, and Remote System Upgrades in Arria V Devices**
  For more information about the reconfiguration input for the ALTREMOTE_UPDATE IP core, refer to the "User Watchdog Timer" section.
- **Configuration, Design Security, and Remote System Upgrades in Arria V Devices**
  For more information about the `reset_timer` input for the ALTREMOTE_UPDATE IP core, refer to the "Remote System Upgrade State Machine" section.

User Watchdog Internal Oscillator Frequency Specification

Table 2-65: User Watchdog Internal Oscillator Frequency Specifications

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

Arria V Devices Documentation page
For the Excel-based I/O Timing spreadsheet

(226) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification. For more information, refer to the "Remote System Upgrade State Machine" section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

(227) This is equivalent to strobing the reset_timer input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification. For more information, refer to the "User Watchdog Timer" section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Term	Definition
V_{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
V_{SWING}	Differential input voltage
V_X	Input differential cross point voltage
V_{OX}	Output differential cross point voltage
W	High-speed I/O block—clock boost factor

Document Revision History

Date	Version	Changes
February 2017	2017.02.10	• Changed the minimum value for t_{CD2UMC} in the “FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1” table. • Changed the minimum value for t_{CD2UMC} in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1" table. • Changed the minimum value for t_{CD2UMC} in the "AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices" table. • Changed the minimum value for t_{CD2UMC} in the "PS Timing Parameters for Arria V GZ Devices" table. • Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices" table.