### Intel - 5AGXFB1H6F35C6N Datasheet





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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Details	
Product Status	Obsolete
Number of LABs/CLBs	14151
Number of Logic Elements/Cells	300000
Total RAM Bits	17358848
Number of I/O	544
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxfb1h6f35c6n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Symbol	Description	Minimum <sup>(5)</sup>	Typical	Maximum <sup>(5)</sup>	Unit
V <sub>CCL_GXBL</sub>	GX and SX speed grades—clock network power (left side)	1 08/1 12	1 1/1 15(6)	1 14/1 18	V
V <sub>CCL_GXBR</sub>	GX and SX speed grades—clock network power (right side)	1.00/ 1.12	1.1/1.13	1.14/1.10	v
V <sub>CCL_GXBL</sub>	GT and ST speed grades—clock network power (left side)	117	1 20	1 22	V
V <sub>CCL_GXBR</sub>	GT and ST speed grades—clock network power (right side)	1.17	1.20	1.23	v

#### **Related Information**

## Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines

Provides more information about the power supply connection for different data rates.

### **HPS Power Supply Operating Conditions**

### Table 1-5: HPS Power Supply Operating Conditions for Arria V SX and ST Devices

This table lists the steady-state voltage and current values expected from Arria V system-on-a-chip (SoC) devices with ARM®-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to Recommended Operating Conditions for Arria V Devices table for the steady-state voltage values expected from the FPGA portion of the Arria V SoC devices.

Symbol	Description	Condition	Minimum <sup>(7)</sup>	Typical	Maximum <sup>(7)</sup>	Unit
	HPS core	-C4, -I5, -C5, -C6	1.07	1.1	1.13	V
V <sub>CC_HPS</sub>	voltage and periphery circuitry power supply	-I3	1.12	1.15	1.18	V

<sup>&</sup>lt;sup>(5)</sup> The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.



<sup>&</sup>lt;sup>(7)</sup> The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

### I/O Pin Leakage Current

# Table 1-6: I/O Pin Leakage Current for Arria V Devices

Symbol	Description	Condition	Min	Тур	Max	Unit
II	Input pin	$V_{I} = 0 V$ to $V_{CCIOMAX}$	-30	—	30	μΑ
I <sub>OZ</sub>	Tri-stated I/O pin	$V_{O} = 0 V$ to $V_{CCIOMAX}$	-30		30	μΑ

## **Bus Hold Specifications**

### Table 1-7: Bus Hold Parameters for Arria V Devices

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

			V <sub>CCIO</sub> (V)												
Parameter	Symbol	Condition	1.	.2	1	.5	1	.8	2	.5	3.	.0	3	.3	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I <sub>SUSL</sub>	V <sub>IN</sub> > V <sub>IL</sub> (max)	8	_	12		30	_	50		70		70		μΑ
Bus-hold, high, sustaining current	I <sub>SUSH</sub>	V <sub>IN</sub> < V <sub>IH</sub> (min)	-8	_	-12		-30	_	-50		-70	_	-70		μΑ
Bus-hold, low, overdrive current	I <sub>ODL</sub>	$\begin{array}{c} 0 \ \mathrm{V} < \mathrm{V_{IN}} \\ < \mathrm{V_{CCIO}} \end{array}$		125	_	175	_	200		300		500	_	500	μΑ
Bus-hold, high, overdrive current	I <sub>ODH</sub>	0 V <v<sub>IN <v<sub>CCIO</v<sub></v<sub>	_	-125	_	-175	_	-200		-300	_	-500	_	-500	μΑ

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Symbol	Description	V <sub>CCIO</sub> (V)	Value	Unit
		3.0	0.189	
		2.5	0.208	
	OCT variation with temperature without recalibration	1.8	0.266	
dR/dT		1.5	0.273	%/°C
		1.35	0.200	
		1.25	0.200	
		1.2	0.317	

# **Pin Capacitance**

# Table 1-11: Pin Capacitance for Arria V Devices

Symbol	Description	Maximum	Unit
C <sub>IOTB</sub>	Input capacitance on top/bottom I/O pins	6	pF
C <sub>IOLR</sub>	Input capacitance on left/right I/O pins	6	pF
C <sub>OUTFB</sub>	Input capacitance on dual-purpose clock output/feedback pins	6	pF
C <sub>IOVREF</sub>	Input capacitance on V <sub>REF</sub> pins	48	pF

# **Hot Socketing**

# Table 1-12: Hot Socketing Specifications for Arria V Devices

Symbol	Description	Maximum	Unit
I <sub>IOPIN (DC)</sub>	DC current per I/O pin	300	μΑ
I <sub>IOPIN (AC)</sub>	AC current per I/O pin	8(10)	mA
I <sub>XCVR-TX (DC)</sub>	DC current per transceiver transmitter (TX) pin	100	mA

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For example, when  $V_{OD}$  = 800 mV, the corresponding  $V_{OD}$  value setting is 40. The following conditions show that the 1st post tap pre-emphasis setting = 2 is valid:

- $|B| + |C| \le 60 \Rightarrow 40 + 2 = 42$ ٠
- $|B| |C| > 5 \rightarrow 40 2 = 38$
- $(V_{MAX}/V_{MIN} 1)\% < 600\% \Rightarrow (42/38 1)\% = 10.52\%$

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Arria V HSSI HSPICE models.

## Table 1-33: Transmitter Pre-Emphasis Levels for Arria V Devices

Quartus Prime 1st	Quartus Prime V <sub>OD</sub> Setting							
Post Tap Pre- Emphasis Setting	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	Unit
0	0	0	0	0	0	0	0	dB
1	1.97	0.88	0.43	0.32	0.24	0.19	0.13	dB
2	3.58	1.67	0.95	0.76	0.61	0.5	0.41	dB
3	5.35	2.48	1.49	1.2	1	0.83	0.69	dB
4	7.27	3.31	2	1.63	1.36	1.14	0.96	dB
5	_	4.19	2.55	2.1	1.76	1.49	1.26	dB
6	_	5.08	3.11	2.56	2.17	1.83	1.56	dB
7	_	5.99	3.71	3.06	2.58	2.18	1.87	dB
8	_	6.92	4.22	3.47	2.93	2.48	2.11	dB
9	_	7.92	4.86	4	3.38	2.87	2.46	dB
10	_	9.04	5.46	4.51	3.79	3.23	2.77	dB
11	_	10.2	6.09	5.01	4.23	3.61	_	dB
12	_	11.56	6.74	5.51	4.68	3.97	_	dB
13	_	12.9	7.44	6.1	5.12	4.36	_	dB
14	_	14.44	8.12	6.64	5.57	4.76	_	dB
15	_	_	8.87	7.21	6.06	5.14	_	dB

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# Figure 1-15: MDIO Timing Diagram



# I<sup>2</sup>C Timing Characteristics

# Table 1-59: I<sup>2</sup>C Timing Requirements for Arria V Devices

Symbol	Description	Standar	d Mode	Fast l	Mode	Unit	
Symbol	Description	Min	Max	Min	Max	onic	
T <sub>clk</sub>	Serial clock (SCL) clock period	10	—	2.5		μs	
T <sub>clkhigh</sub>	SCL high time	4.7	—	0.6		μs	
T <sub>clklow</sub>	SCL low time	4	—	1.3		μs	
T <sub>s</sub>	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1		μs	
T <sub>h</sub>	Hold time for SCL to SDA data	0	3.45	0	0.9	μs	
T <sub>d</sub>	SCL to SDA output data delay	—	0.2		0.2	μs	
T <sub>su_start</sub>	Setup time for a repeated start condition	4.7	_	0.6		μs	
T <sub>hd_start</sub>	Hold time for a repeated start condition	4	_	0.6		μs	
T <sub>su_stop</sub>	Setup time for a stop condition	4	_	0.6	_	μs	



Symbol	Description	Min	Max	Unit
$T_{dh}^{(89)}$	Data to write enable hold time	5	—	ns
T <sub>cea</sub>	Chip enable to data access time		25	ns
T <sub>rea</sub>	Read enable to data access time		16	ns
T <sub>rhz</sub>	Read enable to data high impedance		100	ns
T <sub>rr</sub>	Ready to read enable low	20	—	ns

# Figure 1-17: NAND Command Latch Timing Diagram





Symbol	Parameter	Minimum	Maximum	Unit
t <sub>STATUS</sub>	nSTATUS low pulse width	268	1506 <sup>(94)</sup>	μs
t <sub>CF2ST1</sub>	nCONFIG high to nSTATUS high	—	1506 <sup>(95)</sup>	μs
t <sub>CF2CK</sub> <sup>(96)</sup>	nCONFIG high to first rising edge on DCLK	1506	—	μs
t <sub>ST2CK</sub> <sup>(96)</sup>	nSTATUS high to first rising edge of DCLK	2		μs
t <sub>DSU</sub>	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t <sub>DH</sub>	DATA[] hold time after rising edge on DCLK	0		ns
t <sub>CH</sub>	DCLK high time	$0.45  imes 1/f_{MAX}$	—	S
t <sub>CL</sub>	DCLK low time	$0.45  imes 1/f_{ m MAX}$	—	S
t <sub>CLK</sub>	DCLK period	1/f <sub>MAX</sub>	—	S
f <sub>MAX</sub>	DCLK frequency (FPP ×8/ ×16)	_	125	MHz
t <sub>CD2UM</sub>	CONF_DONE high to user mode <sup>(97)</sup>	175	437	μs
t <sub>CD2CU</sub>	CONF_DONE high to CLKUSR enabled	4× maximum DCLK period	_	_
t <sub>CD2UMC</sub>	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU}$ + ( $T_{init} \times CLKUSR$ period)	_	_
T <sub>init</sub>	Number of clock cycles required for device initialization	8,576	_	Cycles

### **Related Information**

### **FPP Configuration Timing**

Provides the FPP configuration timing waveforms.



<sup>&</sup>lt;sup>(94)</sup> You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.

<sup>&</sup>lt;sup>(95)</sup> You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

<sup>&</sup>lt;sup>(96)</sup> If nSTATUS is monitored, follow the t<sub>ST2CK</sub> specification. If nSTATUS is not monitored, follow the t<sub>CF2CK</sub> specification.

<sup>&</sup>lt;sup>(97)</sup> The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

# FPP Configuration Timing when DCLK-to-DATA[] >1

### Table 1-67: FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
t <sub>CF2CD</sub>	nCONFIG low to CONF_DONE low	_	600	ns
t <sub>CF2ST0</sub>	nconfig low to nstatus low	—	600	ns
t <sub>CFG</sub>	nCONFIG low pulse width	2		μs
t <sub>STATUS</sub>	nSTATUS low pulse width	268	1506 <sup>(98)</sup>	μs
t <sub>CF2ST1</sub>	nCONFIG high to nSTATUS high	_	1506 <sup>(99)</sup>	μs
t <sub>CF2CK</sub> <sup>(100)</sup>	nCONFIG high to first rising edge on DCLK	1506	_	μs
t <sub>ST2CK</sub> <sup>(100)</sup>	nSTATUS high to first rising edge of DCLK	2		μs
t <sub>DSU</sub>	DATA[] setup time before rising edge on DCLK	5.5	_	ns
t <sub>DH</sub>	DATA[] hold time after rising edge on DCLK	$N - 1/f_{\rm DCLK}^{(101)}$		S
t <sub>CH</sub>	DCLK high time	$0.45  imes 1/f_{MAX}$		S
t <sub>CL</sub>	DCLK low time	$0.45  imes 1/f_{ m MAX}$		S
t <sub>CLK</sub>	DCLK period	1/f <sub>MAX</sub>		S
f <sub>MAX</sub>	DCLK frequency (FPP ×8/ ×16)	_	125	MHz
t <sub>R</sub>	Input rise time	—	40	ns
t <sub>F</sub>	Input fall time	_	40	ns
t <sub>CD2UM</sub>	CONF_DONE high to user mode <sup>(102)</sup>	175	437	μs

<sup>(98)</sup> This value can be obtained if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.



<sup>&</sup>lt;sup>(99)</sup> This value can be obtained if you do not delay configuration by externally holding nSTATUS low.

 $<sup>^{(100)}</sup>$  If nSTATUS is monitored, follow the  $t_{ST2CK}$  specification. If nSTATUS is not monitored, follow the  $t_{CF2CK}$  specification.

<sup>&</sup>lt;sup>(101)</sup> N is the DCLK-to-DATA[] ratio and  $f_{DCLK}$  is the DCLK frequency of the system.

<sup>&</sup>lt;sup>(102)</sup> The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

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	Symbol	Parameter	Typical	Unit
		Rising and/or falling edge delay	0 (default)	ps
D <sub>OUTBUF</sub>	50		ps	
	100		ps	
	150		ps	

# Glossary

# Table 1-78: Glossary

Term	Definition	
Differential I/O standards	Receiver Input Waveforms	
	Single-Ended Waveform	Positive Channel (p) = $V_{IH}$ Negative Channel (n) = $V_{IL}$
		Ground
	Differential Waveform	
		p - n = 0 V



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This document covers the electrical and switching characteristics for Arria V GZ devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, core, and periphery performance. This document also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

#### **Related Information**

#### Arria V Device Overview

For information regarding the densities and packages of devices in the Arria V GZ family.

# **Electrical Characteristics**

# **Operating Conditions**

When you use Arria V GZ devices, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Arria V GZ devices, you must consider the operating requirements described in this datasheet.

Arria V GZ devices are offered in commercial and industrial temperature grades.

Commercial devices are offered in -3 (fastest) and -4 core speed grades. Industrial devices are offered in -3L and -4 core speed grades. Arria V GZ devices are offered in -2 and -3 transceiver speed grades.

#### Table 2-1: Commercial and Industrial Speed Grade Offering for Arria V GZ Devices

C = Commercial temperature grade; I = Industrial temperature grade.

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# **Switching Characteristics**

# **Transceiver Performance Specifications**

# **Reference Clock**

## Table 2-22: Reference Clock Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
Symbol/Description	Conditions	Min	Тур	Мах	Min	Тур	Мах	Unit
Reference Clock								
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCM and HCSL	L, 1.4-V PC	ML, 1.5-V P	CML, 2.5-V	PCML, Di	fferential LV	PECL, LVDS,
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS						
Input Reference Clock Frequency (CMU PLL) <sup>(137)</sup>	_	40		710	40		710	MHz
Input Reference Clock Frequency (ATX PLL) <sup>(137)</sup>	-	100		710	100		710	MHz

<sup>(137)</sup> The input reference clock frequency options depend on the data rate and the device speed grade.



2-28	Transmitter
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Sumbol/Description	Conditions Transceiver Speed Grade 2 Transceiver Speed Grade 3		sceiver Speed Grade 3		Unit			
Symbol/Description	Conditions	Min	Тур	Мах	Min	Тур	Max	
Differential on-chip termination resistors	85- $\Omega$ setting	—	85 ± 20%	_	_	85 ± 20%	—	Ω
	100- $\Omega$ setting		100 ± 20%			100 ± 20%	_	Ω
	120- $\Omega$ setting	—	120 ± 20%			120 ± 20%	_	Ω
	150-Ω setting	_	150 ± 20%			150 ± 20%	_	Ω
V <sub>OCM</sub> (AC coupled)	0.65-V setting	—	650			650	_	mV
V <sub>OCM</sub> (DC coupled)	_	—	650			650	—	mV
Intra-differential pair skew	Tx V <sub>CM</sub> = 0.5 V and slew rate of 15 ps	—		15	_	_	15	ps
Intra-transceiver block transmitter channel-to-channel skew	x6 PMA bonded mode			120			120	ps
Inter-transceiver block transmitter channel-to-channel skew	xN PMA bonded mode			500			500	ps

### **Related Information**

## Arria V Device Overview

For more information about device ordering codes.



## Figure 2-2: AC Gain Curves for Arria V GZ Channels (full bandwidth)







Symbol	Parameter	Min	Тур	Мах	Unit
t <sub>OUTPJ_IO</sub> <sup>, (173)</sup> , <sup>(175)</sup>	Period Jitter for a clock output on a regular I/O in integer PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	600	ps (p-p)
	Period Jitter for a clock output on a regular I/O in integer PLL ( $f_{OUT} < 100 \text{ MHz}$ )	_		60	mUI (p-p)
t (173) (175) (176)	Period Jitter for a clock output on a regular I/O in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )	—		600	ps (p-p)
lFOUTPJ_IO	Period Jitter for a clock output on a regular I/O in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60	mUI (p-p)
t <sub>OUTCCJ_IO</sub> <sup>(173)</sup> , <sup>(175)</sup>	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	600	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL (f <sub>OUT</sub> < 100 MHz)	_		60	mUI (p-p)
t (173) (175) (176)	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )	—		600	ps (p-p)
<sup>I</sup> FOUTCCJ_IO	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60	mUI (p-p)
. (173) (177)	Period Jitter for a dedicated clock output in cascaded PLLs ( $f_{OUT} \ge 100 \text{ MHz}$ )			175	ps (p-p)
CASC_OUTPJ_DC	Period Jitter for a dedicated clock output in cascaded PLLS (f <sub>OUT</sub> < 100 MHz)			17.5	mUI (p-p)
dK <sub>BIT</sub>	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits

<sup>(175)</sup> The external memory interface clock output jitter specifications use a different measurement method, which is available in the "Memory Output Clock Jitter Specification for Arria V GZ Devices" table.

<sup>(176)</sup> This specification only covered fractional PLL for low bandwidth. The  $f_{VCO}$  for fractional value range 0.05–0.95 must be  $\geq$  1000 MHz.

<sup>(177)</sup> The cascaded PLL specification is only applicable with the following condition:



a. Upstream PLL: 0.59Mhz ≤ Upstream PLL BW < 1 MHz

b. Downstream PLL: Downstream PLL BW > 2 MHz

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Symbol	Conditions	C3, I3L			C4, I4			Unit
Symbol	Conditions	Min	Тур	Мах	Min	Тур	Max	Onic
f <sub>HSCLK_in</sub> (input clock frequency) True Differential I/O Standards <sup>(179)</sup>	Clock boost factor W = 1 to 40 $^{(180)}$	5	_	625	5	_	525	MHz
f <sub>HSCLK_in</sub> (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 $^{(180)}$	5		625	5		525	MHz
f <sub>HSCLK_in</sub> (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 $^{(180)}$	5		420	5		420	MHz
f <sub>HSCLK_OUT</sub> (output clock frequency)	—	5		625 (181)	5		525 (181)	MHz

### Transmitter High-Speed I/O Specifications

## Table 2-40: Transmitter High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.



 $<sup>^{(179)}\,</sup>$  This only applies to DPA and soft-CDR modes.

<sup>&</sup>lt;sup>(180)</sup> Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.

<sup>&</sup>lt;sup>(181)</sup> This is achieved by using the LVDS clock network.

## **DLL Range Specifications**

#### Table 2-47: DLL Range Specifications for Arria V GZ Devices

Arria V GZ devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Parameter	C3, I3L	C4, I4	Unit
DLL operating frequency range	300 - 890	300 - 890	MHz

## **DQS Logic Block Specifications**

#### Table 2-48: DQS Phase Offset Delay Per Setting for Arria V GZ Devices

The typical value equals the average of the minimum and maximum values.

The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a -3 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is  $[625 \text{ ps} + (10 \times 11 \text{ ps}) \pm 20 \text{ ps}] = 735 \text{ ps} \pm 20 \text{ ps}$ .

Speed Grade	Min	Мах	Unit
C3, I3L	8	15	ps
C4, I4	8	16	ps

## Table 2-49: DQS Phase Shift Error Specification for DLL-Delayed Clock (t<sub>DQS\_PSERR</sub>) for Arria V GZ Devices

This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a -3 speed grade is  $\pm 84$  ps or  $\pm 42$  ps.

Number of DQS Delay Buffers	C3, I3L	C4, I4	Unit
1	30	32	ps
2	60	64	ps
3	90	96	ps

# **JTAG Configuration Specifications**

Table 2-54: JTAG Timing Parameters and Values for Arria V GZ Devices	;
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Symbol	Description	Min	Мах	Unit
t <sub>JCP</sub>	TCK clock period	30		ns
t <sub>JCP</sub>	TCK clock period	167 (203)		ns
t <sub>JCH</sub>	TCK clock high time	14		ns
t <sub>JCL</sub>	TCK clock low time	14		ns
t <sub>JPSU (TDI)</sub>	TDI JTAG port setup time	2		ns
t <sub>JPSU (TMS)</sub>	TMS JTAG port setup time	3		ns
t <sub>JPH</sub>	JTAG port hold time	5		ns
t <sub>JPCO</sub>	JTAG port clock to output	_	11 (204)	ns
t <sub>JPZX</sub>	JTAG port high impedance to valid output		14 (204)	ns
t <sub>JPXZ</sub>	JTAG port valid output to high impedance	_	14 (204)	ns

# Fast Passive Parallel (FPP) Configuration Timing

# DCLK-to-DATA[] Ratio (r) for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Arria V GZ Device Datasheet



<sup>&</sup>lt;sup>(203)</sup> The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

<sup>(204)</sup> A 1-ns adder is required for each  $V_{CCIO}$  voltage step down from 3.0 V. For example,  $t_{IPCO} = 12$  ns if  $V_{CCIO}$  of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

# FPP Configuration Timing when DCLK to DATA[] > 1

### Figure 2-8: FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1,

t<sub>CF2ST1</sub> tcfg ;↔ nCONFIG ŤĊF2CK nSTATUS (3) 🕳 tstatus tCF2ST0 CONF\_DONE (4) TCL tCH tsT2CK ŤĊF2CD (8) DCLK (6) (7) 1 2 ••• r 2 ••• r 1  $\mathbf{D}$ (5) tCLK DATA[31..0] (8) Word 0 Word User Mode Word 3 • • • Word (n-1) tDH tDH tpsy High-Z User I/O User Mode INIT DONE (9) tCD2UM

Timing when using a MAX II device, MAX V device, or microprocessor as an external host.

#### Notes:

- 1. To find out the DCLK-to-DATA[] ratio for your system, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
- 2. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF\_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- 3. After power-up, the Arria V GZ device holds nSTATUS low for the time as specified by the POR delay.
- 4. After power-up, before and during configuration, CONF\_DONE is low.
- 5. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- 6. "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
- 7. If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31.0] pins prior to sending the first DCLK rising edge.
- 8. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF\_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF\_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- 9. After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT\_DONE goes low.





Term				Definition			
R <sub>L</sub>	Receiver differential input discrete resistor (external to the Arria V GZ device).						
SW (sampling window)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:						
	Bit Time						
		0.5 x TCCS	RSKM	Sampling Window (SW)	RSKM	0.5 x TCCS	
Single-ended voltage referenced I/O standard	The JEDEC standard for SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing: Single-Ended Voltage Referenced I/O Standard						
		V <sub>0H</sub>		V REF	Viн(DC Vil(DC)	V <u>ccio</u> VIH(AC) VIL(AC) VIL(AC)	



Term	Definition
V <sub>OCM</sub>	Output common mode voltage—The common mode of the differential signal at the transmitter.
V <sub>OD</sub>	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
V <sub>SWING</sub>	Differential input voltage
V <sub>X</sub>	Input differential cross point voltage
V <sub>OX</sub>	Output differential cross point voltage
W	High-speed I/O block—clock boost factor

# **Document Revision History**

Date	Version	Changes
February 2017	2017.02.10	<ul> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1" table.</li> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK to DATA[] Ratio is 1" table.</li> </ul>
		<ul> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices" table.</li> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "PS Timing Parameters for Arria V GZ Devices" table.</li> <li>Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices" table.</li> </ul>

