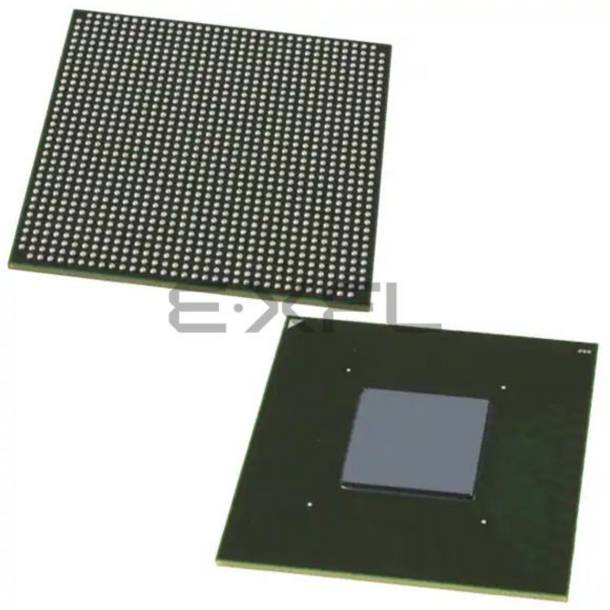

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

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Details	
Product Status	Obsolete
Number of LABs/CLBs	17110
Number of Logic Elements/Cells	362000
Total RAM Bits	19822592
Number of I/O	544
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxfb3h4f35i5

Caution: Conditions outside the range listed in the following table may cause permanent damage tothe device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1-1: Absolute Maximum Ratings for Arria V Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Core voltage power supply	–0.50	1.43	V
V_{CCP}	Periphery circuitry, PCIe® hardIP block, and transceiver physical coding sublayer (PCS) power supply	–0.50	1.43	V
V_{CCPGM}	Configuration pins power supply	–0.50	3.90	V
V_{CC_AUX}	Auxiliary supply	–0.50	3.25	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	–0.50	3.90	V
V_{CCPD}	I/O pre-driver power supply	–0.50	3.90	V
V_{CCIO}	I/O power supply	–0.50	3.90	V
V_{CCD_FPLL}	Phase-locked loop (PLL) digital power supply	–0.50	1.80	V
V_{CCA_FPLL}	PLL analog power supply	–0.50	3.25	V
V_{CCA_GXB}	Transceiver high voltage power	–0.50	3.25	V
V_{CCH_GXB}	Transmitter output buffer power	–0.50	1.80	V
V_{CCR_GXB}	Receiver power	–0.50	1.50	V
V_{CCT_GXB}	Transmitter power	–0.50	1.50	V
V_{CCL_GXB}	Transceiver clock network power	–0.50	1.50	V
V_I	DC input voltage	–0.50	3.80	V
V_{CC_HPS}	HPS core voltage and periphery circuitry power supply	–0.50	1.43	V
V_{CCPD_HPS}	HPS I/O pre-driver power supply	–0.50	3.90	V
V_{CCIO_HPS}	HPS I/O power supply	–0.50	3.90	V
$V_{CCRSTCLK\_HPS}$	HPS reset and clock input pins power supply	–0.50	3.90	V

Symbol	Description	Minimum	Maximum	Unit
V_{CCPLL_HPS}	HPS PLL analog power supply	–0.50	3.25	V
$V_{CC\_AUX\_SHARED}$	HPS auxiliary power supply	–0.50	3.25	V
I_{OUT}	DC output current per pin	–25	40	mA
T_J	Operating junction temperature	–55	125	°C
T_{STG}	Storage temperature (no bias)	–65	150	°C

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 4.00 V can only be at 4.00 V for ~15% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 1.5 years.

Table 1-2: Maximum Allowed Overshoot During Transitions for Arria V Devices

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

Table 1-16: Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Arria V Devices

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL}[14] (mA)	I_{OH}[14] (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	V_{TT} – 0.608	V_{TT} + 0.608	8.1	–8.1
SSTL-2 Class II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
SSTL-18 Class I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	V_{TT} – 0.603	V_{TT} + 0.603	6.7	–6.7
SSTL-18 Class II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} – 0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	16	–16
SSTL-135	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
SSTL-125	—	V_{REF} – 0.85	V_{REF} + 0.85	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
HSTL-18 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8

[14] To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL} [14] (mA)	I_{OH} [14] (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
HSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	–16
HSTL-12 Class I	–0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	8	–8
HSTL-12 Class II	–0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	16	–16
HSUL-12	—	$V_{REF} - 0.13$	$V_{REF} + 0.13$	—	$V_{REF} - 0.22$	$V_{REF} + 0.22$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	—	—

Differential SSTL I/O Standards

Table 1-17: Differential SSTL I/O Standards for Arria V Devices

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.62	$V_{CCIO} + 0.6$
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	$V_{CCIO} + 0.6$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	[15]	$V_{CCIO}/2 - 0.15$	—	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$
SSTL-135	1.283	1.35	1.45	0.18	[15]	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$

(14) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

(15) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Table 1-21: Transceiver Clocks Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
`fixedclk` clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	MHz
Transceiver Reconfiguration Controller IP (`mgmt_clk_clk`) clock frequency	—	75	—	125	75	—	125	MHz

Table 1-22: Receiver Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported I/O standards	1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS							
Data rate[28]	—	611	—	6553.6	611	—	3125	Mbps
Absolute V_{MAX} for a receiver pin[29]	—	—	—	1.2	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	–0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	—	—	—	2.2	—	—	2.2	V

(28) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.
(29) The device cannot tolerate prolonged operation at this absolute maximum.

Quartus Prime 1st Post Tap Pre-Emphasis Setting	Quartus Prime V_{OD} Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
16	—	—	9.56	7.73	6.49	—	—	dB
17	—	—	10.43	8.39	7.02	—	—	dB
18	—	—	11.23	9.03	7.52	—	—	dB
19	—	—	12.18	9.7	8.02	—	—	dB
20	—	—	13.17	10.34	8.59	—	—	dB
21	—	—	14.2	11.1	—	—	—	dB
22	—	—	15.38	11.87	—	—	—	dB
23	—	—	—	12.67	—	—	—	dB
24	—	—	—	13.48	—	—	—	dB
25	—	—	—	14.37	—	—	—	dB
26	—	—	—	—	—	—	—	dB
27	—	—	—	—	—	—	—	dB
28	—	—	—	—	—	—	—	dB
29	—	—	—	—	—	—	—	dB
30	—	—	—	—	—	—	—	dB
31	—	—	—	—	—	—	—	dB

Related Information

SPICE Models for Altera Devices

Provides the Arria V HSSI HSPICE models.

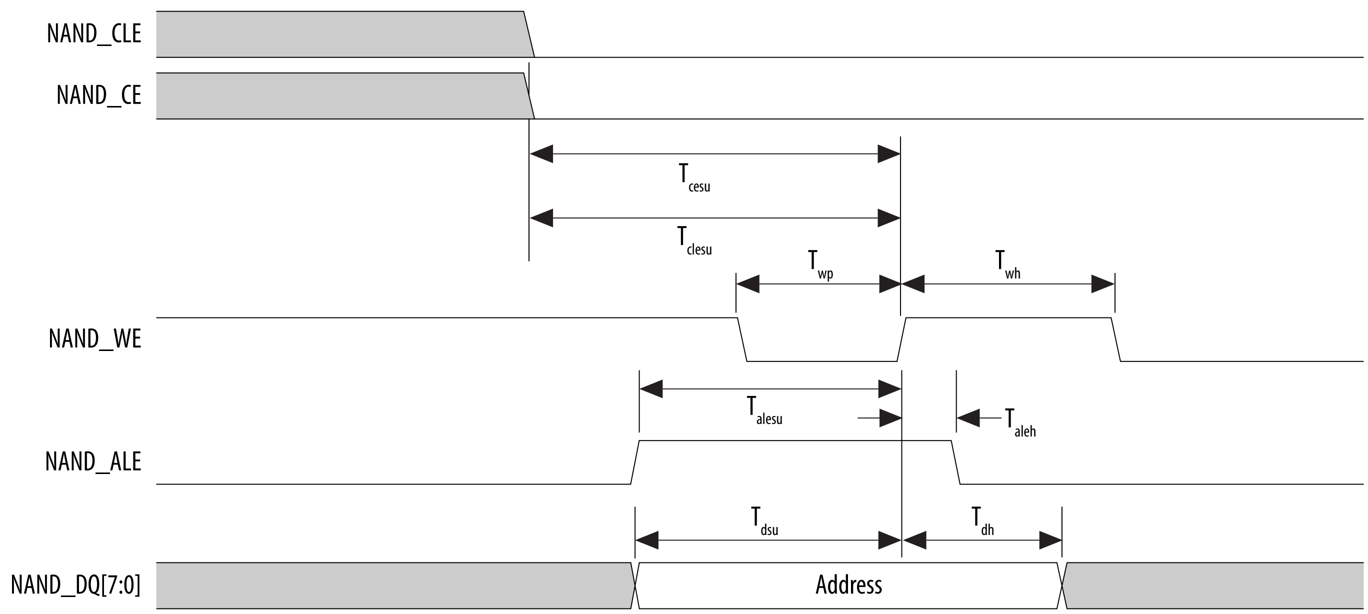
Transceiver Compliance Specification

The following table lists the physical medium attachment (PMA) specification compliance of all supported protocol for Arria V GX, GT, SX, and ST devices. For more information about the protocol parameter details and compliance specifications, contact your Altera Sales Representative.

Symbol	Condition	–I3, –C4			–I5, –C5			–C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	SERDES factor J ≥ 8(76)(78), LVDS TX with RX DPA	(77)	—	1600	(77)	—	1500	(77)	—	1250	Mbps
	SERDES factor J = 1 to 2, Uses DDR Registers	(77)	—	(79)	(77)	—	(79)	(77)	—	(79)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Network - f_{HSDR} (data rate)(80)	SERDES factor J = 4 to 10(81)	(77)	—	945	(77)	—	945	(77)	—	945	Mbps
Emulated Differential I/O Standards with One External Output Resistor Network - f_{HSDR} (data rate)(80)	SERDES factor J = 4 to 10(81)	(77)	—	200	(77)	—	200	(77)	—	200	Mbps
$t_{x\ Jitter}$ -True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps – 1.25 Gbps	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	UI

(78) The V_{CC} and V_{CCP} must be on a separate power layer and a maximum load of 5 pF for chip-to-chip interface.
(79) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}), provided you can close the design timing and the signal integrity simulation is clean.
(80) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.
(81) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

Figure 1-18: NAND Address Latch Timing Diagram



Term	Definition
t_{FALL}	Signal high-to-low transition time (80–20%)
t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input
t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL
t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL
t_{RISE}	Signal low-to-high transition time (20–80%)
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w)
$V_{CM(DC)}$	DC common mode input voltage.
V_{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.
V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
$V_{IH(AC)}$	High-level AC input voltage
$V_{IH(DC)}$	High-level DC input voltage
V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{IL(AC)}$	Low-level AC input voltage
$V_{IL(DC)}$	Low-level DC input voltage
V_{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter.
V_{SWING}	Differential input voltage
V_X	Input differential cross point voltage

Date	Version	Changes

June 2015	2015.06.16	• Added the supported data rates for the following output standards using true LVDS output buffer types in the High-Speed I/O Specifications for Arria V Devices table:
		  • True RSDS output standard: data rates of up to 360 Mbps
		  • True mini-LVDS output standard: data rates of up to 400 Mbps
		• Added note in the condition for Transmitter—Emulated Differential I/O Standards f_{HSDR} data rate parameter in the High-Speed I/O Specifications for Arria V Devices table. Note: When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.
		• Changed Queued Serial Peripheral Interface (QSPI) to Quad Serial Peripheral Interface (SPI) Flash.
		• Updated T_h location in I^2C Timing Diagram.
		• Updared T_{wp} location in NAND Address Latch Timing Diagram.
		• Corrected the unit for t_{DH} from ns to s in FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices table.
		• Updated the maximum value for t_{CO} from 4 ns to 2 ns in AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices table.
		• Moved the following timing diagrams to the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.
		  • FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is 1
		  • FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is >1
		  • AS Configuration Timing Waveform
		  • PS Configuration Timing Waveform

Symbol	Description	Minimum [118]	Typical	Maximum[118]	Unit
V_{CCR_GXBL} [121]	Receiver analog power supply (left side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
V_{CCR_GXBR} [121]	Receiver analog power supply (right side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
V_{CCT_GXBL} [121]	Transmitter analog power supply (left side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
V_{CCT_GXBR} [121]	Transmitter analog power supply (right side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
V_{CCH_GXBL}	Transmitter output buffer power supply (left side)	1.425	1.5	1.575	V
V_{CCH_GXBR}	Transmitter output buffer power supply (right side)	1.425	1.5	1.575	V

(118) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(121) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rate up to 6.5 Gbps, you can connect this supply to 0.85 V.

Symbol	Description	Conditions	Calibration Accuracy		Unit
			C3, I3L	C4, I4	
25-Ω R_S	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%
50-Ω R_S	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2 V	±15	±15	%
48-Ω, 60-Ω, 80-Ω, and 240-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting)	V_{CCIO} = 1.2 V	±15	±15	%
50-Ω R_T	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 2.5, 1.8, 1.5, 1.2 V	−10 to +40	−10 to +40	%
20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (20-Ω , 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25 V	−10 to +40	−10 to +40	%
60-Ω and 120-Ω R_T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V_{CCIO} = 1.2	−10 to +40	−10 to +40	%
25-Ω $R_{S\_left\_shift}$	Internal left shift series termination with calibration (25-Ω $R_{S\_left\_shift}$ setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%

Table 2-11: OCT Without Calibration Resistance Tolerance Specifications for Arria V GZ Devices

Symbol	Description	Conditions	Resistance Tolerance		Unit
			C3, I3L	C4, I4	
25-Ω R, 50-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.0 and 2.5 V	±40	±40	%

Hot Socketing

Table 2-14: Hot Socketing Specifications for Arria V GZ Devices

Symbol	Description	Maximum
$I_{IOPIN (DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN (AC)}$	AC current per I/O pin	8 mA [124]
$I_{XCVR\text{-}TX (DC)}$	DC current per transceiver transmitter pin	100 mA
$I_{XCVR\text{-}RX (DC)}$	DC current per transceiver receiver pin	50 mA

Internal Weak Pull-Up Resistor

Table 2-15: Internal Weak Pull-Up Resistor for Arria V GZ Devices

All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins. The internal weak pull-down feature is only available for the JTAG `TCK` pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ .

Symbol	Description	V_{CCIO} Conditions (V) [125]	Value [126]	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option.	3.0 ±5%	25	k Ω
		2.5 ±5%	25	k Ω
		1.8 ±5%	25	k Ω
		1.5 ±5%	25	kΩ
		1.35 ±5%	25	k Ω
		1.25 ±5%	25	k Ω
		1.2 ±5%	25	k Ω

(124) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}|$ = C dv/dt, in which C is the I/O pin capacitance and dv/dt is the slew rate.
(125) The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
(126) These specifications are valid with a ±10% tolerance to cover changes over PVT.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported data range	—	600	—	3250/ 3125[158]	600	—	3250/ 3125 [158]	Mbps
$t_{pll\_powerdown}$[159]	—	1	—	—	1	—	—	µs
t_{pll_lock} [160]	—	—	—	10		—	10	µs

Related Information

Arria V Device Overview

For more information about device ordering codes.

Clock Network Data Rate

Table 2-29: Clock Network Maximum Data Rate Transmitter Specifications

Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.

Clock Network	ATX PLL			CMU PLL [161]			fPLL		
	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span
x1 [162]	12.5	—	6	12.5	—	6	3.125	—	3
x6 [162]	—	12.5	6	—	12.5	6	—	3.125	6
x6 PLL Feedback [163]	—	12.5	Side-wide	—	12.5	Side-wide	—	—	—

(158) When you use fPLL as a TXPLL of the transceiver.
(159) $t_{pll\_powerdown}$ is the PLL powerdown minimum pulse width.
(160) t_{pll_lock} is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
(161) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.
(162) Channel span is within a transceiver bank.
(163) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Clock Network	ATX PLL			CMU PLL (161)			fPLL		
	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span
xN (PCIe)	—	8.0	8	—	5.0	8	—	—	—
xN (Native PHY IP)	8.0	8.0	Up to 13 channels above and below PLL	7.99	7.99	Up to 13 channels above and below PLL	3.125	3.125	Up to 13 channels above and below PLL
	—	8.01 to 9.8304	Up to 7 channels above and below PLL						

Standard PCS Data Rate

Table 2-30: Standard PCS Approximate Maximum Date Rate (Gbps) for Arria V GZ Devices

The maximum data rate is also constrained by the transceiver speed grade. Refer to the "Commercial and Industrial Speed Grade Offering for Arria V GZ Devices" table for the transceiver speed grade.

Mode (164)	Transceiver Speed Grade	PMA Width	20	20	16	16	10	10	8	8
		PCS/Core Width	40	20	32	16	20	10	16	8
FIFO	2	C3, I3L core speed grade	9.9	9	7.84	7.2	5.3	4.7	4.24	3.76
	3	C4, I4 core speed grade	8.8	8.2	7.2	6.56	4.8	4.3	3.84	3.44

(161) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

(164) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 3 to 10 [192], [193], [194], [195], [196], [197]	150	—	1250	150	—	1050	Mbps
	SERDES factor J ≥ 4 LVDS RX with DPA [193], [195], [196], [197]	150	—	1600	150	—	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	[198]	—	[199]	[198]	—	[199]	Mbps
	SERDES factor J = 1, uses SDR Register	[198]	—	[199]	[198]	—	[199]	Mbps
f_{HSDR} (data rate)	SERDES factor J = 3 to 10	[198]	—	[200]	[198]	—	[200]	Mbps
	SERDES factor J = 2, uses DDR Registers	[198]	—	[199]	[198]	—	[199]	Mbps
	SERDES factor J = 1, uses SDR Register	[198]	—	[199]	[198]	—	[199]	Mbps

(192) The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.
(193) Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.
(194) Arria V GZ LVDS serialization and de-serialization factor needs to be x4 and above.
(195) Requires package skew compensation with PCB trace length.
(196) Do not mix single-ended I/O buffer within LVDS I/O bank.
(197) Chip-to-chip communication only with a maximum load of 5 pF.
(198) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.
(199) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.
(200) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

DLL Range Specifications

Table 2-47: DLL Range Specifications for Arria V GZ Devices

Arria V GZ devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Parameter	C3, I3L	C4, I4	Unit
DLL operating frequency range	300 – 890	300 – 890	MHz

DQS Logic Block Specifications

Table 2-48: DQS Phase Offset Delay Per Setting for Arria V GZ Devices

The typical value equals the average of the minimum and maximum values.

The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a –3 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 11 ps) ± 20 ps] = 735 ps ± 20 ps.

Speed Grade	Min	Max	Unit
C3, I3L	8	15	ps
C4, I4	8	16	ps

Table 2-49: DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria V GZ Devices

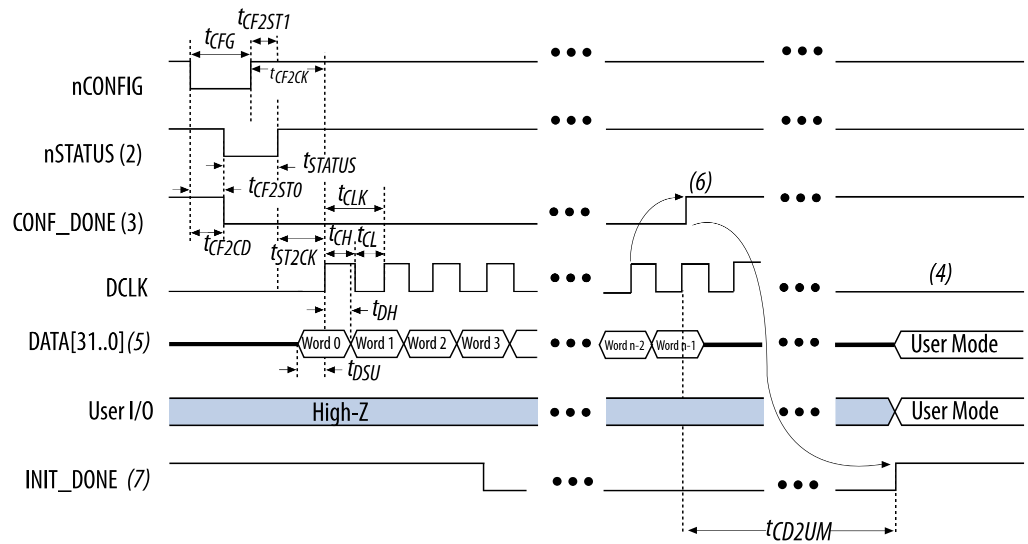
This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a –3 speed grade is ±84 ps or ±42 ps.

Number of DQS Delay Buffers	C3, I3L	C4, I4	Unit
1	30	32	ps
2	60	64	ps
3	90	96	ps

FPP Configuration Timing when DCLK to DATA[] = 1

Figure 2-7: FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1

Timing waveform for FPP configuration when using a MAX® II or MAX V device as an external host.



Notes:
1. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
2. After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.
3. After power-up, before and during configuration, CONF_DONE is low.
4. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
5. For FPP ×16, use DATA[15..0]. For FPP ×8, use DATA[7..0]. DATA[31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high when the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
7. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CD2CU}	`CONF_DONE` high to `CLKUSR` enabled	4 × maximum `DCLK` period	—	—
t_{CD2UMC}	`CONF_DONE` high to user mode with `CLKUSR` option on	t_{CD2CU} + (8576 × `CLKUSR` period) (209)	—	—

Related Information

- **DCLK-to-DATA[] Ratio (r) for FPP Configuration** on page 2-57
- **Configuration, Design Security, and Remote System Upgrades in Arria V Devices**

(208) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

(209) To enable the `CLKUSR` pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Table 2-57: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1,506 (210)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 (211)	µs
t_{CF2CK} (212)	nCONFIG high to first rising edge on DCLK	1,506	—	µs
t_{ST2CK} (212)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N-1/f_{DCLK}$ (213)	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16)	—	125	MHz
	DCLK frequency (FPP ×32)	—	100	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode (214)	175	437	µs

(210) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(211) You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.
(212) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.
(213) N is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.
(214) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.