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Intel - 5AGXFB3H4F40C4N Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Details	
Product Status	Obsolete
Number of LABs/CLBs	17110
Number of Logic Elements/Cells	362000
Total RAM Bits	19822592
Number of I/O	704
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxfb3h4f40c4n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Symbol	Description	Condition	Minimum ⁽¹⁾	Typical	Maximum ⁽¹⁾	Unit
		3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
V	1/O buffers newer supply	1.8 V	1.71	1.8	1.89	V
V CCIO	1/O bullets power supply	1.5 V	1.425	1.5	1.575	V
		1.35 V	1.283	1.35	1.418	V
	-	1.25 V	1.19	1.25	1.31	V
		1.2 V	1.14	1.2	1.26	V
V _{CCD_FPLL}	PLL digital voltage regulator power supply	_	1.425	1.5	1.575	V
V _{CCA_FPLL}	PLL analog voltage regulator power supply	_	2.375	2.5	2.625	V
V _I	DC input voltage	_	-0.5	_	3.6	V
V _O	Output voltage	_	0	_	V _{CCIO}	V
TJ	Operating junction temperature	Commercial	0	_	85	°C
	Operating junction temperature	Industrial	-40	_	100	°C
+ (4)	Power supply ramp time	Standard POR	200 µs	_	100 ms	_
t _{RAMP} ⁽⁴⁾	Power supply ramp time	Fast POR	200 µs	_	4 ms	_



⁽¹⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁴⁾ This is also applicable to HPS power supply. For HPS power supply, refer to t_{RAMP} specifications for standard POR when HPS_PORSEL = 0 and t_{RAMP} specifications for fast POR when HPS_PORSEL = 1.

Table 1-21: Transceiver Clocks Specifications for Arria V GX and SX Devices

Sumbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
Symbol/Description	Condition	Min	Тур	Max	Min	Тур	Max	Onit
fixedclk clock frequency	PCIe Receiver Detect	_	125	_	_	125	_	MHz
Transceiver Reconfigura- tion Controller IP (mgmt_ clk_clk) clock frequency	_	75	_	125	75	_	125	MHz

Table 1-22: Receiver Specifications for Arria V GX and SX Devices

Symbol/Description	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit	
symbol/Description	Condition	Min	Тур	Max	Min	Тур	Max	Onit
Supported I/O standards		1	.5 V PCML,	2.5 V PCML,	LVPECL, an	d LVDS		
Data rate ⁽²⁸⁾		611	—	6553.6	611	—	3125	Mbps
Absolute V_{MAX} for a receiver pin ⁽²⁹⁾	_		_	1.2		—	1.2	V
Absolute V _{MIN} for a receiver pin	_	-0.4	_		-0.4	—	—	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) before device configuration	_	_		1.6		_	1.6	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) after device configuration	_	_	_	2.2		_	2.2	V



 ⁽²⁸⁾ To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.
 ⁽²⁹⁾ The device cannot tolerate prolonged operation at this absolute maximum.

Symbol/Description	Condition	Tran	sceiver Speed Gra	Unit	
Symbol/Description	Condition	Min	Тур	Max	Ont
	85- Ω setting	—	85	—	Ω
Differential on-chip termination	100- Ω setting	—	100	—	Ω
resistors	120-Ω setting	—	120	—	Ω
	150-Ω setting		150	_	Ω
Intra-differential pair skew	TX V_{CM} = 0.65 V (AC coupled) and slew rate of 15 ps			15	ps
Intra-transceiver block transmitter channel-to-channel skew	×6 PMA bonded mode			180	ps
Inter-transceiver block transmitter channel-to-channel skew ⁽⁵⁵⁾	× <i>N</i> PMA bonded mode			500	ps

Table 1-30: CMU PLL Specifications for Arria V GT and ST Devices

Symbol/Description	Transceiver S	peed Grade 3	Unit
Symbol Description	Min	Max	onit
Supported data range	0.611	10.3125	Gbps
fPLL supported data range	611	3125	Mbps

⁽⁵⁵⁾ This specification is only applicable to channels on one side of the device across two transceiver banks.



HPS Clock Performance

Table 1-48: HPS Clock Performance for Arria V Devices

Symbol/Description	-13	-C4	–C5, –I5	-C6	Unit
mpu_base_clk (microprocessor unit clock)	1050	925	800	700	MHz
main_base_clk (L3/L4 interconnect clock)	400	400	400	350	MHz
h2f_user0_clk	100	100	100	100	MHz
h2f_user1_clk	100	100	100	100	MHz
h2f_user2_clk	200	200	200	160	MHz

HPS PLL Specifications

HPS PLL VCO Frequency Range

Table 1-49: HPS PLL VCO Frequency Range for Arria V Devices

Description	Speed Grade	Minimum	Maximum	Unit
	-C5, -I5, -C6	320	1,600	MHz
VCO range	-C4	320	1,850	MHz
	-I3	320	2,100	MHz

HPS PLL Input Clock Range

The HPS PLL input clock range is 10 – 50 MHz. This clock range applies to both HPS_CLK1 and HPS_CLK2 inputs.

Related Information

Clock Select, Booting and Configuration chapter

Provides more information about the clock range for different values of clock select (CSEL).



Symbol	Description	Min	Тур	Max	Unit
T _{din_end}	Input data valid end	$(2 + R_{delay}) \times T_{qspi_clk} - 1.21^{(85)}$			ns

Figure 1-8: Quad SPI Flash Timing Diagram

This timing diagram illustrates clock polarity mode 0 and clock phase mode 0.



Related Information

Quad SPI Flash Controller Chapter, Arria V Hard Processor System Technical Reference Manual

Provides more information about Rdelay.

SPI Timing Characteristics

Table 1-52: SPI Master Timing Requirements for Arria V Devices

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

Symbol	Description	Min	Max	Unit
T _{clk}	CLK clock period	16.67	—	ns
T _{su}	SPI Master-in slave-out (MISO) setup time	8.35 (86)	—	ns

 $^{^{(85)}}$ R_{delay} is set by programming the register <code>qspiregs.rddatacap</code>. For the SoC EDS software version 13.1 and later, Altera provides automatic Quad SPI calibration in the preloader. For more information about R_{delay}, refer to the Quad SPI Flash Controller chapter in the Arria V Hard Processor System Technical Reference Manual.



Figure 1-15: MDIO Timing Diagram



I²C Timing Characteristics

Table 1-59: I²C Timing Requirements for Arria V Devices

Symbol	Symbol		Standard Mode		Mode	Unit	
Symbol	Description	Min	Max	Min	Max	Ont	
T _{clk}	Serial clock (SCL) clock period	10	—	2.5		μs	
T _{clkhigh}	SCL high time	4.7	—	0.6		μs	
T _{clklow}	SCL low time	4	—	1.3		μs	
T _s	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1		μs	
T _h	Hold time for SCL to SDA data	0	3.45	0	0.9	μs	
T _d	SCL to SDA output data delay	—	0.2		0.2	μs	
T _{su_start}	Setup time for a repeated start condition	4.7	_	0.6		μs	
T _{hd_start}	Hold time for a repeated start condition	4	_	0.6		μs	
T _{su_stop}	Setup time for a stop condition	4	_	0.6	_	μs	



Figure 1-18: NAND Address Latch Timing Diagram







Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)
	A1	71,015,712	439,960
	A3	71,015,712	439,960
	A5	101,740,800	446,360
Arria V CY	A7	101,740,800	446,360
	B1	137,785,088	457,368
	B3	137,785,088	457,368
	B5	185,915,808	463,128
	B7	185,915,808	463,128
	C3	71,015,712	439,960
Arria V CT	C7	101,740,800	446,360
Allia v GI	D3	137,785,088	457,368
	D7	185,915,808	463,128
Arria V SV	B3	185,903,680	450,968
Allia V SA	B5	185,903,680	450,968
Arria V ST	D3	185,903,680	450,968
Arria V ST	D5	185,903,680	450,968

Minimum Configuration Time Estimation

Table 1-73: Minimum Configuration Time Estimation for Arria V Devices

The estimated values are based on the configuration .rbf sizes in Uncompressed .rbf Sizes for Arria V Devices table.





Arria V GX, GT, SX, and ST Device Datasheet

Altera Corporation



1-94 Document Revision History

Term	Definition
V _{OX}	Output differential cross point voltage
W	High-speed I/O block—Clock boost factor

Document Revision History

Date	Version	Changes
December 2016	2016.12.09	 Updated V_{ICM} (AC coupled) specifications in Receiver Specifications for Arria V GX and SX Devices table. Added maximum specification for T_d in Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices table. Updated T_{init} specifications in the following tables: FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Arria V Devices FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices PS Timing Parameters for Arria V Devices
June 2016	2016.06.10	 Changed pin capacitance to maximum values. Updated SPI Master Timing Requirements for Arria V Devices table. Added T_{su} and T_h specifications. Removed T_{dinmax} specifications. Updated SPI Master Timing Diagram. Updated T_{clk} spec from maximum to minimum in I²C Timing Requirements for Arria V Devices table.





1-96 Document Revision History

Date	Version	Changes
June 2015	2015.06.16	 Added the supported data rates for the following output standards using true LVDS output buffer types in the High-Speed I/O Specifications for Arria V Devices table:
		True RSDS output standard: data rates of up to 360 Mbps
		 True mini-LVDS output standard: data rates of up to 400 Mbps
		 Added note in the condition for Transmitter—Emulated Differential I/O Standards f_{HSDR} data rate parameter in the High-Speed I/O Specifications for Arria V Devices table. Note: When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.
		Changed Queued Serial Peripheral Interface (QSPI) to Quad Serial Peripheral Interface (SPI) Flash.
		 Updated T_h location in I²C Timing Diagram.
		 Updared T_{wp} location in NAND Address Latch Timing Diagram.
		 Corrected the unit for t_{DH} from ns to s in FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices table.
		• Updated the maximum value for t _{CO} from 4 ns to 2 ns in AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices table.
		• Moved the following timing diagrams to the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.
		FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is 1
		 FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is >1
		AS Configuration Timing Waveform
		PS Configuration Timing Waveform



1-98 Document Revision History

Date	Version	Changes
July 2014	3.8	 Added a note in Table 3, Table 4, and Table 5: The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements. Updated V_{CC_HPS} specification in Table 5. Added a note in Table 19: Differential inputs are powered by V_{CCPD} which requires 2.5 V. Updated "Minimum differential eye opening at the receiver serial input pins" specification in Table 20 and Table 21. Updated description in "HPS PLL Specifications" section. Updated VCO range maximum specification in Table 39. Updated T_d and T_h specifications in Table 45. Added T_h specification in Table 47 and Figure 13. Updated a note in Figure 20, Figure 21, and Figure 23 as follows: Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required. Removed "Remote update only in AS mode" specification in Table 58. Added DCLK device initialization clock source specification in Table 60. Added description in "Configuration Files" section: The IOCSR .rbf size is specifically for the Configuration via Protocol (CvP) feature. Removed f_{MAX_RU_CLK} specification in Table 63.
February 2014	3.7	 Updated V_{CCRSTCLK_HPS} maximum specification in Table 1. Added V_{CC_AUX_SHARED} specification in Table 1.
December 2013	3.6	 Added "HPS PLL Specifications". Added Table 24, Table 39, and Table 40. Updated Table 1, Table 3, Table 5, Table 19, Table 20, Table 21, Table 38, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, Table 51, Table 55, Table 56, and Table 59. Updated Figure 7, Figure 13, Figure 15, Figure 16, and Figure 19. Removed table: GPIO Pulse Width for Arria V Devices.



Symbol	Description	Condition	Minimum ⁽¹¹⁴⁾	Typical	Maximum ⁽¹¹⁴⁾	Unit
VI	DC input voltage	_	-0.5	_	3.6	V
Vo	Output voltage		0	_	V _{CCIO}	V
Т.	Operating junction temperature	Commercial	0		85	°C
IJ		Industrial	-40	_	100	°C
t	Power supply ramp time	Standard POR	200 µs	_	100 ms	
•RAMP		Fast POR	200 µs	—	4 ms	

Recommended Transceiver Power Supply Operating Conditions

Table 2-6: Recommended Transceiver Power Supply Operating Conditions for Arria V GZ Devices

Symbol	Description	Minimum ⁽¹¹⁸⁾	Typical	Maximum ⁽¹¹⁸⁾	Unit
V _{CCA_GXBL}	Transcaiver channel DLL newer supply (left side)	2.85	3.0	3.15	V
(119), (120)	Transceiver channel FLL power supply (left side)	2.375	2.5	2.625	V
V _{CCA}	Transcaiver channel DLL never supply (right side)	2.85	3.0	3.15	V
GXBR ⁽¹¹⁹⁾ , ⁽¹²⁰⁾	Transceiver channel PLL power supply (right side)	2.375	2.5	2.625	v
V _{CCHIP_L}	Transceiver hard IP power supply (left side)	0.82	0.85	0.88	V
V _{CCHSSI_L}	Transceiver PCS power supply (left side)	0.82	0.85	0.88	V
V _{CCHSSI_R}	Transceiver PCS power supply (right side)	0.82	0.85	0.88	V

⁽¹¹⁴⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹¹⁸⁾ This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹²⁰⁾ When using ATX PLLs, the supply must be 3.0 V.



⁽¹¹⁹⁾ This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

Symbol	Description	Minimum ⁽¹¹⁸⁾	Typical	Maximum ⁽¹¹⁸⁾	Unit
		0.82	0.85	0.88	
V _{CCR_GXBL} ⁽¹²¹⁾	Receiver analog power supply (left side)	0.97	1.0	1.03	V
		1.03	1.05	1.07	
		0.82	0.85	0.88	
V _{CCR_GXBR} ⁽¹²¹⁾	Receiver analog power supply (right side)	0.97	1.0	1.03	V
		1.03	1.05	1.07	
		0.82	0.85	0.88	
V _{CCT_GXBL} ⁽¹²¹⁾	Transmitter analog power supply (left side)	0.97	1.0	1.03	V
		1.03	1.05	1.07	
		0.82	0.85	0.88	
V _{CCT_GXBR} ⁽¹²¹⁾	Transmitter analog power supply (right side)	0.97	1.0	1.03	V
· CC1_GADR		1.03	1.05	1.07	
V _{CCH_GXBL}	Transmitter output buffer power supply (left side)	1.425	1.5	1.575	V
V _{CCH_GXBR}	Transmitter output buffer power supply (right side)	1.425	1.5	1.575	V



⁽¹¹⁸⁾ This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹²¹⁾ This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rate up to 6.5 Gbps, you can connect this supply to 0.85 V.

Symbol	V _{OD} Setting	V _{OD} Value (mV)	V _{OD} Setting	V _{OD} Value (mV)
	15	300	47	940
	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
V_{OD} differential peak to peak typical	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260



Core Performance Specifications

Clock Tree Specifications

Table 2-33: Clock Tree Performance for Arria V GZ Devices

Sumbol	Perfo	llait	
зульог	C3, I3L	C4, I4	
Global and Regional Clock	650	580	MHz
Periphery Clock	500	500	MHz

PLL Specifications

Table 2-34: PLL Specifications for Arria V GZ Devices

Symbol	Parameter	Min	Тур	Мах	Unit
f (167)	Input clock frequency (C3, I3L speed grade)	5	—	800	MHz
IN	Input clock frequency (C4, I4 speed grade)	5	—	650	MHz
f _{INPFD}	Input frequency to the PFD	5	_	325	MHz
f _{FINPFD}	Fractional Input clock frequency to the PFD	50	_	160	MHz
f	PLL VCO operating range (C3, I3L speed grade)	600	_	1600	MHz
IVCO	PLL VCO operating range (C4, I4 speed grade)	600	—	1300	MHz
t _{EINDUTY}	Input clock or external feedback clock input duty cycle	40	_	60	%

⁽¹⁶⁷⁾ This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

⁽¹⁶⁸⁾ The VCO frequency reported by the Quartus II software in the **PLL Usage Summary** section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

Arria V GZ Device Datasheet





Non DPA Mode High-Speed I/O Specifications

Table 2-46: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions	C3, I3L			C4, I4			Unit
	Conditions	Min	Тур	Max	Min	Тур	Max	
Sampling Window	—	_		300	_		300	ps



2-64 FPP Configuration Timing when DCLK to DATA[] > 1

Symbol	Parameter	Minimum	Maximum	Unit
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK}$ period	_	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (8576 × CLKUSR period) ⁽²¹⁵⁾		_

Related Information

- DCLK-to-DATA[] Ratio (r) for FPP Configuration on page 2-57
- Configuration, Design Security, and Remote System Upgrades in Arria V Devices





⁽²¹⁵⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Active Serial Configuration Timing

Figure 2-9: AS Configuration Timing



Timing waveform for the active serial (AS) x1 mode and AS x4 mode configuration timing.

Notes:

1. If you are using AS ×4 mode, this signal represents the AS_DATA[3..0] and ERCQ sends in 4-bits of data for each DCLKcycle.

2. The initialization clock can be from internal oscillator or CLKUSR pin

3. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE ges low.

Table 2-58: AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices

The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in the "PS Timing Parameters for Arria V GZ Devices" table.



Term				Definition				
R _L	Receiver differential input discrete resistor (external to the Arria V GZ device).							
SW (sampling window)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:							
		Bit Time						
		0.5 x TCCS	RSKM	Sampling Window (SW)	RSKM	0.5 x TCCS		
Single-ended voltage referenced I/O standard	The JEDEC standard for SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing: Single-Ended Voltage Referenced I/O Standard							
		V _{0H}		V REF	Viн(DC Vil(DC)	V <u>ccio</u> VIH(AC) VIL(AC) VIL(AC)		

