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Intel - 5AGXFB3H4F40C5N Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Betuils	
Product Status	Obsolete
Number of LABs/CLBs	17110
Number of Logic Elements/Cells	362000
Total RAM Bits	19822592
Number of I/O	704
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxfb3h4f40c5n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Arria V GX, GT, SX, and ST Device Datasheet



This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Arria® V devices.

Arria V devices are offered in commercial and industrial grades. Commercial devices are offered in -C4 (fastest), -C5, and -C6 speed grades. Industrial grade devices are offered in the -I3 and -I5 speed grades.

Related Information

Arria V Device Overview

Provides more information about the densities and packages of devices in the Arria V family.

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Arria V devices.

Operating Conditions

Arria V devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Arria V devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Arria V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms.

The functional operation of the device is not implied for these conditions.

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		V _{CCIO} (V)													
Parameter Symbo	Symbol	nbol Condition	1	.2	1	.5	1	.8	2	.5	3	.0	3	.3	Unit
			Min	Мах	Min	Max	Min	Max	Min	Мах	Min	Max	Min	Max	
Bus-hold trip point	V _{TRIP}	_	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 1-8: OCT Calibration Accuracy Specifications for Arria V Devices

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (\/)	Ca	Unit		
Symbol	Description		–I3, –C4	–I5, –C5	-C6	Ont
25-Ω R _S	Internal series termination with calibration (25- Ω setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
50-Ω R _S	Internal series termination with calibration (50- Ω setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
34- Ω and 40- Ω R_S	Internal series termination with calibration (34- Ω and 40- Ω setting)	V _{CCIO} = 1.5, 1.35, 1.25, 1.2	±15	±15	±15	%
48-Ω, 60-Ω, and 80- Ω R _S	Internal series termination with calibration (48- Ω , 60- Ω , and 80- Ω setting)	$V_{CCIO} = 1.2$	±15	±15	±15	%
50-Ω R_T	Internal parallel termination with calibration (50- Ω setting)	V _{CCIO} = 2.5, 1.8, 1.5, 1.2	-10 to +40	-10 to +40	-10 to +40	%
20- Ω , 30- Ω , 40- Ω ,60- Ω , and 120- Ω R _T	Internal parallel termination with calibration (20- Ω , 30- Ω , 40- Ω , 60- Ω , and 120- Ω setting)	V _{CCIO} = 1.5, 1.35, 1.25	-10 to +40	-10 to +40	-10 to +40	%



Symbol	Description	Maximum	Unit
I _{XCVR-RX (DC)}	DC current per transceiver receiver (RX) pin	50	mA

Internal Weak Pull-Up Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up.

Table 1-13: Internal Weak Pull-Up Resistor Values for Arria V Devices

Symbol	Description	Condition (V) ⁽¹¹⁾	Value ⁽¹²⁾	Unit
		$V_{CCIO} = 3.3 \pm 5\%$	25	kΩ
		$V_{CCIO} = 3.0 \pm 5\%$	25	kΩ
	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	$V_{CCIO} = 2.5 \pm 5\%$	25	kΩ
D		$V_{CCIO} = 1.8 \pm 5\%$	25	kΩ
кру		$V_{CCIO} = 1.5 \pm 5\%$	25	kΩ
		$V_{CCIO} = 1.35 \pm 5\%$	25	kΩ
		$V_{CCIO} = 1.25 \pm 5\%$	25	kΩ
		$V_{CCIO} = 1.2 \pm 5\%$	25	kΩ

Related Information

Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines

Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.



⁽¹⁰⁾ The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

 $^{^{(11)}}$ Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

⁽¹²⁾ Valid with $\pm 10\%$ tolerances to cover changes over PVT.

Symbol/Description	Condition	Т	Unit		
Symbol/Description	Condition	Min	Тур	Мах	Onit
$t_{LTD_manual}^{(51)}$		4	_	_	μs
t _{LTR_LTD_manual} ⁽⁵²⁾	_	15	_	—	μs
Programmable ppm detector ⁽⁵³⁾	_	±62.5, 100, 125, 200, 250, 300, 500, and 1000			ppm
Run length	_		_	200	UI
Programmable equalization AC and DC gain	AC gain setting = 0 to $3^{(54)}$ DC gain setting = 0 to 1	Refer to CTLE Response at Data Rates > 3.25 Gbps across Supported A and DC Gain for Arria V GX, GT, SX, and ST Devices and CTLE Response Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for A GX, GT, SX, and ST Devices diagrams.			oss Supported AC Gain and CTLE Response at d DC Gain for Arria V ums.

Table 1-29: Transmitter Specifications for Arria V GT and ST Devices

Sumbol/Description	Condition	Tran	lleit		
Symbol Description	Condition	Min	Тур	Max	onit
Supported I/O standards	1.5 V PCML				
Data rate (6-Gbps transceiver)	—	611		6553.6	Mbps
Data rate (10-Gbps transceiver)	_	0.611		10.3125	Gbps
V _{OCM} (AC coupled)	_		650		mV
V _{OCM} (DC coupled)	\leq 3.2 Gbps ⁽⁴⁸⁾	670	700	730	mV

⁽⁵³⁾ The rate match FIFO supports only up to ± 300 ppm.

⁽⁵⁴⁾ The Quartus Prime software allows AC gain setting = 3 for design with data rate between 611 Mbps and 1.25 Gbps only.



 $^{^{(51)}}$ t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.

⁽⁵²⁾ t_{LTR_LTD_manual} is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.

DPA Lock Time Specifications

Figure 1-4: Dynamic Phase Alignment (DPA) Lock Time Specifications with DPA PLL Calibration Enabled



Table 1-41: DPA Lock Time Specifications for Arria V Devices

The specifications are applicable to both commercial and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽⁸⁴⁾	Maximum Data Transition
SPI-4	00000000001111111111	2	128	640
Denallal Danid I/O	00001111	2	128	640
rataliei Kapiti 1/0	10010000	4	64	640
Miscellencous	10101010	8	32	640
witscenaricous	01010101	8	32	640

⁽⁸⁴⁾ This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.



Figure 1-20: NAND Data Read Timing Diagram



ARM Trace Timing Characteristics

Table 1-61: ARM Trace Timing Requirements for Arria V Devices

Most debugging tools have a mechanism to adjust the capture point of trace data.

Description	Min	Мах	Unit
CLK clock period	12.5	_	ns
CLK maximum duty cycle	45	55	%
CLK to D0 –D7 output data delay	-1	1	ns

UART Interface

The maximum UART baud rate is 6.25 megasymbols per second.

GPIO Interface

The minimum detectable general-purpose I/O (GPIO) pulse width is 2 µs. The pulse width is based on a debounce clock frequency of 1 MHz.



1-80 AS Configuration Timing

Symbol	Parameter	Minimum	Maximum	Unit
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times maximum$ DCLK period	—	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + ($T_{init} \times CLKUSR$ period)		
T _{init}	Number of clock cycles required for device initialization	8,576		Cycles

Related Information

FPP Configuration Timing

Provides the FPP configuration timing waveforms.

AS Configuration Timing

Table 1-68: AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices

The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

The t_{CF2CD} , t_{CF2ST0} , t_{CFG} , t_{STATUS} , and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in PS Timing Parameters for Arria V Devices table. You can obtain the t_{CF2ST1} value if you do not delay configuration by externally holding nSTATUS low.

Symbol	Parameter	Minimum	Maximum	Unit
t _{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	2	ns
t _{SU}	Data setup time before the falling edge on DCLK	1.5		ns
t _{DH}	Data hold time after the falling edge on DCLK	0	_	ns
t _{CD2UM}	CONF_DONE high to user mode	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	_	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + ($T_{init} \times CLKUSR$ period)	_	—
T _{init}	Number of clock cycles required for device initialization	8,576		Cycles



Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)
	A1	71,015,712	439,960
	A3	71,015,712	439,960
	A5	101,740,800	446,360
Arria V CY	A7	101,740,800	446,360
	B1	137,785,088	457,368
	B3	137,785,088	457,368
	B5	185,915,808	463,128
	B7	185,915,808	463,128
	C3	71,015,712	439,960
Arria V CT	C7	101,740,800	446,360
Allia v GI	D3	137,785,088	457,368
	D7	185,915,808	463,128
Arria V SV	B3	185,903,680	450,968
Arria V SX	B5	185,903,680	450,968
Arria V ST	D3	185,903,680	450,968
Arria V SI	D5	185,903,680	450,968

Minimum Configuration Time Estimation

Table 1-73: Minimum Configuration Time Estimation for Arria V Devices

The estimated values are based on the configuration .rbf sizes in Uncompressed .rbf Sizes for Arria V Devices table.



1-88	Glossary			AV-5100 2017.02.1
	Symbol	Parameter	Typical	Unit
			0 (default)	ps
Л	·	Rising and/or falling edge delay	50	ps
D _{OUTBUF}	OUTBUF		100	ps
			150	ps

Glossary

Table 1-78: Glossary

Term	Definition	
Differential I/O standards	Receiver Input Waveforms	
	Single-Ended Waveform	Positive Channel (p) = V_{IH} Negative Channel (n) = V_{IL}
		Ground
	Differential Waveform	
		p - n = 0 V



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Term		Definition							
Single-ended voltage referenced I/O standard	 The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The A values indicate the voltage levels at which the receiver must meet its timing specifications. The DC value indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approact is intended to provide predictable receiver timing in the presence of input waveform ringing. Single-Ended Voltage Referenced I/O Standard 								
	V _{ОН}		V _{IH(AC)}						
			VIH(DC)						
		V _{REF}	V IL(DC)						
			VIL(AC)						
	V _{0L}								
			V _{SS}						
t _C	High-speed receiver/transmitter	input and output clock period.							
TCCS (channel-to-channel-skew)	The timing difference between th skew, across channels driven by th the Timing Diagram figure under	e fastest and slowest output edges, in he same PLL. The clock is included in r SW in this table).	cluding the t _{CO} variation and clock n the TCCS measurement (refer to						
t _{DUTY}	High-speed I/O block—Duty cyc	le on high-speed transmitter output	clock.						



1-98 Document Revision History

Date	Version	Changes
July 2014	3.8	 Added a note in Table 3, Table 4, and Table 5: The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements. Updated V_{CC_HPS} specification in Table 5. Added a note in Table 19: Differential inputs are powered by V_{CCPD} which requires 2.5 V. Updated "Minimum differential eye opening at the receiver serial input pins" specification in Table 20 and Table 21. Updated description in "HPS PLL Specifications" section. Updated VCO range maximum specification in Table 39. Updated T_d and T_h specifications in Table 45. Added T_h specification in Table 47 and Figure 13. Updated a note in Figure 20, Figure 21, and Figure 23 as follows: Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required. Removed "Remote update only in AS mode" specification in Table 58. Added DCLK device initialization clock source specification in Table 60. Added description in "Configuration Files" section: The IOCSR .rbf size is specifically for the Configuration via Protocol (CvP) feature. Removed f_{MAX_RU_CLK} specification in Table 63.
February 2014	3.7	 Updated V_{CCRSTCLK_HPS} maximum specification in Table 1. Added V_{CC_AUX_SHARED} specification in Table 1.
December 2013	3.6	 Added "HPS PLL Specifications". Added Table 24, Table 39, and Table 40. Updated Table 1, Table 3, Table 5, Table 19, Table 20, Table 21, Table 38, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, Table 51, Table 55, Table 56, and Table 59. Updated Figure 7, Figure 13, Figure 15, Figure 16, and Figure 19. Removed table: GPIO Pulse Width for Arria V Devices.



Hot Socketing

Table 2-14: Hot Socketing Specifications for Arria V GZ Devices

Symbol	Description	Maximum
I _{IOPIN (DC)}	DC current per I/O pin	300 µA
I _{IOPIN (AC)}	AC current per I/O pin	8 mA ⁽¹²⁴⁾
I _{XCVR-TX (DC)}	DC current per transceiver transmitter pin	100 mA
I _{XCVR-RX (DC)}	DC current per transceiver receiver pin	50 mA

Internal Weak Pull-Up Resistor

Table 2-15: Internal Weak Pull-Up Resistor for Arria V GZ Devices

All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins. The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 k Ω .

Symbol	Description	V _{CCIO} Conditions (V) ⁽¹²⁵⁾	Value ⁽¹²⁶⁾	Unit
		3.0 ±5%	25	kΩ
		2.5 ±5%	25	kΩ
	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option.	1.8 ±5%		kΩ
R _{PU}		1.5 ±5%	25	kΩ
		1.35 ±5%	25	kΩ
		1.25 ±5%	25	kΩ
		1.2 ±5%	25	kΩ

⁽¹²⁴⁾ The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.





 $^{^{(125)}}$ The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO} .

 $^{^{(126)}}$ These specifications are valid with a ±10% tolerance to cover changes over PVT.

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	V _{IL(DC)} (V)		V _{IH(DC)} (V)		V _{IL(AC)} (V)	$V_{IL(AC)}(V)$ $V_{IH(AC)}(V)$		V _{OL} (V) V _{OH} (V)		I (m A)
i/O Standard	Min	Max	Min	Max	Max	Min	Max	Min	i _{ol} (mA)	I _{oh} (MA)
SSTL-18 Class II	-0.3	V _{REF} – 0.125	V _{REF} + 0.125	V _{CCIO} + 0.3	V _{REF} – 0.25	V _{REF} + 0.25	0.28	V _{CCIO} – 0.28	13.4	-13.4
SSTL-15 Class I	—	V _{REF} – 0.1	V _{REF} + 0.1	—	V _{REF} – 0.175	V _{REF} + 0.175	$0.2 \times V_{ m CCIO}$	$0.8 \times V_{ m CCIO}$	8	-8
SSTL-15 Class II	_	V _{REF} – 0.1	V _{REF} + 0.1	—	V _{REF} – 0.175	V _{REF} + 0.175	$0.2 \times V_{ m CCIO}$	$0.8 \times V_{ m CCIO}$	16	-16
SSTL-135 Class I, II	_	V _{REF} – 0.09	V _{REF} + 0.09	—	V _{REF} – 0.16	V _{REF} + 0.16	0.2 * V _{CCIO}	0.8 * V _{CCIO}	_	-
SSTL-125 Class I, II	_	V _{REF} – 0.85	V _{REF} + 0.85	—	V _{REF} – 0.15	V _{REF} + 0.15	0.2 * V _{CCIO}	0.8 * V _{CCIO}	_	_
SSTL-12 Class I, II	_	V _{REF} – 0.1	V _{REF} + 0.1	—	V _{REF} – 0.15	V _{REF} + 0.15	0.2 * V _{CCIO}	0.8 * V _{CCIO}	—	_
HSTL-18 Class I		V _{REF} – 0.1	V _{REF} + 0.1	—	V _{REF} – 0.2	V _{REF} + 0.2	0.4	$V_{\rm CCIO}$ – 0.4	8	-8
HSTL-18 Class II		V _{REF} – 0.1	V _{REF} + 0.1	—	V _{REF} - 0.2	V _{REF} + 0.2	0.4	$V_{\rm CCIO}$ – 0.4	16	-16
HSTL-15 Class I	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} - 0.2	V _{REF} + 0.2	0.4	V _{CCIO} – 0.4	8	-8
HSTL-15 Class II	_	V _{REF} – 0.1	V _{REF} + 0.1	—	V _{REF} - 0.2	V _{REF} + 0.2	0.4	V _{CCIO} – 0.4	16	-16
HSTL-12 Class I	-0.15	V _{REF} – 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	$0.25 \times V_{ m CCIO}$	$0.75 \times V_{ m CCIO}$	8	-8
HSTL-12 Class II	-0.15	V _{REF} – 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	$0.25 \times V_{ m CCIO}$	$0.75 \times V_{ m CCIO}$	16	-16
HSUL-12	—	V _{REF} – 0.13	V _{REF} + 0.13	_	V _{REF} - 0.22	V_{REF} + 0.22	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	_	_

Arria V GZ Device Datasheet

Altera Corporation



Switching Characteristics

Transceiver Performance Specifications

Reference Clock

Table 2-22: Reference Clock Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transce	iver Speed	Unit			
Symbol/Description	Conditions	Min	Тур	Мах	Min	Тур	Мах	Onit		
Reference Clock										
Supported I/O Standards	Dedicated reference clock pin	e clock 1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, and HCSL								
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS								
Input Reference Clock Frequency (CMU PLL) ⁽¹³⁷⁾	_	40		710	40		710	MHz		
Input Reference Clock Frequency (ATX PLL) ⁽¹³⁷⁾	-	100		710	100		710	MHz		

⁽¹³⁷⁾ The input reference clock frequency options depend on the data rate and the device speed grade.



Sumbol	Conditions		C3, I3L			C4, I4			
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Onic	
	SERDES factor J = 3 to 10 (182), (183)	(184)	_	1250	(184)	_	1050	Mbps	
True Differential I/O Standards - f _{HSDR} (data rate)	SERDES factor $J \ge 4$ LVDS TX with DPA (185), (186), (187), (188)	(184)		1600	(184)	_	1250	Mbps	
	SERDES factor J = 2, uses DDR Registers	(184)	—	(189)	(184)	_	(189)	Mbps	
	SERDES factor J = 1, uses SDR Register	(184)	—	(189)	(184)		(189)	Mbps	
Emulated Differential I/O Standards with Three External Output Resistor Networks - f _{HSDR} (data rate) (190)	SERDES factor J = 4 to 10 ⁽¹⁹¹⁾	(184)		840	(184)		840	Mbps	

⁽¹⁸²⁾ If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

- ⁽¹⁸⁵⁾ Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.
- Requires package skew compensation with PCB trace length. (186)
- (187)Do not mix single-ended I/O buffer within LVDS I/O bank.
- Chip-to-chip communication only with a maximum load of 5 pF. (188)
- ⁽¹⁸⁹⁾ The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.
- ⁽¹⁹⁰⁾ You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.
- ⁽¹⁹¹⁾ When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.



⁽¹⁸³⁾ The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

⁽¹⁸⁴⁾ The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

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Symbol	Conditions		C3, I3L			Unit		
Symbol	Conditions	Min	Тур	Мах	Min	Тур	Max	Unit
t _{x Jitter} - True Differential I/O	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—		160		—	160	ps
Standards	Total Jitter for Data Rate < 600 Mbps	—		0.1		_	0.1	UI
t _{x Jitter} - Emulated Differential I/O Standards with Three	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—		300		—	325	ps
External Output Resistor Network	Total Jitter for Data Rate < 600 Mbps	—		0.2		—	0.25	UI
t _{DUTY}	Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	%
	True Differential I/O Standards	_		200		—	200	ps
t _{RISE} & t _{FALL}	Emulated Differential I/O Standards with three external output resistor networks			250		_	300	ps
	True Differential I/O Standards			150		—	150	ps
TCCS	Emulated Differential I/O Standards	_	_	300		_	300	ps

Receiver High-Speed I/O Specifications

Table 2-41: Receiver High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.



Number of DQS Delay Buffers	C3, I3L	C4, I4	Unit
4	120	128	ps

Memory Output Clock Jitter Specifications

Table 2-50: Memory Output Clock Jitter Specification for Arria V GZ Devices

The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

Clock Notwork	Parameter	Symbol	C3, I3L		C4	llnit	
CIOCK NELWOIK	raiailietei	Symbol	Min	Мах	Min	Мах	
	Clock period jitter	t _{JIT(per)}	-55	55	-55	55	ps
Regional	Cycle-to-cycle period jitter	t _{JIT(cc)}	-110	110	-110	110	ps
	Duty cycle jitter	t _{JIT(duty)}	-82.5	82.5	-82.5	82.5	ps
	Clock period jitter	t _{JIT(per)}	-82.5	82.5	-82.5	82.5	ps
Global	Cycle-to-cycle period jitter	t _{JIT(cc)}	-165	165	-165	165	ps
	Duty cycle jitter	t _{JIT(duty)}	-90	90	-90	90	ps
	Clock period jitter	t _{JIT(per)}	-30	30	-35	35	ps
PHY Clock	Cycle-to-cycle period jitter	t _{JIT(cc)}	-60	60	-70	70	ps
	Duty cycle jitter	t _{JIT(duty)}	-45	45	-56	56	ps



Symbol	Parameter	Minimum	Maximum	Unit
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times maximum$	—	_
		DCLK period		
t _{CD2UM} C	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (8576 × CLKUSR period) (209)		_

Related Information

- DCLK-to-DATA[] Ratio (r) for FPP Configuration on page 2-57 ٠
- Configuration, Design Security, and Remote System Upgrades in Arria V Devices

Arria V GZ Device Datasheet

Altera Corporation



⁽²⁰⁸⁾ The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

⁽²⁰⁹⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.

2-70 Remote System Upgrades Circuitry Timing Specification

Table 2-62: Uncompressed .rbf Sizes for Arria V GZ Devices

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ⁽²²³⁾
	E1	137,598,880	562,208
Arria V C7	E3	137,598,880	562,208
	E5	213,798,880	561,760
	E7	213,798,880	561,760

Table 2-63: Minimum Configuration Time Estimation for Arria V GZ Devices

	Member Code	Active Serial ⁽²²⁴⁾		Fast Passive Parallel ⁽²²⁵⁾			
Variant		Width	DCLK (MHz)	Min Config Time (ms)	Width	DCLK (MHz)	Min Config Time (ms)
	E1	4	100	344	32	100	43
Arria V GZ	E3	4	100	344	32	100	43
	E5	4	100	534	32	100	67
	E7	4	100	534	32	100	67

Remote System Upgrades Circuitry Timing Specification

Table 2-64: Remote System Upgrade Circuitry Timing Specifications

Parameter	Minimum	Maximum	Unit
t _{RU_nCONFIG} ⁽²²⁶⁾	250	—	ns
t _{RU_nRSTIMER} ⁽²²⁷⁾	250	_	ns

⁽²²³⁾ The IOCSR **.rbf** size is specifically for the Configuration via Protocol (CvP) feature.

⁽²²⁴⁾ DCLK frequency of 100 MHz using external CLKUSR.

⁽²²⁵⁾ Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.



Term	Definition			
	Single-Ended WaveformVODPositive Channel (p) = VOHVCMNegative Channel (n) = VOLGroundGround			
	Differential Waveform V_{0D} V_{0D} V_{0D} V_{0D}			
f _{HSCLK}	Left and right PLL input clock frequency.			
f _{HSDR}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDR} = 1/TUI), non-DPA.			
f _{hsdrdpa}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDRDPA} = 1/TUI), DPA.			
J	High-speed I/O block—Deserialization factor (width of parallel data bus).			



