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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	19811
Number of Logic Elements/Cells	420000
Total RAM Bits	23625728
Number of I/O	544
Number of Gates	-
Voltage - Supply	1.12V ~ 1.18V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/5agxfb5h4f35i3">https://www.e-xfl.com/product-detail/intel/5agxfb5h4f35i3</a>

Symbol	Description	Minimum <sup>(5)</sup>	Typical	Maximum <sup>(5)</sup>	Unit
V <sub>CCL_GXBL</sub>	GX and SX speed grades—clock network power (left side)	1.08/1.12	1.1/1.15 <sup>(6)</sup>	1.14/1.18	V
V <sub>CCL_GXBR</sub>	GX and SX speed grades—clock network power (right side)				
V <sub>CCL_GXBL</sub>	GT and ST speed grades—clock network power (left side)	1.17	1.20	1.23	V
V <sub>CCL_GXBR</sub>	GT and ST speed grades—clock network power (right side)				

**Related Information****Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines**

Provides more information about the power supply connection for different data rates.

**HPS Power Supply Operating Conditions****Table 1-5: HPS Power Supply Operating Conditions for Arria V SX and ST Devices**

This table lists the steady-state voltage and current values expected from Arria V system-on-a-chip (SoC) devices with ARM®-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to Recommended Operating Conditions for Arria V Devices table for the steady-state voltage values expected from the FPGA portion of the Arria V SoC devices.

Symbol	Description	Condition	Minimum <sup>(7)</sup>	Typical	Maximum <sup>(7)</sup>	Unit
V <sub>CC_HPS</sub>	HPS core voltage and periphery circuitry power supply	–C4, –I5, –C5, –C6	1.07	1.1	1.13	V
		–I3	1.12	1.15	1.18	V

<sup>(5)</sup> The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

<sup>(7)</sup> The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

I/O Standard	$V_{IL(DC)} (V)$		$V_{IH(DC)} (V)$		$V_{IL(AC)} (V)$	$V_{IH(AC)} (V)$	$V_{OL} (V)$	$V_{OH} (V)$	$I_{OL}^{(14)} (mA)$	$I_{OH}^{(14)} (mA)$
	Min	Max	Min	Max	Max	Min	Max	Min		
HSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-12 Class I	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	16	-16
HSUL-12	—	$V_{REF} - 0.13$	$V_{REF} + 0.13$	—	$V_{REF} - 0.22$	$V_{REF} + 0.22$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	—	—

### Differential SSTL I/O Standards

Table 1-17: Differential SSTL I/O Standards for Arria V Devices

I/O Standard	$V_{CCIO} (V)$			$V_{SWING(DC)} (V)$		$V_{X(AC)} (V)$			$V_{SWING(AC)} (V)$	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.62	$V_{CCIO} + 0.6$
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	$V_{CCIO} + 0.6$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	<sup>(15)</sup>	$V_{CCIO}/2 - 0.15$	—	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$
SSTL-135	1.283	1.35	1.45	0.18	<sup>(15)</sup>	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$

<sup>(14)</sup> To meet the  $I_{OL}$  and  $I_{OH}$  specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the  $I_{OL}$  and  $I_{OH}$  specifications in the datasheet.

<sup>(15)</sup> The maximum value for  $V_{SWING(DC)}$  is not defined. However, each single-ended signal needs to be within the respective single-ended limits ( $V_{IH(DC)}$  and  $V_{IL(DC)}$ ).

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Minimum differential eye opening at the receiver serial input pins <sup>(30)</sup>	—	100	—	—	100	—	—	mV
V <sub>ICM</sub> (AC coupled)	—	—	0.7/0.75/ 0.8 <sup>(31)</sup>	—	—	0.7/0.75/ 0.8 <sup>(31)</sup>	—	mV
V <sub>ICM</sub> (DC coupled)	≤ 3.2Gbps <sup>(32)</sup>	670	700	730	670	700	730	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	—	85	—	Ω
	100-Ω setting	—	100	—	—	100	—	Ω
	120-Ω setting	—	120	—	—	120	—	Ω
	150-Ω setting	—	150	—	—	150	—	Ω
t <sub>LTR</sub> <sup>(33)</sup>	—	—	—	10	—	—	10	μs
t <sub>LTD</sub> <sup>(34)</sup>	—	4	—	—	4	—	—	μs
t <sub>LTD_manual</sub> <sup>(35)</sup>	—	4	—	—	4	—	—	μs
t <sub>LTR_LTD_manual</sub> <sup>(36)</sup>	—	15	—	—	15	—	—	μs
Programmable ppm detector <sup>(37)</sup>	—	±62.5, 100, 125, 200, 250, 300, 500, and 1000						ppm

<sup>(30)</sup> The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

<sup>(31)</sup> The AC coupled V<sub>ICM</sub> = 700 mV for Arria V GX and SX in PCIe mode only. The AC coupled V<sub>ICM</sub> = 750 mV for Arria V GT and ST in PCIe mode only.

<sup>(32)</sup> For standard protocol compliance, use AC coupling.

<sup>(33)</sup> t<sub>LTR</sub> is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

<sup>(34)</sup> t<sub>LTD</sub> is time required for the receiver CDR to start recovering valid data after the rx\_is\_lockedto data signal goes high.

<sup>(35)</sup> t<sub>LTD\_manual</sub> is the time required for the receiver CDR to start recovering valid data after the rx\_is\_lockedto data signal goes high when the CDR is functioning in the manual mode.

<sup>(36)</sup> t<sub>LTR\_LTD\_manual</sub> is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx\_is\_lockedto ref signal goes high when the CDR is functioning in the manual mode.

For example, when  $V_{OD} = 800$  mV, the corresponding  $V_{OD}$  value setting is 40. The following conditions show that the 1st post tap pre-emphasis setting = 2 is valid:

- $|B| + |C| \leq 60 \rightarrow 40 + 2 = 42$
- $|B| - |C| > 5 \rightarrow 40 - 2 = 38$
- $(V_{MAX}/V_{MIN} - 1)\% < 600\% \rightarrow (42/38 - 1)\% = 10.52\%$

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Arria V HSSI HSPICE models.

**Table 1-33: Transmitter Pre-Emphasis Levels for Arria V Devices**

Quartus Prime 1st Post Tap Pre-Emphasis Setting	Quartus Prime $V_{OD}$ Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
0	0	0	0	0	0	0	0	dB
1	1.97	0.88	0.43	0.32	0.24	0.19	0.13	dB
2	3.58	1.67	0.95	0.76	0.61	0.5	0.41	dB
3	5.35	2.48	1.49	1.2	1	0.83	0.69	dB
4	7.27	3.31	2	1.63	1.36	1.14	0.96	dB
5	—	4.19	2.55	2.1	1.76	1.49	1.26	dB
6	—	5.08	3.11	2.56	2.17	1.83	1.56	dB
7	—	5.99	3.71	3.06	2.58	2.18	1.87	dB
8	—	6.92	4.22	3.47	2.93	2.48	2.11	dB
9	—	7.92	4.86	4	3.38	2.87	2.46	dB
10	—	9.04	5.46	4.51	3.79	3.23	2.77	dB
11	—	10.2	6.09	5.01	4.23	3.61	—	dB
12	—	11.56	6.74	5.51	4.68	3.97	—	dB
13	—	12.9	7.44	6.1	5.12	4.36	—	dB
14	—	14.44	8.12	6.64	5.57	4.76	—	dB
15	—	—	8.87	7.21	6.06	5.14	—	dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{\text{OUT\_EXT}}$	Output frequency for external clock output	–3 speed grade	—	—	670 <sup>(63)</sup>	MHz
		–4 speed grade	—	—	670 <sup>(63)</sup>	MHz
		–5 speed grade	—	—	622 <sup>(63)</sup>	MHz
		–6 speed grade	—	—	500 <sup>(63)</sup>	MHz
$t_{\text{OUTDUTY}}$	Duty cycle for external clock output (when set to 50%)	—	45	50	55	%
$t_{\text{FCOMP}}$	External feedback clock compensation time	—	—	—	10	ns
$t_{\text{DYCONFIGCLK}}$	Dynamic configuration clock for <code>mgmt_clk</code> and <code>scanclk</code>	—	—	—	100	MHz
$t_{\text{LOCK}}$	Time required to lock from end-of-device configuration or deassertion of <code>areset</code>	—	—	—	1	ms
$t_{\text{DLOCK}}$	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
$f_{\text{CLBW}}$	PLL closed-loop bandwidth	Low	—	0.3	—	MHz
		Medium	—	1.5	—	MHz
		High <sup>(64)</sup>	—	4	—	MHz
$t_{\text{PLL\_PSERR}}$	Accuracy of PLL phase shift	—	—	—	±50	ps
$t_{\text{ARESET}}$	Minimum pulse width on the <code>areset</code> signal	—	10	—	—	ns
$t_{\text{INCCJ}}^{(65)(66)}$	Input clock cycle-to-cycle jitter	$F_{\text{REF}} \geq 100 \text{ MHz}$	—	—	0.15	UI (p-p)
		$F_{\text{REF}} < 100 \text{ MHz}$	—	—	±750	ps (p-p)

<sup>(64)</sup> High bandwidth PLL settings are not supported in external feedback mode.

<sup>(65)</sup> A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

<sup>(66)</sup>  $F_{\text{REF}}$  is  $f_{\text{IN}}/N$ , specification applies when  $N = 1$ .

## HPS Clock Performance

Table 1-48: HPS Clock Performance for Arria V Devices

Symbol/Description	–I3	–C4	–C5, –I5	–C6	Unit
mpu_base_clk (microprocessor unit clock)	1050	925	800	700	MHz
main_base_clk (L3/L4 interconnect clock)	400	400	400	350	MHz
h2f_user0_clk	100	100	100	100	MHz
h2f_user1_clk	100	100	100	100	MHz
h2f_user2_clk	200	200	200	160	MHz

## HPS PLL Specifications

### HPS PLL VCO Frequency Range

Table 1-49: HPS PLL VCO Frequency Range for Arria V Devices

Description	Speed Grade	Minimum	Maximum	Unit
VCO range	–C5, –I5, –C6	320	1,600	MHz
	–C4	320	1,850	MHz
	–I3	320	2,100	MHz

### HPS PLL Input Clock Range

The HPS PLL input clock range is 10 – 50 MHz. This clock range applies to both HPS\_CLK1 and HPS\_CLK2 inputs.

#### Related Information

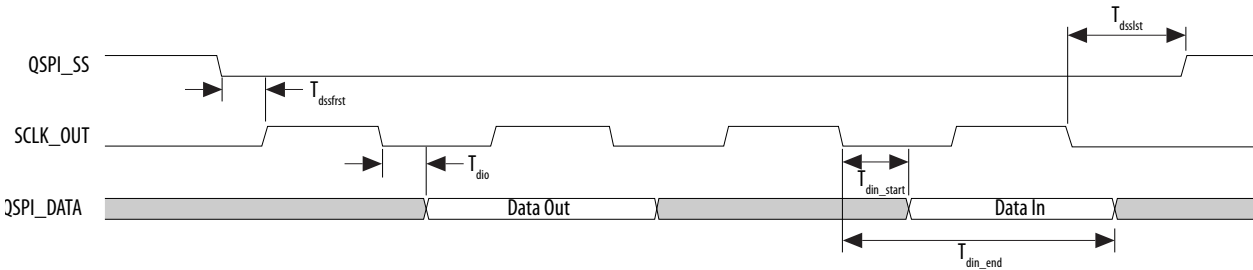
#### [Clock Select, Booting and Configuration chapter](#)

Provides more information about the clock range for different values of clock select (CSEL).

Symbol	Description	Min	Typ	Max	Unit
$T_{din\_end}$	Input data valid end	$(2 + R_{delay}) \times T_{qspi\_clk} - 1.21^{(85)}$	—	—	ns

Figure 1-8: Quad SPI Flash Timing Diagram

This timing diagram illustrates clock polarity mode 0 and clock phase mode 0.



Related Information

[Quad SPI Flash Controller Chapter, Arria V Hard Processor System Technical Reference Manual](#)

Provides more information about Rdelay.

SPI Timing Characteristics

Table 1-52: SPI Master Timing Requirements for Arria V Devices

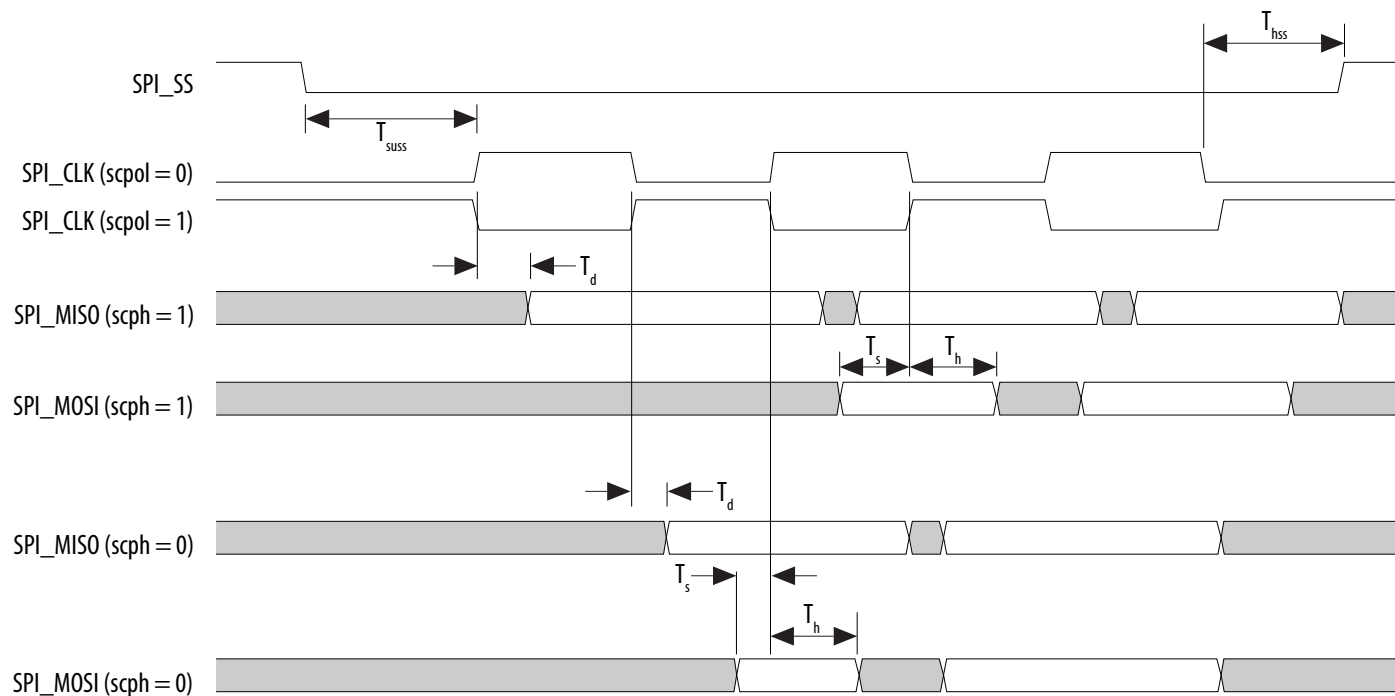
The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

Symbol	Description	Min	Max	Unit
$T_{clk}$	CLK clock period	16.67	—	ns
$T_{su}$	SPI Master-in slave-out (MISO) setup time	8.35 <sup>(86)</sup>	—	ns

<sup>(85)</sup>  $R_{delay}$  is set by programming the register `qspiregs.rddatacap`. For the SoC EDS software version 13.1 and later, Altera provides automatic Quad SPI calibration in the preloader. For more information about  $R_{delay}$ , refer to the Quad SPI Flash Controller chapter in the Arria V Hard Processor System Technical Reference Manual.



Figure 1-10: SPI Slave Timing Diagram

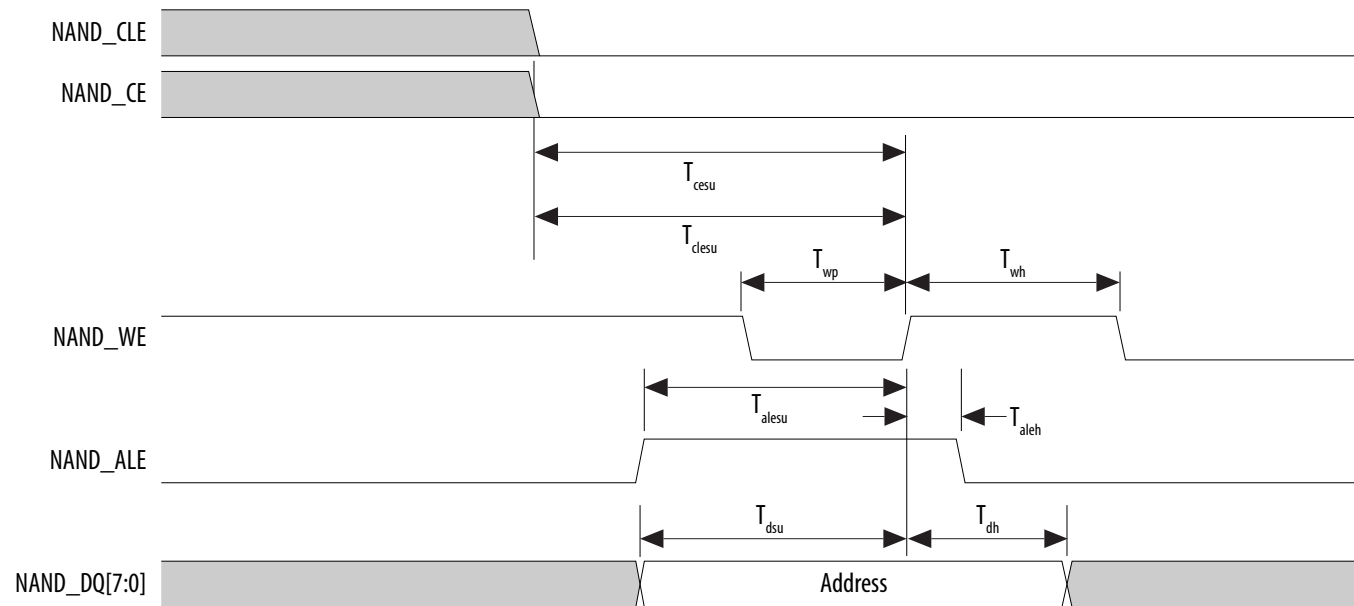
**Related Information****[SPI Controller, Arria V Hard Processor System Technical Reference Manual](#)**

Provides more information about rx\_sample\_delay.

**SD/MMC Timing Characteristics****Table 1-54: Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices**

After power up or cold reset, the Boot ROM uses `drvsel = 3` and `smplsel = 0` to execute the code. At the same time, the SD/MMC controller enters the Identification Phase followed by the Data Phase. During this time, the value of interface output clock `SDMMC_CLK_OUT` changes from a maximum of 400 kHz (Identification Phase) up to a maximum of 12.5 MHz (Data Phase), depending on the internal reference clock `SDMMC_CLK` and the `CSEL` setting. The value of `SDMMC_CLK` is based on the external oscillator frequency and has a maximum value of 50 MHz.

Figure 1-18: NAND Address Latch Timing Diagram



## FPP Configuration Timing when DCLK-to-DATA[] &gt;1

Table 1-67: FPP Timing Parameters When DCLK-to-DATA[] Ratio is &gt;1 for Arria V Devices

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
$t_{CF2CD}$	nCONFIG low to CONF_DONE low	—	600	ns
$t_{CF2ST0}$	nCONFIG low to nSTATUS low	—	600	ns
$t_{CFG}$	nCONFIG low pulse width	2	—	μs
$t_{STATUS}$	nSTATUS low pulse width	268	1506 <sup>(98)</sup>	μs
$t_{CF2ST1}$	nCONFIG high to nSTATUS high	—	1506 <sup>(99)</sup>	μs
$t_{CF2CK}^{(100)}$	nCONFIG high to first rising edge on DCLK	1506	—	μs
$t_{ST2CK}^{(100)}$	nSTATUS high to first rising edge of DCLK	2	—	μs
$t_{DSU}$	DATA[] setup time before rising edge on DCLK	5.5	—	ns
$t_{DH}$	DATA[] hold time after rising edge on DCLK	$N - 1/f_{DCLK}^{(101)}$	—	s
$t_{CH}$	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
$t_{CL}$	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
$t_{CLK}$	DCLK period	$1/f_{MAX}$	—	s
$f_{MAX}$	DCLK frequency (FPP ×8/ ×16)	—	125	MHz
$t_R$	Input rise time	—	40	ns
$t_F$	Input fall time	—	40	ns
$t_{CD2UM}$	CONF_DONE high to user mode <sup>(102)</sup>	175	437	μs

<sup>(98)</sup> This value can be obtained if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

<sup>(99)</sup> This value can be obtained if you do not delay configuration by externally holding nSTATUS low.

<sup>(100)</sup> If nSTATUS is monitored, follow the  $t_{ST2CK}$  specification. If nSTATUS is not monitored, follow the  $t_{CF2CK}$  specification.

<sup>(101)</sup>  $N$  is the DCLK-to-DATA[] ratio and  $f_{DCLK}$  is the DCLK frequency of the system.

<sup>(102)</sup> The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

**Related Information**

- [PS Configuration Timing](#) on page 1-81
- [AS Configuration Timing](#)  
Provides the AS configuration timing waveform.

## DCLK Frequency Specification in the AS Configuration Scheme

**Table 1-69: DCLK Frequency Specification in the AS Configuration Scheme**

This table lists the internal clock frequency specification for the AS configuration scheme. The DCLK frequency specification applies when you use the internal oscillator as the configuration clock source. The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Parameter	Minimum	Typical	Maximum	Unit
DCLK frequency in AS configuration scheme	5.3	7.9	12.5	MHz
	10.6	15.7	25.0	MHz
	21.3	31.4	50.0	MHz
	42.6	62.9	100.0	MHz

## PS Configuration Timing

**Table 1-70: PS Timing Parameters for Arria V Devices**

Symbol	Parameter	Minimum	Maximum	Unit
t <sub>CF2CD</sub>	nCONFIG low to CONF_DONE low	—	600	ns
t <sub>CF2ST0</sub>	nCONFIG low to nSTATUS low	—	600	ns
t <sub>CFG</sub>	nCONFIG low pulse width	2	—	μs
t <sub>STATUS</sub>	nSTATUS low pulse width	268	1506 <sup>(103)</sup>	μs
t <sub>CF2ST1</sub>	nCONFIG high to nSTATUS high	—	1506 <sup>(104)</sup>	μs

<sup>(103)</sup> You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

<sup>(104)</sup> You can obtain this value if you do not delay configuration by externally holding nSTATUS low.

Term	Definition
$t_{\text{FALL}}$	Signal high-to-low transition time (80–20%)
$t_{\text{INCCJ}}$	Cycle-to-cycle jitter tolerance on the PLL clock input
$t_{\text{OUTPJ\_IO}}$	Period jitter on the GPIO driven by a PLL
$t_{\text{OUTPJ\_DC}}$	Period jitter on the dedicated clock output driven by a PLL
$t_{\text{RISE}}$	Signal low-to-high transition time (20–80%)
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = $1 / (\text{Receiver Input Clock Frequency Multiplication Factor}) = t_c/w$ )
$V_{\text{CM(DC)}}$	DC common mode input voltage.
$V_{\text{ICM}}$	Input common mode voltage—The common mode of the differential signal at the receiver.
$V_{\text{ID}}$	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
$V_{\text{DIF(AC)}}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
$V_{\text{DIF(DC)}}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
$V_{\text{IH}}$	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
$V_{\text{IH(AC)}}$	High-level AC input voltage
$V_{\text{IH(DC)}}$	High-level DC input voltage
$V_{\text{IL}}$	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{\text{IL(AC)}}$	Low-level AC input voltage
$V_{\text{IL(DC)}}$	Low-level DC input voltage
$V_{\text{OCM}}$	Output common mode voltage—The common mode of the differential signal at the transmitter.
$V_{\text{OD}}$	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter.
$V_{\text{SWING}}$	Differential input voltage
$V_{\text{X}}$	Input differential cross point voltage

Symbol	Description	Conditions	Resistance Tolerance		Unit
			C3, I3L	C4, I4	
25-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCIO</sub> = 1.8 and 1.5 V	±40	±40	%
25-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCIO</sub> = 1.2 V	±50	±50	%
50-Ω R <sub>S</sub>	Internal series termination without calibration (50-Ω setting)	V <sub>CCIO</sub> = 1.8 and 1.5 V	±40	±40	%
50-Ω R <sub>S</sub>	Internal series termination without calibration (50-Ω setting)	V <sub>CCIO</sub> = 1.2 V	±50	±50	%
100-Ω R <sub>D</sub>	Internal differential termination (100-Ω setting)	V <sub>CCIO</sub> = 2.5 V	±25	±25	%

Figure 2-1: OCT Variation Without Re-Calibration for Arria V GZ Devices

$$R_{\text{OCT}} = R_{\text{SCAL}} \left( 1 + \left( \frac{dR}{dT} \times \Delta T \right) \pm \left( \frac{dR}{dV} \times \Delta V \right) \right)$$

Notes:

1. The R<sub>OCT</sub> value shows the range of OCT resistance with the variation of temperature and V<sub>CCIO</sub>.
2. R<sub>SCAL</sub> is the OCT resistance value at power-up.
3. ΔT is the variation of temperature with respect to the temperature at power-up.
4. ΔV is the variation of voltage with respect to the V<sub>CCIO</sub> at power-up.
5. dR/dT is the percentage change of R<sub>SCAL</sub> with temperature.
6. dR/dV is the percentage change of R<sub>SCAL</sub> with voltage.

Table 2-12: OCT Variation after Power-Up Calibration for Arria V GZ Devices

Valid for a V<sub>CCIO</sub> range of ±5% and a temperature range of 0° to 85°C.

## Hot Socketing

Table 2-14: Hot Socketing Specifications for Arria V GZ Devices

Symbol	Description	Maximum
$I_{IOPIN} (DC)$	DC current per I/O pin	300 $\mu A$
$I_{IOPIN} (AC)$	AC current per I/O pin	8 mA <sup>(124)</sup>
$I_{XCVR-TX} (DC)$	DC current per transceiver transmitter pin	100 mA
$I_{XCVR-RX} (DC)$	DC current per transceiver receiver pin	50 mA

## Internal Weak Pull-Up Resistor

Table 2-15: Internal Weak Pull-Up Resistor for Arria V GZ Devices

All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins. The internal weak pull-down feature is only available for the JTAG  $TCK$  pin. The typical value for this internal weak pull-down resistor is approximately 25 k $\Omega$ .

Symbol	Description	$V_{CCIO}$ Conditions (V) <sup>(125)</sup>	Value <sup>(126)</sup>	Unit
$R_{PU}$	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option.	3.0 $\pm 5\%$	25	k $\Omega$
		2.5 $\pm 5\%$	25	k $\Omega$
		1.8 $\pm 5\%$	25	k $\Omega$
		1.5 $\pm 5\%$	25	k $\Omega$
		1.35 $\pm 5\%$	25	k $\Omega$
		1.25 $\pm 5\%$	25	k $\Omega$
		1.2 $\pm 5\%$	25	k $\Omega$

<sup>(124)</sup> The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns,  $|I_{IOPIN}| = C dv/dt$ , in which C is the I/O pin capacitance and  $dv/dt$  is the slew rate.

<sup>(125)</sup> The pin pull-up resistance values may be lower if an external source drives the pin higher than  $V_{CCIO}$ .

<sup>(126)</sup> These specifications are valid with a  $\pm 10\%$  tolerance to cover changes over PVT.

I/O Standard	$V_{IL(DC)} (V)$		$V_{IH(DC)} (V)$		$V_{IL(AC)} (V)$	$V_{IH(AC)} (V)$	$V_{OL} (V)$	$V_{OH} (V)$	$I_{ol} (mA)$	$I_{oh} (mA)$
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-18 Class II	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCIO} + 0.3$	$V_{REF} - 0.25$	$V_{REF} + 0.25$	0.28	$V_{CCIO} - 0.28$	13.4	-13.4
SSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	8	-8
SSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	16	-16
SSTL-135 Class I, II	—	$V_{REF} - 0.09$	$V_{REF} + 0.09$	—	$V_{REF} - 0.16$	$V_{REF} + 0.16$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	—	—
SSTL-125 Class I, II	—	$V_{REF} - 0.85$	$V_{REF} + 0.85$	—	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	—	—
SSTL-12 Class I, II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	—	—
HSTL-18 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-18 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-12 Class I	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	16	-16
HSUL-12	—	$V_{REF} - 0.13$	$V_{REF} + 0.13$	—	$V_{REF} - 0.22$	$V_{REF} + 0.22$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	—	—



Symbol	V <sub>OD</sub> Setting	V <sub>OD</sub> Value (mV)	V <sub>OD</sub> Setting	V <sub>OD</sub> Value (mV)
V <sub>OD</sub> differential peak to peak typical	15	300	47	940
	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260

## DLL Range Specifications

**Table 2-47: DLL Range Specifications for Arria V GZ Devices**

Arria V GZ devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Parameter	C3, I3L	C4, I4	Unit
DLL operating frequency range	300 – 890	300 – 890	MHz

## DQS Logic Block Specifications

**Table 2-48: DQS Phase Offset Delay Per Setting for Arria V GZ Devices**

The typical value equals the average of the minimum and maximum values.

The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a –3 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is  $[625 \text{ ps} + (10 \times 11 \text{ ps}) \pm 20 \text{ ps}] = 735 \text{ ps} \pm 20 \text{ ps}$ .

Speed Grade	Min	Max	Unit
C3, I3L	8	15	ps
C4, I4	8	16	ps

**Table 2-49: DQS Phase Shift Error Specification for DLL-Delayed Clock ( $t_{\text{DQS\_PSERR}}$ ) for Arria V GZ Devices**

This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a –3 speed grade is  $\pm 84 \text{ ps}$  or  $\pm 42 \text{ ps}$ .

Number of DQS Delay Buffers	C3, I3L	C4, I4	Unit
1	30	32	ps
2	60	64	ps
3	90	96	ps

**Table 2-57: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1**

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
$t_{CF2CD}$	nCONFIG low to CONF_DONE low	—	600	ns
$t_{CF2ST0}$	nCONFIG low to nSTATUS low	—	600	ns
$t_{CFG}$	nCONFIG low pulse width	2	—	$\mu$ s
$t_{STATUS}$	nSTATUS low pulse width	268	1,506 <sup>(210)</sup>	$\mu$ s
$t_{CF2ST1}$	nCONFIG high to nSTATUS high	—	1,506 <sup>(211)</sup>	$\mu$ s
$t_{CF2CK}$ <sup>(212)</sup>	nCONFIG high to first rising edge on DCLK	1,506	—	$\mu$ s
$t_{ST2CK}$ <sup>(212)</sup>	nSTATUS high to first rising edge of DCLK	2	—	$\mu$ s
$t_{DSU}$	DATA[] setup time before rising edge on DCLK	5.5	—	ns
$t_{DH}$	DATA[] hold time after rising edge on DCLK	$N - 1/f_{DCLK}$ <sup>(213)</sup>	—	s
$t_{CH}$	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
$t_{CL}$	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
$t_{CLK}$	DCLK period	$1/f_{MAX}$	—	s
$f_{MAX}$	DCLK frequency (FPP $\times 8/\times 16$ )	—	125	MHz
	DCLK frequency (FPP $\times 32$ )	—	100	MHz
$t_R$	Input rise time	—	40	ns
$t_F$	Input fall time	—	40	ns
$t_{CD2UM}$	CONF_DONE high to user mode <sup>(214)</sup>	175	437	$\mu$ s

<sup>(210)</sup> You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

<sup>(211)</sup> You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

<sup>(212)</sup> If nSTATUS is monitored, follow the  $t_{ST2CK}$  specification. If nSTATUS is not monitored, follow the  $t_{CF2CK}$  specification.

<sup>(213)</sup> N is the DCLK-to-DATA ratio and  $f_{DCLK}$  is the DCLK frequency the system is operating.

<sup>(214)</sup> The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

## Related Information

## Configuration, Design Security, and Remote System Upgrades in Arria V Devices

## Initialization

Table 2-61: Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices

Initialization Clock Source	Configuration Schemes	Maximum Frequency (MHz)	Minimum Number of Clock Cycles
Internal Oscillator	AS, PS, FPP	12.5	8576
CLKUSR <sup>(222)</sup>	PS, FPP	125	
	AS	100	
DCLK	PS, FPP	125	

## Configuration Files

Use the following table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (.hex) or tabular text file (.tcf) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size.

<sup>(221)</sup> To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the “Initialization” section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

<sup>(222)</sup> To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** panel of the **Device and Pin Options** dialog box.

**Related Information**

- [Configuration, Design Security, and Remote System Upgrades in Arria V Devices](#)  
For more information about the reconfiguration input for the ALTREMOTE\_UPDATE IP core, refer to the “User Watchdog Timer” section.
- [Configuration, Design Security, and Remote System Upgrades in Arria V Devices](#)  
For more information about the `reset_timer` input for the ALTREMOTE\_UPDATE IP core, refer to the “Remote System Upgrade State Machine” section.

## User Watchdog Internal Oscillator Frequency Specification

**Table 2-65: User Watchdog Internal Oscillator Frequency Specifications**

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz

## I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

**Related Information**

[Arria V Devices Documentation page](#)

For the Excel-based I/O Timing spreadsheet

<sup>(226)</sup> This is equivalent to strobing the reconfiguration input of the ALTREMOTE\_UPDATE IP core high for the minimum timing specification. For more information, refer to the “Remote System Upgrade State Machine” section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

<sup>(227)</sup> This is equivalent to strobing the `reset_timer` input of the ALTREMOTE\_UPDATE IP core high for the minimum timing specification. For more information, refer to the “User Watchdog Timer” section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.