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Understanding Embedded - FPGAs (Field Programmable Gate Array)

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	19811
Number of Logic Elements/Cells	420000
Total RAM Bits	23625728
Number of I/O	704
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxfb5k6f40c6n

Caution: Conditions outside the range listed in the following table may cause permanent damage tothe device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1-1: Absolute Maximum Ratings for Arria V Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Core voltage power supply	–0.50	1.43	V
V_{CCP}	Periphery circuitry, PCIe® hardIP block, and transceiver physical coding sublayer (PCS) power supply	–0.50	1.43	V
V_{CCPGM}	Configuration pins power supply	–0.50	3.90	V
V_{CC_AUX}	Auxiliary supply	–0.50	3.25	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	–0.50	3.90	V
V_{CCPD}	I/O pre-driver power supply	–0.50	3.90	V
V_{CCIO}	I/O power supply	–0.50	3.90	V
V_{CCD_FPLL}	Phase-locked loop (PLL) digital power supply	–0.50	1.80	V
V_{CCA_FPLL}	PLL analog power supply	–0.50	3.25	V
V_{CCA_GXB}	Transceiver high voltage power	–0.50	3.25	V
V_{CCH_GXB}	Transmitter output buffer power	–0.50	1.80	V
V_{CCR_GXB}	Receiver power	–0.50	1.50	V
V_{CCT_GXB}	Transmitter power	–0.50	1.50	V
V_{CCL_GXB}	Transceiver clock network power	–0.50	1.50	V
V_I	DC input voltage	–0.50	3.80	V
V_{CC_HPS}	HPS core voltage and periphery circuitry power supply	–0.50	1.43	V
V_{CCPD_HPS}	HPS I/O pre-driver power supply	–0.50	3.90	V
V_{CCIO_HPS}	HPS I/O power supply	–0.50	3.90	V
$V_{CCRSTCLK\_HPS}$	HPS reset and clock input pins power supply	–0.50	3.90	V

Table 1-21: Transceiver Clocks Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
`fixedclk` clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	MHz
Transceiver Reconfiguration Controller IP (`mgmt_clk_clk`) clock frequency	—	75	—	125	75	—	125	MHz

Table 1-22: Receiver Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported I/O standards	1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS							
Data rate[28]	—	611	—	6553.6	611	—	3125	Mbps
Absolute V_{MAX} for a receiver pin[29]	—	—	—	1.2	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	–0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	—	—	—	2.2	—	—	2.2	V

(28) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.
(29) The device cannot tolerate prolonged operation at this absolute maximum.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Differential on-chip termination resistors	85-Ω setting	—	85	—	Ω
	100-Ω setting	—	100	—	Ω
	120-Ω setting	—	120	—	Ω
	150-Ω setting	—	150	—	Ω
Intra-differential pair skew	TX V_{CM} = 0.65 V (AC coupled) and slew rate of 15 ps	—	—	15	ps
Intra-transceiver block transmitter channel-to-channel skew	×6 PMA bonded mode	—	—	180	ps
Inter-transceiver block transmitter channel-to-channel skew[55]	×*N* PMA bonded mode	—	—	500	ps

Table 1-30: CMU PLL Specifications for Arria V GT and ST Devices

Symbol/Description	Transceiver Speed Grade 3		Unit
	Min	Max	
Supported data range	0.611	10.3125	Gbps
fPLL supported data range	611	3125	Mbps

[55] This specification is only applicable to channels on one side of the device across two transceiver banks.

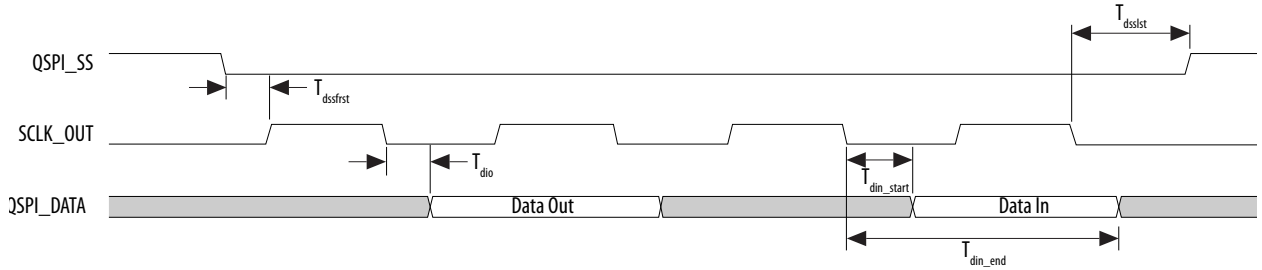
Symbol	Condition	–I3, –C4			–I5, –C5			–C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{x\ Jitter}$ -Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate 600 Mbps – 1.25 Gbps	—	—	260	—	—	300	—	—	350	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.16	—	—	0.18	—	—	0.21	UI
$t_{x\ Jitter}$ -Emulated Differential I/O Standards with One External Output Resistor Network	—	—	—	0.15	—	—	0.15	—	—	0.15	UI
t_{DUTY}	TX output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	%
t_{RISE} and t_{FALL}	True Differential I/O Standards[82]	—	—	160	—	—	180	—	—	200	ps
	Emulated Differential I/O Standards with Three External Output Resistor Network	—	—	250	—	—	250	—	—	300	ps
	Emulated Differential I/O Standards with One External Output Resistor Network	—	—	500	—	—	500	—	—	500	ps

(82) This applies to default pre-emphasis and V_{OD} settings only.

Symbol	Description	Min	Typ	Max	Unit
T_{din_end}	Input data valid end	$(2 + R_{delay}) \times T_{qspi\_clk} - 1.21$ (85)	—	—	ns

Figure 1-8: Quad SPI Flash Timing Diagram

This timing diagram illustrates clock polarity mode 0 and clock phase mode 0.



Related Information

Quad SPI Flash Controller Chapter, Arria V Hard Processor System Technical Reference Manual
Provides more information about Rdelay.

SPI Timing Characteristics

Table 1-52: SPI Master Timing Requirements for Arria V Devices

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

Symbol	Description	Min	Max	Unit
T_{clk}	CLK clock period	16.67	—	ns
T_{su}	SPI Master-in slave-out (MISO) setup time	8.35 (86)	—	ns

(85) R_{delay} is set by programming the register `qspiregs.rddatacap`. For the SoC EDS software version 13.1 and later, Altera provides automatic Quad SPI calibration in the preloader. For more information about R_{delay}, refer to the Quad SPI Flash Controller chapter in the Arria V Hard Processor System Technical Reference Manual.

After the Boot ROM code exits and control is passed to the preloader, software can adjust the value of `drvsel` and `smplsel` via the system manager. `drvsel` can be set from 1 to 7 and `smplsel` can be set from 0 to 7. While the preloader is executing, the values for `SDMMC_CLK` and `SDMMC_CLK_OUT` increase to a maximum of 200 MHz and 50 MHz respectively.

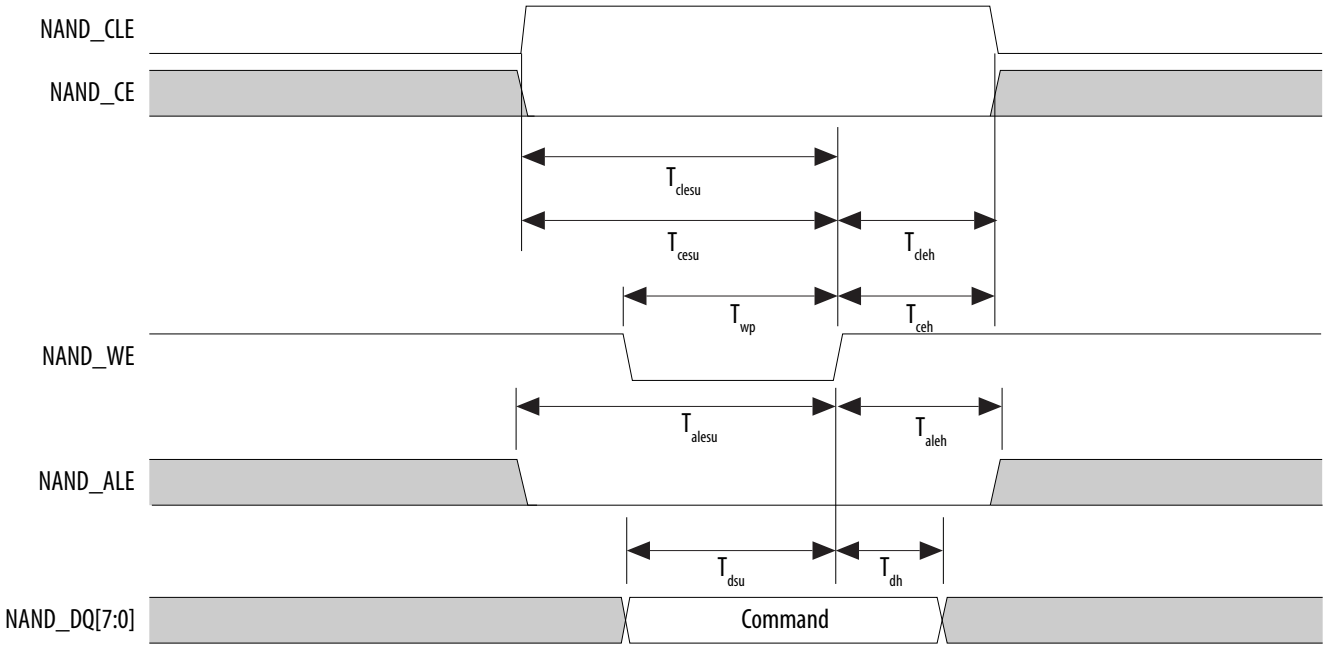
The SD/MMC interface calibration support will be available in a future release of the preloader through the SoC EDS software update.

Symbol	Description	Min	Max	Unit
T_{sdmmc_clk} (internal reference clock)	SDMMC_CLK clock period (Identification mode)	20	—	ns
	SDMMC_CLK clock period (Default speed mode)	5	—	ns
	SDMMC_CLK clock period (High speed mode)	5	—	ns
$T_{sdmmc\_clk\_out}$ (interface output clock)	SDMMC_CLK_OUT clock period (Identification mode)	2500	—	ns
	SDMMC_CLK_OUT clock period (Default speed mode)	40	—	ns
	SDMMC_CLK_OUT clock period (High speed mode)	20	—	ns
$T_{dutycycle}$	SDMMC_CLK_OUT duty cycle	45	55	%
T_d	SDMMC_CMD/SDMMC_D output delay	(T_{sdmmc_clk} × `drvsel`)/2 – 1.23 (87)	(T_{sdmmc_clk} × `drvsel`)/2 + 1.69 (87)	ns
T_{su}	Input setup time	1.05 – (T_{sdmmc_clk} × `smplsel`)/2 (88)	—	ns
T_h	Input hold time	(T_{sdmmc_clk} × `smplsel`)/2 (88)	—	ns

(87) `drvsel` is the drive clock phase shift select value.
(88) `smplsel` is the sample clock phase shift select value.

Symbol	Description	Min	Max	Unit
T_{dh} (89)	Data to write enable hold time	5	—	ns
T_{cea}	Chip enable to data access time	—	25	ns
T_{rea}	Read enable to data access time	—	16	ns
T_{rhz}	Read enable to data high impedance	—	100	ns
T_{rr}	Ready to read enable low	20	—	ns

Figure 1-17: NAND Command Latch Timing Diagram



Symbol	Parameter	Minimum	Maximum	Unit
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} × CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

FPP Configuration Timing
Provides the FPP configuration timing waveforms.

AS Configuration Timing

Table 1-68: AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices

The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

The t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in PS Timing Parameters for Arria V Devices table. You can obtain the t_{CF2ST1} value if you do not delay configuration by externally holding nSTATUS low.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	2	ns
t_{SU}	Data setup time before the falling edge on DCLK	1.5	—	ns
t_{DH}	Data hold time after the falling edge on DCLK	0	—	ns
t_{CD2UM}	CONF_DONE high to user mode	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} × CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Date	Version	Changes
August 2013	3.5	• Removed "Pending silicon characterization" note in Table 29. • Updated Table 25.
August 2013	3.4	• Removed Preliminary tags for Table 1, Table 2, Table 3, Table 4, Table 5, Table 6, Table 7, Table 9, Table 12, Table 13, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, Table 21, Table 22, Table 23, Table 24, Table 25, Table 26, Table 27, Table 28, Table 29, Table 30, Table 31, Table 35, Table 36, Table 51, Table 53, Table 54, Table 55, Table 56, Table 57, Table 60, Table 62, and Table 64. • Updated Table 1, Table 3, Table 11, Table 19, Table 20, Table 21, Table 22, Table 25, and Table 29.
June 2013	3.3	Updated Table 20, Table 21, Table 25, and Table 38.
May 2013	3.2	• Added Table 37. • Updated Figure 8, Figure 9, Figure 20, Figure 22, and Figure 23. • Updated Table 1, Table 5, Table 10, Table 13, Table 19, Table 20, Table 21, Table 23, Table 29, Table 39, Table 40, Table 46, Table 56, Table 57, Table 60, and Table 64. • Updated industrial junction temperature range for –I3 speed grade in "PLL Specifications" section.
March 2013	3.1	• Added HPS reset information in the "HPS Specifications" section. • Added Table 60. • Updated Table 1, Table 3, Table 17, Table 20, Table 29, and Table 59. • Updated Figure 21.

Date	Version	Changes

November 2012	3.0	• Updated Table 2, Table 4, Table 9, Table 14, Table 16, Table 17, Table 20, Table 21, Table 25, Table 29, Table 36, Table 56, Table 57, and Table 60.
		• Removed table: Transceiver Block Jitter Specifications for Arria V Devices.
		• Added HPS information:
		  • Added "HPS Specifications" section.
		  • Added Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, and Table 50.
		  • Added Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19.
		  • Updated Table 3 and Table 5.

October 2012	2.4	• Updated Arria V GX $V_{CCR\_GXBL/R}$, $V_{CCT\_GXBL/R}$, and $V_{CCL\_GXBL/R}$ minimum and maximum values, and data rate in Table 4. • Added receiver V_{ICM} (AC coupled) and V_{ICM} (DC coupled) values, and transmitter V_{OCM} (AC coupled) and V_{OCM} (DC coupled) values in Table 20 and Table 21.
August 2012	2.3	Updated the SERDES factor condition in Table 30.
July 2012	2.2	• Updated the maximum voltage for V_I (DC input voltage) in Table 1. • Updated Table 20 to include the Arria V GX -I3 speed grade. • Updated the minimum value of the fixedclk clock frequency in Table 20 and Table 21. • Updated the SERDES factor condition in Table 30. • Updated Table 50 to include the IOE programmable delay settings for the Arria V GX -I3 speed grade.
June 2012	2.1	Updated $V_{CCR\_GXBL/R}$, $V_{CCT\_GXBL/R}$, and $V_{CCL\_GXBL/R}$ values in Table 4.

Date	Version	Changes
June 2012	2.0	• Updated for the Quartus II software v12.0 release: • Restructured document. • Updated "Supply Current and Power Consumption" section. • Updated Table 20, Table 21, Table 24, Table 25, Table 26, Table 35, Table 39, Table 43, and Table 52. • Added Table 22, Table 23, and Table 33. • Added Figure 1–1 and Figure 1–2. • Added "Initialization" and "Configuration Files" sections.
February 2012	1.3	• Updated Table 2–1. • Updated Transceiver-FPGA Fabric Interface rows in Table 2–20. • Updated V_{CCP} description.
December 2011	1.2	Updated Table 2–1 and Table 2–3.
November 2011	1.1	• Updated Table 2–1, Table 2–19, Table 2–26, and Table 2–36. • Added Table 2–5. • Added Figure 2–4.
August 2011	1.0	Initial release.

Transceiver Power Supply Requirements

Table 2-7: Transceiver Power Supply Voltage Requirements for Arria V GZ Devices

Conditions	VCCR_GXB and VCCT_GXB (122)	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true: • Data rate > 10.3 Gbps. • DFE is used.	1.05	3.0	1.5	V
If ANY of the following conditions are true (123) : • ATX PLL is used. • Data rate > 6.5Gbps. • DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used.	1.0			
If ALL of the following conditions are true: • ATX PLL is not used. • Data rate ≤ 6.5Gbps. • DFE, AEQ, and EyeQ are not used.	0.85	2.5		

DC Characteristics

Supply Current

Standby current is the current drawn from the respective power rails used for power budgeting.

Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

(122) If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to 0.85 V, they can be shared with the VCC core supply.

(123) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

I/O Standard Specifications

The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

Table 2-16: Single-Ended I/O Standards for Arria V GZ Devices

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.4	2.4	2	–2
LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.6	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2

Table 2-17: Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V GZ Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × VCCIO	0.51 × V_{CCIO}

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{ICM} (AC and DC coupled)	V_{CCR_GXB} = 0.85 V full bandwidth	—	600	—	—	600	—	mV
	V_{CCR_GXB} = 0.85 V half bandwidth	—	600	—	—	600	—	mV
	V_{CCR_GXB} = 1.0 V full bandwidth	—	700	—	—	700	—	mV
	V_{CCR_GXB} = 1.0 V half bandwidth	—	700	—	—	700	—	mV
t_{LTR} (149)	—	—	—	10	—	—	10	µs
t_{LTD} (150)	—	4	—	—	4	—	—	µs
t_{LTD_manual} (151)	—	4	—	—	4	—	—	µs
$t_{LTR\_LTD\_manual}$ (152)	—	15	—	—	15	—	—	µs
Programmable equalization (AC Gain)	Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz)	—	—	16	—	—	16	dB

(149) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
(150) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.
(151) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.
(152) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

CMU PLL

Table 2-26: CMU PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported data range	—	600	—	12500	600	—	10312.5	Mbps
$t_{pll\_powerdown}$ (153)	—	1	—	—	1	—	—	µs
t_{pll_lock} (154)	—		—	10	—	—	10	µs

Related Information

Arria V Device Overview

For more information about device ordering codes.

ATX PLL

Table 2-27: ATX PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

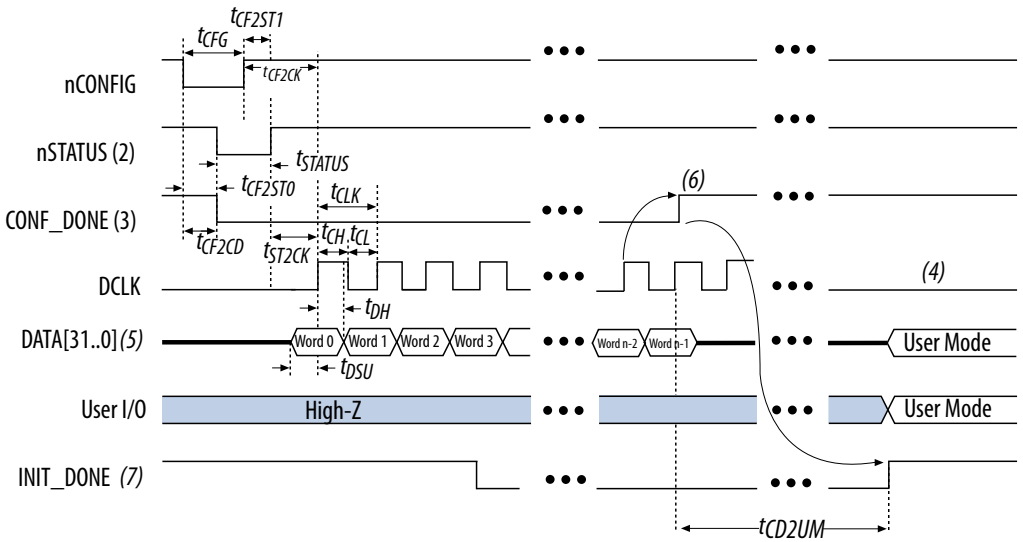
(153) $t_{pll\_powerdown}$ is the PLL powerdown minimum pulse width.

(154) t_{pll_lock} is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

FPP Configuration Timing when DCLK to DATA[] = 1

Figure 2-7: FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1

Timing waveform for FPP configuration when using a MAX® II or MAX V device as an external host.



Notes:
1. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
2. After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.
3. After power-up, before and during configuration, CONF_DONE is low.
4. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
5. For FPP ×16, use DATA[15..0]. For FPP ×8, use DATA[7..0]. DATA[31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high when the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
7. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Note: When you enable the decompression or design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8, FPP ×16, and FPP ×32. For the respective DCLK-to-DATA[] ratio, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.

Table 2-56: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1

Use these timing parameters when the decompression and design security features are disabled.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1,506 (205)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 (206)	µs
t_{CF2CK} (207)	nCONFIG high to first rising edge on DCLK	1,506	—	µs
t_{ST2CK} (207)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16)	—	125	MHz
	DCLK frequency (FPP ×32)	—	100	MHz
t_{CD2UM}	CONF_DONE high to user mode (208)	175	437	µs

(205) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(206) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.
(207) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Table 2-57: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1,506 (210)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 (211)	µs
t_{CF2CK} (212)	nCONFIG high to first rising edge on DCLK	1,506	—	µs
t_{ST2CK} (212)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N-1/f_{DCLK}$ (213)	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16)	—	125	MHz
	DCLK frequency (FPP ×32)	—	100	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode (214)	175	437	µs

(210) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(211) You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.
(212) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.
(213) N is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.
(214) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

Related Information

Configuration, Design Security, and Remote System Upgrades in Arria V Devices

Initialization

Table 2-61: Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices

Initialization Clock Source	Configuration Schemes	Maximum Frequency (MHz)	Minimum Number of Clock Cycles
Internal Oscillator	AS, PS, FPP	12.5	8576
CLKUSR (222)	PS, FPP	125	
	AS	100	
DCLK	PS, FPP	125	

Configuration Files

Use the following table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (`.hex`) or tabular text file (`.ttf`) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size.

(221) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

(222) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** panel of the **Device and Pin Options** dialog box.

Table 2-62: Uncompressed .rbf Sizes for Arria V GZ Devices

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) (223)
Arria V GZ	E1	137,598,880	562,208
	E3	137,598,880	562,208
	E5	213,798,880	561,760
	E7	213,798,880	561,760

Table 2-63: Minimum Configuration Time Estimation for Arria V GZ Devices

Variant	Member Code	Active Serial (224)			Fast Passive Parallel (225)		
		Width	DCLK (MHz)	Min Config Time (ms)	Width	DCLK (MHz)	Min Config Time (ms)
Arria V GZ	E1	4	100	344	32	100	43
	E3	4	100	344	32	100	43
	E5	4	100	534	32	100	67
	E7	4	100	534	32	100	67

Remote System Upgrades Circuitry Timing Specification

Table 2-64: Remote System Upgrade Circuitry Timing Specifications

Parameter	Minimum	Maximum	Unit
$t_{RU\_nCONFIG}$ (226)	250	—	ns
$t_{RU\_nRSTIMER}$ (227)	250	—	ns

(223) The IOCSR **.rbf** size is specifically for the Configuration via Protocol (CvP) feature.
(224) DCLK frequency of 100 MHz using external CLKUSR.
(225) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.