Intel - 5AGXFB7H4F35C4N Datasheet





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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	23780
Number of Logic Elements/Cells	504000
Total RAM Bits	27695104
Number of I/O	544
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxfb7h4f35c4n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

AV-51002 2017.02.10

Symbol	Description	Condition (V)	Ca	Unit		
Symbol			-I3, -C4	–I5, –C5	-C6	Ont
60- Ω and 120- Ω R_{T}	Internal parallel termination with calibration (60- Ω and 120- Ω setting)	$V_{CCIO} = 1.2$	-10 to +40	-10 to +40	-10 to +40	%
25- $\Omega R_{S_left_shift}$	Internal left shift series termination with calibration (25- $\Omega R_{s_left_shift}$ setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%

OCT Without Calibration Resistance Tolerance Specifications

Table 1-9: OCT Without Calibration Resistance Tolerance Specifications for Arria V Devices

This table lists the Arria V OCT without calibration resistance to PVT changes.

Symbol	Description	Condition (V/)	Re	Unit		
Symbol	Description		–I3, –C4	–I5, –C5	-C6	Ont
$25-\Omega R_S$	Internal series termination without calibration (25- Ω setting)	V _{CCIO} = 3.0, 2.5	±30	±40	±40	%
25-Ω R _S	Internal series termination without calibration (25- Ω setting)	V _{CCIO} = 1.8, 1.5	±30	±40	±40	%
$25-\Omega R_S$	Internal series termination without calibration (25- Ω setting)	$V_{CCIO} = 1.2$	±35	±50	±50	%
50-Ω R _S	Internal series termination without calibration (50- Ω setting)	V _{CCIO} = 3.0, 2.5	±30	±40	±40	%
50-Ω R _S	Internal series termination without calibration (50- Ω setting)	V _{CCIO} = 1.8, 1.5	±30	±40	±40	%
50-Ω R _S	Internal series termination without calibration (50- Ω setting)	$V_{CCIO} = 1.2$	±35	±50	±50	%
100-Ω R _D	Internal differential termination $(100-\Omega \text{ setting})$	$V_{CCIO} = 2.5$	±25	±40	±40	%



Table 1-21: Transceiver Clocks Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4		Transceiver Speed Grade 6			Unit	
Symbol/Description		Min	Тур	Max	Min	Тур	Max	Onit
fixedclk clock frequency	PCIe Receiver Detect	_	125	_	_	125	_	MHz
Transceiver Reconfigura- tion Controller IP (mgmt_ clk_clk) clock frequency	_	75	_	125	75	_	125	MHz

Table 1-22: Receiver Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4		Transceiver Speed Grade 6			l ln it	
Symbol/Description	Condition	Min	Тур	Max	Min	Тур	Max	Onit
Supported I/O standards		1	.5 V PCML,	2.5 V PCML,	LVPECL, an	d LVDS		
Data rate ⁽²⁸⁾		611	—	6553.6	611	—	3125	Mbps
Absolute V_{MAX} for a receiver pin ⁽²⁹⁾	_		_	1.2		—	1.2	V
Absolute V _{MIN} for a receiver pin	_	-0.4	_		-0.4	—	—	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) before device configuration	_	_		1.6		_	1.6	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) after device configuration	_	_	_	2.2		_	2.2	V



 ⁽²⁸⁾ To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.
 ⁽²⁹⁾ The device cannot tolerate prolonged operation at this absolute maximum.

Table 1-57: RGMII RX Timing Requirements for Arria V Devices

Symbol	Description	Min	Тур	Unit
T _{clk} (1000Base-T)	RX_CLK clock period		8	ns
T _{clk} (100Base-T)	RX_CLK clock period		40	ns
T _{clk} (10Base-T)	RX_CLK clock period		400	ns
T _{su}	RX_D/RX_CTL setup time	1		ns
T _h	RX_D/RX_CTL hold time	1		ns

Figure 1-14: RGMII RX Timing Diagram



Table 1-58: Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices

Symbol	Description	Min	Тур	Мах	Unit
T _{clk}	MDC clock period	—	400	_	ns
T _d	MDC to MDIO output data delay	10		20	ns
T _s	Setup time for MDIO data	10	_		ns
T _h	Hold time for MDIO data	0			ns



Symbol	Parameter	Minimum	Maximum	Unit
t _{STATUS}	nSTATUS low pulse width	268	1506 ⁽⁹⁴⁾	μs
t _{CF2ST1}	nCONFIG high to nSTATUS high	—	1506 ⁽⁹⁵⁾	μs
t _{CF2CK} ⁽⁹⁶⁾	nCONFIG high to first rising edge on DCLK	1506	—	μs
t _{ST2CK} ⁽⁹⁶⁾	nSTATUS high to first rising edge of DCLK	2		μs
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t _{DH}	DATA[] hold time after rising edge on DCLK	0		ns
t _{CH}	DCLK high time	$0.45 imes 1/f_{MAX}$	—	S
t _{CL}	DCLK low time	$0.45 imes 1/f_{ m MAX}$	—	S
t _{CLK}	DCLK period	1/f _{MAX}	—	S
f _{MAX}	DCLK frequency (FPP ×8/ ×16)	_	125	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽⁹⁷⁾	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	4× maximum DCLK period	_	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + ($T_{init} \times CLKUSR$ period)	_	_
T _{init}	Number of clock cycles required for device initialization	8,576	_	Cycles

Related Information

FPP Configuration Timing

Provides the FPP configuration timing waveforms.



⁽⁹⁴⁾ You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.

⁽⁹⁵⁾ You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

⁽⁹⁶⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

⁽⁹⁷⁾ The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

1-80 AS Configuration Timing

Symbol	Parameter	Minimum	Maximum	Unit
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times maximum$ DCLK period	—	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + ($T_{init} \times CLKUSR$ period)		
T _{init}	Number of clock cycles required for device initialization	8,576		Cycles

Related Information

FPP Configuration Timing

Provides the FPP configuration timing waveforms.

AS Configuration Timing

Table 1-68: AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices

The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

The t_{CF2CD} , t_{CF2ST0} , t_{CFG} , t_{STATUS} , and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in PS Timing Parameters for Arria V Devices table. You can obtain the t_{CF2ST1} value if you do not delay configuration by externally holding nSTATUS low.

Symbol	Parameter	Minimum	Maximum	Unit
t _{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	2	ns
t _{SU}	Data setup time before the falling edge on DCLK	1.5		ns
t _{DH}	Data hold time after the falling edge on DCLK	0	_	ns
t _{CD2UM}	CONF_DONE high to user mode	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	_	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + ($T_{init} \times CLKUSR$ period)	_	—
T _{init}	Number of clock cycles required for device initialization	8,576		Cycles







2-4 Recommended Operating Conditions

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle.

For example, a signal that overshoots to 3.95 V can be at 3.95 V for only $\sim 21\%$ over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~ 2 years.

Table 2-4: Maximum Allowed Overshoot During Transitions for Arria V GZ Devices
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Symbol	Description	Condition (V)	Overshoot Duration as % @ T」= 100°C	Unit
		3.8	100	%
		3.85	64	%
		3.9	36	%
		3.95	21	%
Vi (AC)	AC input voltage	4	12	%
	-	4.05	7	%
		4.1	4	%
		4.15	2	%
		4.2	1	%

Recommended Operating Conditions

Table 2-5: Recommended Operating Conditions for Arria V GZ Devices

Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum ⁽¹¹⁴⁾	Typical	Maximum ⁽¹¹⁴⁾	Unit
V _{CC}	Core voltage and periphery circuitry power supply ⁽¹¹⁵⁾	—	0.82	0.85	0.88	V

⁽¹¹⁴⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.





⁽¹¹⁵⁾ The V_{CC} core supply must be set to 0.9 V if the Partial Reconfiguration (PR) feature is used.

Symbol	Description	Condition	Minimum ⁽¹¹⁴⁾	Typical	Maximum ⁽¹¹⁴⁾	Unit
V _{CCPT}	Power supply for programmable power technology	—	1.45	1.50	1.55	V
V _{CC_AUX}	Auxiliary supply for the programmable power technology	_	2.375	2.5	2.625	V
V _{CCPD} (116	I/O pre-driver (3.0 V) power supply	_	2.85	3.0	3.15	V
)	I/O pre-driver (2.5 V) power supply	_	2.375	2.5	2.625	V
	I/O buffers (3.0 V) power supply	_	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	_	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	_	1.71	1.8	1.89	V
V _{CCIO}	I/O buffers (1.5 V) power supply	_	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply	_	1.283	1.35	1.45	V
	I/O buffers (1.25 V) power supply	_	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply		1.14	1.2	1.26	V
	Configuration pins (3.0 V) power supply	_	2.85	3.0	3.15	V
V _{CCPGM}	Configuration pins (2.5 V) power supply	_	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply		1.71	1.8	1.89	V
V _{CCA} _	PLL analog voltage regulator power supply		2.375	2.5	2.625	V
V _{CCD} FPLL	PLL digital voltage regulator power supply	_	1.45	1.5	1.55	V
V _{CCBAT} (117	Battery back-up power supply (For design security volatile key register)		1.2		3.0	V

⁽¹¹⁴⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements.
Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.



⁽¹¹⁶⁾ V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V.

⁽¹¹⁷⁾ If you do not use the design security feature in Arria V GZ devices, connect V_{CCBAT} to a 1.2- to 3.0-V power supply. Arria V GZ power-on-reset (POR) circuitry monitors V_{CCBAT}. Arria V GZ devices do not exit POR if V_{CCBAT} is not powered up.

Symbol	Description	Condition	Minimum ⁽¹¹⁴⁾	Typical	Maximum ⁽¹¹⁴⁾	Unit
VI	DC input voltage	_	-0.5	_	3.6	V
Vo	Output voltage		0		V _{CCIO}	V
 Т_	Operating junction temperature	Commercial	0		85	°C
1 j	Operating junction temperature	Industrial	-40	_	100	°C
t	Power supply ramp time	Standard POR	200 µs	_	100 ms	
•RAMP		Fast POR	200 µs	—	4 ms	—

Recommended Transceiver Power Supply Operating Conditions

Table 2-6: Recommended Transceiver Power Supply Operating Conditions for Arria V GZ Devices

Symbol	Description	Minimum ⁽¹¹⁸⁾	Typical	Maximum ⁽¹¹⁸⁾	Unit
V _{CCA_GXBL}	Transceiver channel DLL nevver supply (left side)	2.85	3.0	3.15	V
(119), (120)	Transceiver channel PLL power supply (left side)	2.375	2.5	2.625	v
V _{CCA}	Transceiver channel DL newer supply (right side)	2.85	3.0	3.15	V
GXBR ⁽¹¹⁹⁾ , ⁽¹²⁰⁾	Transceiver channel FLL power supply (fight side)	2.375	2.5	2.625	v
V _{CCHIP_L}	Transceiver hard IP power supply (left side)	0.82	0.85	0.88	V
V _{CCHSSI_L}	Transceiver PCS power supply (left side)	0.82	0.85	0.88	V
V _{CCHSSI_R}	Transceiver PCS power supply (right side)	0.82	0.85	0.88	V

⁽¹¹⁴⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹¹⁸⁾ This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹²⁰⁾ When using ATX PLLs, the supply must be 3.0 V.



⁽¹¹⁹⁾ This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

Bus Hold Specifications

Table 2-9: Bus Hold Parameters for Arria V GZ Devices

							۷ _C	CIO					
Parameter	Symbol	Conditions	1.2	2 V	1.5	5 V	1.8	3 V	2.5	5 V	3.0	V	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I _{SUSL}	V _{IN} > V _{IL} (maximum)	22.5	_	25.0	_	30.0		50.0	_	70.0	_	μΑ
High sustaining current	I _{SUSH}	V _{IN} < V _{IH} (minimum)	-22.5	_	-25.0	_	-30.0	_	-50.0	_	-70.0	_	μΑ
Low overdrive current	I _{ODL}	$0V < V_{IN} < V_{CCIO}$	_	120	_	160	_	200	_	300	_	500	μΑ
High overdrive current	I _{ODH}	$0V < V_{IN} < V_{CCIO}$	—	-120	_	-160	_	-200		-300	_	-500	μΑ
Bus-hold trip point	V _{TRIP}		0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block.

Table 2-10: OCT Calibration Accuracy Specifications for Arria V GZ Devices

OCT calibration accuracy is valid at the time of calibration only.





Symbol	Description	V _{CCIO} (V)	Typical	Unit
		3.0	0.0297	
dR/dV		2.5	0.0344	
	OCT variation with voltage without re-calibration	1.8	0.0499	%/mV
		1.5	0.0744	
		1.2	0.1241	
		3.0	0.189	
		2.5	0.208	
dR/dT	OCT variation with temperature without re-calibration	1.8	0.266	%/°C
		1.5	0.273	
		1.2	0.317	

Pin Capacitance

Table 2-13: Pin Capacitance for Arria V GZ Devices

Symbol	Description	Maximum	Unit
C _{IOTB}	Input capacitance on the top and bottom I/O pins	6	pF
C _{IOLR}	Input capacitance on the left and right I/O pins	6	pF
C _{OUTFB}	Input capacitance on dual-purpose clock output and feedback pins	6	pF



I/O Standard	V _{CCIO} (V)		V _{DIF}	_(DC) (V)		$V_{X(AC)}(V)$ $V_{CM(DC)}(V)$)	V _{DIF(AC)} (V)				
	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Max
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V _{CCIO} + 0.3		$0.5 \times V_{CCIO}$	_	$0.4 \times V_{\rm CCIO}$	0.5 × V _{CC} IO	$0.6 \times V_{CCIO}$	0.3	V _{CCIO} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5 × V _{CCIO} – 0.12	$0.5 \times V_{CCIO}$	$0.5 \times V_{CCIO} + 0.12$	$0.4 \times V_{CCIO}$	0.5 × V _{CC} IO	0.6 × V _{CCIO}	0.44	0.44

Table 2-21: Differential I/O Standard Specifications for Arria V GZ Devices

I/O Standard	Vc	_{:CIO} (V) ⁽	128)		V _{ID} (mV) ⁽¹²⁹⁾		V _{ICM(DC)} (V) V _{OD}			_D (V) ⁽¹³	0)	V _{OCM} (V) ⁽¹³⁰⁾			
	Min	Тур	Max	Min	Condition	Max	Min	Condition	Max	Min	Тур	Max	Min	Тур	Max
PCML	Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to the "Transceiver Performance Specifications" section.														
2.5 V LVDS 2 (131)	2 375	25	2 625	100	V _{CM} =		0.05	D _{MAX} ≤ 700 Mbps	1.8	0.247	—	0.6	1.125	1.25	1.375
	2.375	2.5	2.025	100	1.25 V		1.05	D _{MAX} > 700 Mbps	1.55	0.247	—	0.6	1.125	1.25	1.375
BLVDS (132)	2.375	2.5	2.625	100						_	_			—	

⁽¹²⁸⁾ Differential inputs are powered by VCCPD which requires 2.5 V.



⁽¹²⁹⁾ The minimum VID value is applicable over the entire common mode range, VCM.

⁽¹³⁰⁾ RL range: $90 \le \text{RL} \le 110 \Omega$.

⁽¹³¹⁾ For optimized LVDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.

 $^{^{(132)}}$ There are no fixed V_{ICM}, V_{OD}, and V_{OCM} specifications for BLVDS. They depend on the system topology.

Symbol/Description	Conditions	Trans	ceiver Spee	d Grade 2	Transc	eiver Spee	Unit	
Symbol/Description	Conditions	Min	Тур	Мах	Min	Тур	Max	
	DC gain setting = 0	—	0	_	_	0	—	dB
	DC gain setting = 1		2	_		2	_	dB
Programmable DC gain	DC gain setting = 2		4			4		dB
	DC gain setting = 3		6			6	_	dB
	DC gain setting = 4	_	8			8		dB

Related Information

Arria V Device Overview

For more information about device ordering codes.

Transmitter

Table 2-25: Transmitter Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Trans	ceiver Spee	d Grade 2	Transc	Transceiver Speed Grade 3			
Symbol/Description	Conditions	Min	Тур	Мах	Min	Тур	Мах	Offic	
Supported I/O Standards	1.4-V and 1.5-V PCML								
Data rate (Standard PCS)	—	600	_	9900	600		8800	Mbps	
Data rate (10G PCS)	_	600	_	12500	600	_	10312.5	Mbps	



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Symbol	Parameter	Min	Тур	Max	Unit
t (171) (172)	Input clock cycle-to-cycle jitter (f_{REF} $\geq 100~MHz)$	—	—	0.15	UI (p-p)
'INCCJ',	Input clock cycle-to-cycle jitter ($f_{REF} < 100 \text{ MHz}$)	-750		+750	ps (p-p)
tourny p.c. ⁽¹⁷³⁾	Period Jitter for dedicated clock output in integer PLL ($f_{OUT} \ge 100 \text{ MHz}$)			175	ps (p-p)
COUTPJ_DC	Period Jitter for dedicated clock output in integer PLL (f _{OUT} < 100 Mhz)	_		17.5	mUI (p-p)
t (173)	Period Jitter for dedicated clock output in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)	_		250 ⁽¹⁷⁶⁾ , 175 ⁽¹⁷⁴⁾	ps (p-p)
FOUTPJ_DC	Period Jitter for dedicated clock output in fractional PLL (f _{OUT} < 100 MHz)	_		$25^{(176)},$ 17.5 ⁽¹⁷⁴⁾	mUI (p-p)
t	Cycle-to-cycle Jitter for a dedicated clock output in integer PLL ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	175	ps (p-p)
COUTCCJ_DC	Cycle-to-cycle Jitter for a dedicated clock output in integer PLL (f _{OUT} < 100 MHz)	_		17.5	mUI (p-p)
t (173)	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)	—		250 ⁽¹⁷⁶⁾ , 175 ⁽¹⁷⁴⁾	ps (p-p)
FOUTCCJ_DC	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} < 100 \text{ MHz}$)			$25^{(176)}, \\ 17.5^{(174)}$	mUI (p-p)

⁽¹⁷¹⁾ A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps. ⁽¹⁷²⁾ The f_{REF} is fIN/N specification applies when N = 1.

⁽¹⁷⁴⁾ This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.20–0.80 must be \geq 1200 MHz.



⁽¹⁷³⁾ Peak-to-peak jitter with a probability level of 10⁻¹² (14 sigma, 99.999999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in the "Worst-Case DCD on Arria V GZ I/O Pins" table.

DPA Mode High-Speed I/O Specifications

Table 2-42: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions Min		C3, I3L		C4, I4			Unit
		Min	Тур	Мах	Min	Тур	Мах	Offic
DPA run length	—	_	_	10000	_		10000	UI

Figure 2-3: DPA Lock Time Specification with DPA PLL Calibration Enabled



Table 2-43: DPA Lock Time Specifications for Arria V GZ Devices

The DPA lock time is for one channel.

One data transition is defined as a 0-to-1 or 1-to-0 transition.

The DPA lock time stated in this table applies to both commercial and industrial grade.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽²⁰¹⁾	Maximum
SPI-4	0000000001111111111	2	128	640 data transitions



⁽²⁰¹⁾ This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.



Non DPA Mode High-Speed I/O Specifications

Table 2-46: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions –	C3, I3L			C4, I4			llait
		Min	Тур	Max	Min	Тур	Max	Onit
Sampling Window	—	_		300	_		300	ps



Table 2-57: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t _{CFG}	nCONFIG low pulse width	2	_	μs
t _{STATUS}	nSTATUS low pulse width	268	1,506 (210)	μs
t _{CF2ST1}	nCONFIG high to nSTATUS high	-	1,506 (211)	μs
t _{CF2CK} ⁽²¹²⁾	nCONFIG high to first rising edge on DCLK	1,506	_	μs
t _{ST2CK} ⁽²¹²⁾	nSTATUS high to first rising edge of DCLK	2	_	μs
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5	_	ns
t _{DH}	DATA[] hold time after rising edge on DCLK	N-1/f _{DCLK} ⁽²¹³⁾	_	S
t _{CH}	DCLK high time	$0.45 imes 1/f_{MAX}$	_	S
t _{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$		S
t _{CLK}	DCLK period	1/f _{MAX}	_	S
£	DCLK frequency (FPP ×8/×16)	-	125	MHz
IMAX	DCLK frequency (FPP ×32)	—	100	MHz
t _R	Input rise time	-	40	ns
t _F	Input fall time	—	40	ns
t _{CD2UM}	CONF_DONE high to user mode ⁽²¹⁴⁾	175	437	μs

⁽²¹⁰⁾ You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

⁽²¹¹⁾ You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

 $^{(212)}$ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

 $^{(213)}$ N is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.

⁽²¹⁴⁾ The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

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Related Information

- Configuration, Design Security, and Remote System Upgrades in Arria V Devices For more information about the reconfiguration input for the ALTREMOTE_UPDATE IP core, refer to the "User Watchdog Timer" section.
- Configuration, Design Security, and Remote System Upgrades in Arria V Devices For more information about the reset_timer input for the ALTREMOTE_UPDATE IP core, refer to the "Remote System Upgrade State Machine" section.

User Watchdog Internal Oscillator Frequency Specification

Table 2-65: User Watchdog Internal Oscillator Frequency Specifications

Minimum	Minimum Typical		Unit	
5.3	7.9	12.5	MHz	

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete placeand-route.

Related Information

Arria V Devices Documentation page

For the Excel-based I/O Timing spreadsheet

Arria V GZ Device Datasheet

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⁽²²⁶⁾ This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification. For more information, refer to the "Remote System Upgrade State Machine" section in the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.

⁽²²⁷⁾ This is equivalent to strobing the reset_timer input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification. For more information, refer to the "User Watchdog Timer" section in the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.

Programmable IOE Delay

Fast Model Slow Model Available Parameter (228) Min Offset (229) Unit Settings Industrial Commercial C3 C4 I3L 14 D1 64 0 0.464 0.493 0.924 1.011 0.921 1.006 ns 0 D2 32 0.230 0.244 0.459 0.503 0.456 0.500 ns D3 8 0 1.699 2.992 3.192 1.587 3.047 3.257 ns 0 D4 64 0.464 0.492 0.924 1.011 0.920 1.006 ns D5 64 0 0.464 0.493 0.924 1.011 0.921 1.006 ns 0.499 D6 32 0 0.244 0.503 0.229 0.458 0.456 ns

Table 2-66: IOE Programmable Delay for Arria V GZ Devices

Programmable Output Buffer Delay

Table 2-67: Programmable Output Buffer Delay for Arria V GZ Devices

You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

Symbol	Parameter	Typical	Unit
		0 (default)	ps
D _{OUTBUF}	Dising and/or falling adge delay	50	ps
	Rising and/or failing edge delay	100	ps
		150	ps

⁽²²⁸⁾ You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D4**, **D5**, and **D6** in the **Assignment Name** column of **Assignment Editor**.





⁽²²⁹⁾ Minimum offset does not include the intrinsic delay.

Term				Definition			
R _L	Receiver differential input discrete resistor (external to the Arria V GZ device).						
SW (sampling window)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:						
		◀		Bit Time			
		0.5 x TCCS RSKM Sampling Window RSKM 0.5 x TCCS (SW)					
Single-ended voltage referenced I/O standard	The JEDEC standard for SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing: Single-Ended Voltage Referenced I/O Standard						
	-	V _{0H}		V REF	Viн(DC Vil(DC)	V <u>ccio</u> VIH(AC) VIL(AC) VIL(AC)	

