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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	23780
Number of Logic Elements/Cells	504000
Total RAM Bits	27695104
Number of I/O	544
Number of Gates	-
Voltage - Supply	1.12V ~ 1.18V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxfb7h4f35i3n

Symbol	Description	Condition	Minimum ⁽¹⁾	Typical	Maximum ⁽¹⁾	Unit
V _{CCIO}	I/O buffers power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	1.283	1.35	1.418	V
		1.25 V	1.19	1.25	1.31	V
		1.2 V	1.14	1.2	1.26	V
V _{CCD_FPLL}	PLL digital voltage regulator power supply	—	1.425	1.5	1.575	V
V _{CCA_FPLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V _I	DC input voltage	—	−0.5	—	3.6	V
V _O	Output voltage	—	0	—	V _{CCIO}	V
T _J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	−40	—	100	°C
t _{RAMP} ⁽⁴⁾	Power supply ramp time	Standard POR	200 μs	—	100 ms	—
		Fast POR	200 μs	—	4 ms	—

⁽¹⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁴⁾ This is also applicable to HPS power supply. For HPS power supply, refer to t_{RAMP} specifications for standard POR when HPS_PORSEL = 0 and t_{RAMP} specifications for fast POR when HPS_PORSEL = 1.

Transceiver Power Supply Operating Conditions

Table 1-4: Transceiver Power Supply Operating Conditions for Arria V Devices

Symbol	Description	Minimum ⁽⁵⁾	Typical	Maximum ⁽⁵⁾	Unit
V _{CCA_GXBL}	Transceiver high voltage power (left side)	2.375	2.500	2.625	V
V _{CCA_GXBR}	Transceiver high voltage power (right side)				
V _{CCR_GXBL}	GX and SX speed grades—receiver power (left side)	1.08/1.12	1.1/1.15 ⁽⁶⁾	1.14/1.18	V
V _{CCR_GXBR}	GX and SX speed grades—receiver power (right side)				
V _{CCR_GXBL}	GT and ST speed grades—receiver power (left side)	1.17	1.20	1.23	V
V _{CCR_GXBR}	GT and ST speed grades—receiver power (right side)				
V _{CCT_GXBL}	GX and SX speed grades—transmitter power (left side)	1.08/1.12	1.1/1.15 ⁽⁶⁾	1.14/1.18	V
V _{CCT_GXBR}	GX and SX speed grades—transmitter power (right side)				
V _{CCT_GXBL}	GT and ST speed grades—transmitter power (left side)	1.17	1.20	1.23	V
V _{CCT_GXBR}	GT and ST speed grades—transmitter power (right side)				
V _{CCH_GXBL}	Transmitter output buffer power (left side)	1.425	1.500	1.575	V
V _{CCH_GXBR}	Transmitter output buffer power (right side)				

⁽⁵⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁶⁾ For data rate ≤ 3.2 Gbps, connect V_{CCR_GXBL/R}, V_{CCT_GXBL/R}, or V_{CCL_GXBL/R} to either 1.1-V or 1.15-V power supply. For data rate > 3.2 Gbps, connect V_{CCR_GXBL/R}, V_{CCT_GXBL/R}, or V_{CCL_GXBL/R} to a 1.15-V power supply. For details, refer to the Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines.

Symbol	Description	Minimum ⁽⁵⁾	Typical	Maximum ⁽⁵⁾	Unit
V _{CCL_GXBL}	GX and SX speed grades—clock network power (left side)	1.08/1.12	1.1/1.15 ⁽⁶⁾	1.14/1.18	V
V _{CCL_GXBR}	GX and SX speed grades—clock network power (right side)				
V _{CCL_GXBL}	GT and ST speed grades—clock network power (left side)	1.17	1.20	1.23	V
V _{CCL_GXBR}	GT and ST speed grades—clock network power (right side)				

Related Information**Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines**

Provides more information about the power supply connection for different data rates.

HPS Power Supply Operating Conditions**Table 1-5: HPS Power Supply Operating Conditions for Arria V SX and ST Devices**

This table lists the steady-state voltage and current values expected from Arria V system-on-a-chip (SoC) devices with ARM®-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to Recommended Operating Conditions for Arria V Devices table for the steady-state voltage values expected from the FPGA portion of the Arria V SoC devices.

Symbol	Description	Condition	Minimum ⁽⁷⁾	Typical	Maximum ⁽⁷⁾	Unit
V _{CC_HPS}	HPS core voltage and periphery circuitry power supply	–C4, –I5, –C5, –C6	1.07	1.1	1.13	V
		–I3	1.12	1.15	1.18	V

⁽⁵⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁷⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Symbol	V _{OD} Setting ⁽⁵⁸⁾	V _{OD} Value (mV)	V _{OD} Setting ⁽⁵⁸⁾	V _{OD} Value (mV)
	25	500	53	1060
	26	520	54	1080
	27	540	55	1100
	28	560	56	1120
	29	580	57	1140
	30	600	58	1160
	31	620	59	1180
	32	640	60	1200
	33	660		

Transmitter Pre-Emphasis Levels

The following table lists the simulation data on the transmitter pre-emphasis levels in dB for the first post tap under the following conditions:

- Low-frequency data pattern—five 1s and five 0s
- Data rate—2.5 Gbps

The levels listed are a representation of possible pre-emphasis levels under the specified conditions only and the pre-emphasis levels may change with data pattern and data rate.

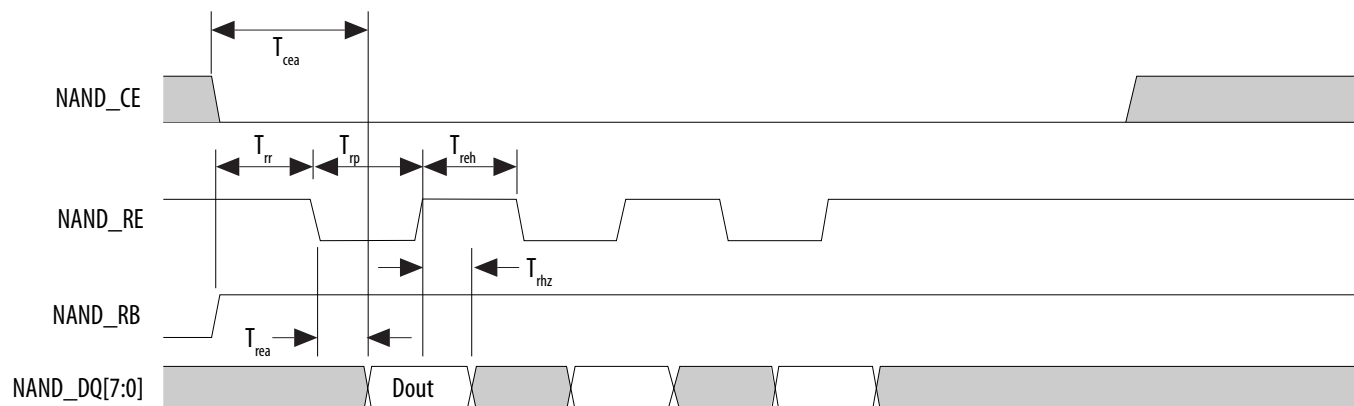
Arria V devices only support 1st post tap pre-emphasis with the following conditions:

- The 1st post tap pre-emphasis settings must satisfy $|B| + |C| \leq 60$ where $|B| = V_{OD}$ setting with termination value, $R_{TERM} = 100 \Omega$ and $|C| = 1st$ post tap pre-emphasis setting.
- $|B| - |C| > 5$ for data rates < 5 Gbps and $|B| - |C| > 8.25$ for data rates > 5 Gbps.
- $(V_{MAX}/V_{MIN} - 1)\% < 600\%$, where $V_{MAX} = |B| + |C|$ and $V_{MIN} = |B| - |C|$.

Exception for PCIe Gen2 design: V_{OD} setting = 43 and pre-emphasis setting = 19 are allowed for PCIe Gen2 design with transmit de-emphasis – 6dB setting (pipe_txdeemp = 1'b0) using Altera PCIe Hard IP and PIPE IP cores.

⁽⁵⁸⁾ Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

Figure 1-20: NAND Data Read Timing Diagram



ARM Trace Timing Characteristics

Table 1-61: ARM Trace Timing Requirements for Arria V Devices

Most debugging tools have a mechanism to adjust the capture point of trace data.

Description	Min	Max	Unit
CLK clock period	12.5	—	ns
CLK maximum duty cycle	45	55	%
CLK to D0 –D7 output data delay	–1	1	ns

UART Interface

The maximum UART baud rate is 6.25 megasymbols per second.

GPIO Interface

The minimum detectable general-purpose I/O (GPIO) pulse width is 2 μ s. The pulse width is based on a debounce clock frequency of 1 MHz.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times \text{CLKUSR period})$	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information**FPP Configuration Timing**

Provides the FPP configuration timing waveforms.

AS Configuration Timing

Table 1-68: AS Timing Parameters for AS $\times 1$ and $\times 4$ Configurations in Arria V Devices

The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

The t_{CF2CD} , t_{CF2ST0} , t_{CFG} , t_{STATUS} , and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in PS Timing Parameters for Arria V Devices table. You can obtain the t_{CF2ST1} value if you do not delay configuration by externally holding $nSTATUS$ low.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	2	ns
t_{SU}	Data setup time before the falling edge on DCLK	1.5	—	ns
t_{DH}	Data hold time after the falling edge on DCLK	0	—	ns
t_{CD2UM}	CONF_DONE high to user mode	175	437	μs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times \text{CLKUSR period})$	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

The Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

[Arria V I/O Timing Spreadsheet](#)

Provides the Arria V Excel-based I/O timing spreadsheet.

Programmable IOE Delay

Table 1-76: I/O element (IOE) Programmable Delay for Arria V Devices

Parameter ⁽¹¹²⁾	Available Settings	Minimum Offset ⁽¹¹³⁾	Fast Model		Slow Model					Unit
			Industrial	Commercial	–C4	–C5	–C6	–I3	–I5	
D1	32	0	0.508	0.517	0.870	1.063	1.063	0.872	1.057	ns
D3	8	0	1.763	1.795	2.999	3.496	3.571	3.031	3.643	ns
D4	32	0	0.508	0.518	0.869	1.063	1.063	1.063	1.057	ns
D5	32	0	0.508	0.517	0.870	1.063	1.063	0.872	1.057	ns

Programmable Output Buffer Delay

Table 1-77: Programmable Output Buffer Delay for Arria V Devices

This table lists the delay chain settings that control the rising and falling edge delays of the output buffer.

You can set the programmable output buffer delay in the Quartus Prime software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

⁽¹¹²⁾ You can set this value in the Quartus Prime software by selecting **D1**, **D3**, **D4**, and **D5** in the **Assignment Name** column of **Assignment Editor**.

⁽¹¹³⁾ Minimum offset does not include the intrinsic delay.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle.

For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

Table 2-4: Maximum Allowed Overshoot During Transitions for Arria V GZ Devices

Symbol	Description	Condition (V)	Overshoot Duration as % @ $T_J = 100^\circ\text{C}$	Unit
Vi (AC)	AC input voltage	3.8	100	%
		3.85	64	%
		3.9	36	%
		3.95	21	%
		4	12	%
		4.05	7	%
		4.1	4	%
		4.15	2	%
		4.2	1	%

Recommended Operating Conditions

Table 2-5: Recommended Operating Conditions for Arria V GZ Devices

Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum ⁽¹¹⁴⁾	Typical	Maximum ⁽¹¹⁴⁾	Unit
V _{CC}	Core voltage and periphery circuitry power supply ⁽¹¹⁵⁾	—	0.82	0.85	0.88	V

⁽¹¹⁴⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹¹⁵⁾ The V_{CC} core supply must be set to 0.9 V if the Partial Reconfiguration (PR) feature is used.

Transceiver Power Supply Requirements

Table 2-7: Transceiver Power Supply Voltage Requirements for Arria V GZ Devices

Conditions	VCCR_GXB and VCCT_GXB ⁽¹²²⁾	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true: <ul style="list-style-type: none"> Data rate > 10.3 Gbps. DFE is used. 	1.05	3.0	1.5	V
If ANY of the following conditions are true ⁽¹²³⁾ : <ul style="list-style-type: none"> ATX PLL is used. Data rate > 6.5Gbps. DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used. 	1.0			
If ALL of the following conditions are true: <ul style="list-style-type: none"> ATX PLL is not used. Data rate ≤ 6.5Gbps. DFE, AEQ, and EyeQ are not used. 	0.85	2.5		

DC Characteristics

Supply Current

Standby current is the current drawn from the respective power rails used for power budgeting.

Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

⁽¹²²⁾ If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to 0.85 V, they can be shared with the VCC core supply.

⁽¹²³⁾ Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

Symbol	Description	V_{CCIO} (V)	Typical	Unit
dR/dV	OCT variation with voltage without re-calibration	3.0	0.0297	%/mV
		2.5	0.0344	
		1.8	0.0499	
		1.5	0.0744	
		1.2	0.1241	
dR/dT	OCT variation with temperature without re-calibration	3.0	0.189	%/°C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.2	0.317	

Pin Capacitance

Table 2-13: Pin Capacitance for Arria V GZ Devices

Symbol	Description	Maximum	Unit
C_{IOTB}	Input capacitance on the top and bottom I/O pins	6	pF
C_{IOLR}	Input capacitance on the left and right I/O pins	6	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output and feedback pins	6	pF

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration ⁽¹⁴⁶⁾	$V_{CCR_GXB} = 1.0\text{ V}$ ($V_{ICM} = 0.75\text{ V}$)	—	—	1.8	—	—	1.8	V
	$V_{CCR_GXB} = 0.85\text{ V}$ ($V_{ICM} = 0.6\text{ V}$)	—	—	2.4	—	—	2.4	V
Minimum differential eye opening at receiver serial input pins ⁽¹⁴⁷⁾⁽¹⁴⁸⁾	—	85	—	—	85	—	—	mV
Differential on-chip termination resistors	85- Ω setting	—	$85 \pm 30\%$	—	—	$85 \pm 30\%$	—	Ω
	100- Ω setting	—	$100 \pm 30\%$	—	—	$100 \pm 30\%$	—	Ω
	120- Ω setting	—	$120 \pm 30\%$	—	—	$120 \pm 30\%$	—	Ω
	150- Ω setting	—	$150 \pm 30\%$	—	—	$150 \pm 30\%$	—	Ω

⁽¹⁴⁶⁾ The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to $4 \times (\text{absolute } V_{MAX} \text{ for receiver pin} - V_{ICM})$.

⁽¹⁴⁷⁾ The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

⁽¹⁴⁸⁾ Minimum eye opening of 85 mV is only for the unstressed input eye condition.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported data range	—	600	—	3250/ 3125 ⁽¹⁵⁸⁾	600	—	3250/ 3125 ⁽¹⁵⁸⁾	Mbps
$t_{\text{pll_powerdown}}$ ⁽¹⁵⁹⁾	—	1	—	—	1	—	—	μs
$t_{\text{pll_lock}}$ ⁽¹⁶⁰⁾	—	—	—	10	—	—	10	μs

Related Information[Arria V Device Overview](#)

For more information about device ordering codes.

Clock Network Data Rate**Table 2-29: Clock Network Maximum Data Rate Transmitter Specifications**

Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.

Clock Network	ATX PLL			CMU PLL ⁽¹⁶¹⁾			fPLL		
	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span
x1 ⁽¹⁶²⁾	12.5	—	6	12.5	—	6	3.125	—	3
x6 ⁽¹⁶²⁾	—	12.5	6	—	12.5	6	—	3.125	6
x6 PLL Feedback ⁽¹⁶³⁾	—	12.5	Side-wide	—	12.5	Side-wide	—	—	—

⁽¹⁵⁸⁾ When you use fPLL as a TXPLL of the transceiver.

⁽¹⁵⁹⁾ $t_{\text{pll_powerdown}}$ is the PLL powerdown minimum pulse width.

⁽¹⁶⁰⁾ $t_{\text{pll_lock}}$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

⁽¹⁶¹⁾ ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

⁽¹⁶²⁾ Channel span is within a transceiver bank.

⁽¹⁶³⁾ Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
True Differential I/O Standards - f_{HSDRDPA} (data rate)	SERDES factor J = 3 to 10 (192), (193), (194), (195), (196), (197)	150	—	1250	150	—	1050	Mbps
	SERDES factor J ≥ 4 LVDS RX with DPA (193), (195), (196), (197)	150	—	1600	150	—	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(198)	—	(199)	(198)	—	(199)	Mbps
	SERDES factor J = 1, uses SDR Register	(198)	—	(199)	(198)	—	(199)	Mbps
f_{HSDR} (data rate)	SERDES factor J = 3 to 10	(198)	—	(200)	(198)	—	(200)	Mbps
	SERDES factor J = 2, uses DDR Registers	(198)	—	(199)	(198)	—	(199)	Mbps
	SERDES factor J = 1, uses SDR Register	(198)	—	(199)	(198)	—	(199)	Mbps

(192) The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(193) Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.

(194) Arria V GZ LVDS serialization and de-serialization factor needs to be x4 and above.

(195) Requires package skew compensation with PCB trace length.

(196) Do not mix single-ended I/O buffer within LVDS I/O bank.

(197) Chip-to-chip communication only with a maximum load of 5 pF.

(198) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(199) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity simulation is clean.

(200) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽²⁰¹⁾	Maximum
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
	01010101	8	32	640 data transitions

Soft CDR Mode High-Speed I/O Specifications

Table 2-44: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Soft-CDR ppm tolerance	—	—	—	300	—	—	300	± ppm

⁽²⁰¹⁾ This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Duty Cycle Distortion (DCD) Specifications

Table 2-52: Worst-Case DCD on Arria V GZ I/O Pins

The DCD numbers do not cover the core clock network.

Symbol	C3, I3L		C4, I4		Unit
	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	%

Configuration Specification

POR Specifications

Table 2-53: Fast and Standard POR Delay Specification for Arria V GZ Devices

Select the POR delay based on the MSEL setting as described in the “Configuration Schemes for Arria V Devices” table in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

POR Delay	Minimum (ms)	Maximum (ms)
Fast	4	12 ⁽²⁰²⁾
Standard	100	300

Related Information

[Configuration, Design Security, and Remote System Upgrades in Arria V Devices](#)

⁽²⁰²⁾ The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

Table 2-57: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	μ s
t_{STATUS}	nSTATUS low pulse width	268	1,506 ⁽²¹⁰⁾	μ s
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽²¹¹⁾	μ s
t_{CF2CK} ⁽²¹²⁾	nCONFIG high to first rising edge on DCLK	1,506	—	μ s
t_{ST2CK} ⁽²¹²⁾	nSTATUS high to first rising edge of DCLK	2	—	μ s
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N - 1/f_{DCLK}$ ⁽²¹³⁾	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP $\times 8/\times 16$)	—	125	MHz
	DCLK frequency (FPP $\times 32$)	—	100	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode ⁽²¹⁴⁾	175	437	μ s

⁽²¹⁰⁾ You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

⁽²¹¹⁾ You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

⁽²¹²⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

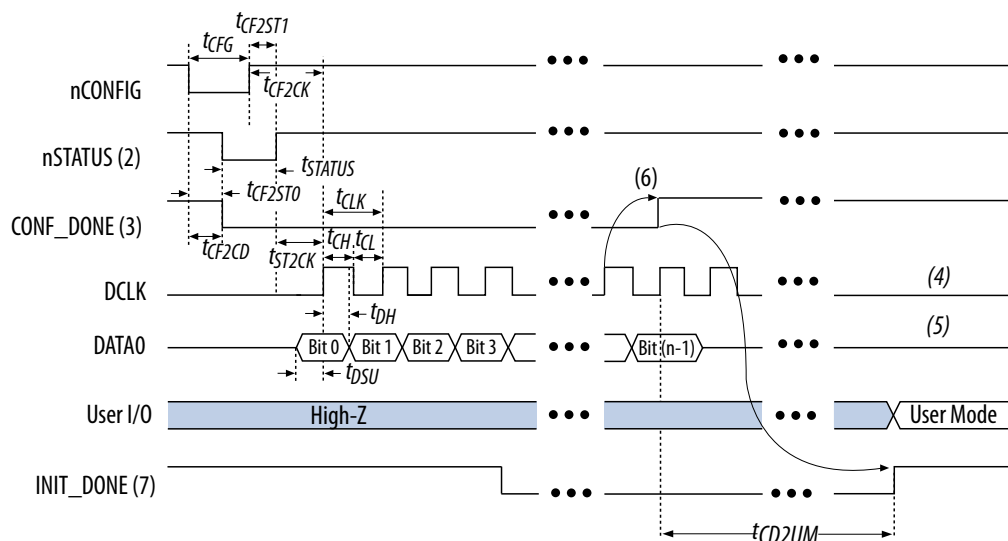
⁽²¹³⁾ N is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.

⁽²¹⁴⁾ The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

Passive Serial Configuration Timing

Figure 2-10: PS Configuration Timing Waveform

Timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.



Notes:

1. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
2. After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.
3. After power-up, before and during configuration, CONF_DONE is low.
4. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
5. DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the Device and Pins Option.
6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
7. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 2-62: Uncompressed .rbf Sizes for Arria V GZ Devices

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ⁽²²³⁾
Arria V GZ	E1	137,598,880	562,208
	E3	137,598,880	562,208
	E5	213,798,880	561,760
	E7	213,798,880	561,760

Table 2-63: Minimum Configuration Time Estimation for Arria V GZ Devices

Variant	Member Code	Active Serial ⁽²²⁴⁾			Fast Passive Parallel ⁽²²⁵⁾		
		Width	DCLK (MHz)	Min Config Time (ms)	Width	DCLK (MHz)	Min Config Time (ms)
Arria V GZ	E1	4	100	344	32	100	43
	E3	4	100	344	32	100	43
	E5	4	100	534	32	100	67
	E7	4	100	534	32	100	67

Remote System Upgrades Circuitry Timing Specification

Table 2-64: Remote System Upgrade Circuitry Timing Specifications

Parameter	Minimum	Maximum	Unit
$t_{RU_nCONFIG}$ ⁽²²⁶⁾	250	—	ns
$t_{RU_nRSTIMER}$ ⁽²²⁷⁾	250	—	ns

⁽²²³⁾ The IOCSR .rbf size is specifically for the Configuration via Protocol (CvP) feature.

⁽²²⁴⁾ DCLK frequency of 100 MHz using external CLKUSR.

⁽²²⁵⁾ Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Programmable IOE Delay

Table 2-66: IOE Programmable Delay for Arria V GZ Devices

Parameter ⁽²²⁸⁾	Available Settings	Min Offset ⁽²²⁹⁾	Fast Model		Slow Model				Unit
			Industrial	Commercial	C3	C4	I3L	I4	
D1	64	0	0.464	0.493	0.924	1.011	0.921	1.006	ns
D2	32	0	0.230	0.244	0.459	0.503	0.456	0.500	ns
D3	8	0	1.587	1.699	2.992	3.192	3.047	3.257	ns
D4	64	0	0.464	0.492	0.924	1.011	0.920	1.006	ns
D5	64	0	0.464	0.493	0.924	1.011	0.921	1.006	ns
D6	32	0	0.229	0.244	0.458	0.503	0.456	0.499	ns

Programmable Output Buffer Delay

Table 2-67: Programmable Output Buffer Delay for Arria V GZ Devices

You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

Symbol	Parameter	Typical	Unit
D _{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

⁽²²⁸⁾ You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D4**, **D5**, and **D6** in the **Assignment Name** column of **Assignment Editor**.

⁽²²⁹⁾ Minimum offset does not include the intrinsic delay.

Term	Definition
V_{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
V_{SWING}	Differential input voltage
V_X	Input differential cross point voltage
V_{OX}	Output differential cross point voltage
W	High-speed I/O block—clock boost factor

Document Revision History

Date	Version	Changes
February 2017	2017.02.10	<ul style="list-style-type: none"> Changed the minimum value for t_{CD2UMC} in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1" table. Changed the minimum value for t_{CD2UMC} in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1" table. Changed the minimum value for t_{CD2UMC} in the "AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices" table. Changed the minimum value for t_{CD2UMC} in the "PS Timing Parameters for Arria V GZ Devices" table. Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices" table.