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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 23780 |
| Number of Logic Elements/Cells | 504000 |
| Total RAM Bits | 27695104 |
| Number of I/O | 704 |
| Number of Gates | - |
| Voltage - Supply | 1.07V ~ 1.13V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1517-BBGA |
| Supplier Device Package | 1517-FBGA (40x40) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5agxfb7k6f40c6n |

| Symbol | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $V_{CCPLL\_HPS}$ | HPS PLL analog power supply | –0.50 | 3.25 | V |
| $V_{CC\_AUX\_SHARED}$ | HPS auxiliary power supply | –0.50 | 3.25 | V |
| $I_{OUT}$ | DC output current per pin | –25 | 40 | mA |
| $T_J$ | Operating junction temperature | –55 | 125 | °C |
| $T_{STG}$ | Storage temperature (no bias) | –65 | 150 | °C |

## Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 4.00 V can only be at 4.00 V for ~15% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 1.5 years.

### Table 1-2: Maximum Allowed Overshoot During Transitions for Arria V Devices

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

| Symbol | Description | Condition | Minimum[7] | Typical | Maximum[7] | Unit |
|---|---|---|---|---|---|---|
| $V_{CCPD\_HPS}$ [8] | HPS I/O pre-driver power supply | 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | | 3.0 V | 2.85 | 3.0 | 3.15 | V |
| | | 2.5 V | 2.375 | 2.5 | 2.625 | V |
| $V_{CCIO\_HPS}$ | HPS I/O buffers power supply | 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | | 3.0 V | 2.85 | 3.0 | 3.15 | V |
| | | 2.5 V | 2.375 | 2.5 | 2.625 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | V |
| | | 1.5 V | 1.425 | 1.5 | 1.575 | V |
| | | 1.35 V [9] | 1.283 | 1.35 | 1.418 | V |
| | | 1.2 V | 1.14 | 1.2 | 1.26 | V |
| $V_{CCRSTCLK\_HPS}$ | HPS reset and clock input pins power supply | 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | | 3.0 V | 2.85 | 3.0 | 3.15 | V |
| | | 2.5 V | 2.375 | 2.5 | 2.625 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | V |
| $V_{CCPLL\_HPS}$ | HPS PLL analog voltage regulator power supply | — | 2.375 | 2.5 | 2.625 | V |

(7) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(8) $V_{CCPD\_HPS}$ must be 2.5 V when $V_{CCIO\_HPS}$ is 2.5, 1.8, 1.5, or 1.2 V. $V_{CCPD\_HPS}$ must be 3.0 V when $V_{CCIO\_HPS}$ is 3.0 V. $V_{CCPD\_HPS}$ must be 3.3 V when $V_{CCIO\_HPS}$ is 3.3 V.

(9) $V_{CCIO\_HPS}$ 1.35 V is supported for HPS row I/O bank only.

## I/O Pin Leakage Current

### Table 1-6: I/O Pin Leakage Current for Arria V Devices

| Symbol | Description | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input pin | $V_I$ = 0 V to $V_{CCIOMAX}$ | –30 | — | 30 | µA |
| $I_{OZ}$ | Tri-stated I/O pin | $V_O$ = 0 V to $V_{CCIOMAX}$ | –30 | — | 30 | µA |

## Bus Hold Specifications

### Table 1-7: Bus Hold Parameters for Arria V Devices

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

| Parameter | Symbol | Condition | $V_{CCIO}$ (V) | | | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | 3.3 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus-hold, low, sustaining current | $I_{SUSL}$ | $V_{IN} > V_{IL}$ (max) | 8 | — | 12 | — | 30 | — | 50 | — | 70 | — | 70 | — | µA |
| Bus-hold, high, sustaining current | $I_{SUSH}$ | $V_{IN} < V_{IH}$ (min) | –8 | — | –12 | — | –30 | — | –50 | — | –70 | — | –70 | — | µA |
| Bus-hold, low, overdrive current | $I_{ODL}$ | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | 125 | — | 175 | — | 200 | — | 300 | — | 500 | — | 500 | µA |
| Bus-hold, high, overdrive current | $I_{ODH}$ | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | –125 | — | –175 | — | –200 | — | –300 | — | –500 | — | –500 | µA |

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{SWING(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{SWING(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Max |
| SSTL-125 | 1.19 | 1.25 | 1.31 | 0.18 | (15) | $V_{CCIO}/2 - 0.15$ | $V_{CCIO}/2$ | $V_{CCIO}/2 + 0.15$ | $2(V_{IH(AC)} - V_{REF})$ | $2(V_{IL(AC)} - V_{REF})$ |

### Differential HSTL and HSUL I/O Standards

**Table 1-18: Differential HSTL and HSUL I/O Standards for Arria V Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.78 | — | 1.12 | 0.78 | — | 1.12 | 0.4 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.68 | — | 0.9 | 0.68 | — | 0.9 | 0.4 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | $V_{CCIO} + 0.3$ | — | $0.5 \times V_{CCIO}$ | — | $0.4 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.6 \times V_{CCIO}$ | 0.3 | $V_{CCIO} + 0.48$ |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.26 | 0.26 | $0.5 \times V_{CCIO} - 0.12$ | $0.5 \times V_{CCIO}$ | $0.5 \times V_{CCIO} + 0.12$ | $0.4 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.6 \times V_{CCIO}$ | 0.44 | 0.44 |

### Differential I/O Standard Specifications

**Table 1-19: Differential I/O Standard Specifications for Arria V Devices**

Differential inputs are powered by $V_{CCPD}$ which requires 2.5 V.

## Transceiver Specifications for Arria V GT and ST Devices

### Table 1-26: Reference Clock Specifications for Arria V GT and ST Devices

| Symbol/Description | Condition | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Supported I/O standards | 1.2 V PCML, 1.4 VPCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL(40), HCSL, and LVDS | | | | |
| Input frequency from REFCLK input pins | — | 27 | — | 710 | MHz |
| Rise time | Measure at ±60 mV of differential signal(41) | — | — | 400 | ps |
| Fall time | Measure at ±60 mV of differential signal(41) | — | — | 400 | ps |
| Duty cycle | — | 45 | — | 55 | % |
| Peak-to-peak differential input voltage | — | 200 | — | 300(42)/2000 | mV |
| Spread-spectrum modulating clock frequency | PCI Express (PCIe) | 30 | — | 33 | kHz |
| Spread-spectrum downspread | PCIe | — | 0 to –0.5% | — | — |
| On-chip termination resistors | — | — | 100 | — | Ω |
| $V_{ICM}$ (AC coupled) | — | — | 1.2 | — | V |
| $V_{ICM}$ (DC coupled) | HCSL I/O standard for the PCIe reference clock | 250 | — | 550 | mV |

(40) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.
(41) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
(42) The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

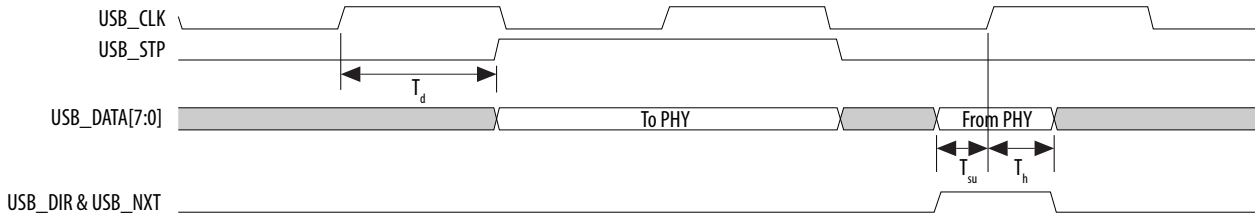
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{OUT\_EXT}$ | Output frequency for external clock output | –3 speed grade | — | — | 670[63] | MHz |
| | | –4 speed grade | — | — | 670[63] | MHz |
| | | –5 speed grade | — | — | 622[63] | MHz |
| | | –6 speed grade | — | — | 500[63] | MHz |
| $t_{OUTDUTY}$ | Duty cycle for external clock output (when set to 50%) | — | 45 | 50 | 55 | % |
| $t_{FCOMP}$ | External feedback clock compensation time | — | — | — | 10 | ns |
| $t_{DYCONFIGCLK}$ | Dynamic configuration clock for `mgmt_clk` and `scanclk` | — | — | — | 100 | MHz |
| $t_{LOCK}$ | Time required to lock from end-of-device configuration or deassertion of `areset` | — | — | — | 1 | ms |
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | — | 1 | ms |
| $f_{CLBW}$ | PLL closed-loop bandwidth | Low | — | 0.3 | — | MHz |
| | | Medium | — | 1.5 | — | MHz |
| | | High[64] | — | 4 | — | MHz |
| $t_{PLL\_PSERR}$ | Accuracy of PLL phase shift | — | — | — | ±50 | ps |
| $t_{ARESET}$ | Minimum pulse width on the `areset` signal | — | 10 | — | — | ns |
| $t_{INCCJ}$[65][66] | Input clock cycle-to-cycle jitter | $F_{REF} \geq 100$ MHz | — | — | 0.15 | UI (p-p) |
| | | $F_{REF} < 100$ MHz | — | — | ±750 | ps (p-p) |

(64) High bandwidth PLL settings are not supported in external feedback mode.
(65) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.
(66) $F_{REF}$ is $f_{IN}/N$, specification applies when $N = 1$.

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $T_h$ | SPI MISO hold time | 1 | — | ns |
| $T_{dutycycle}$ | SPI_CLK duty cycle | 45 | 55 | % |
| $T_{dssfrst}$ | Output delay SPI_SS valid before first clock edge | 8 | — | ns |
| $T_{dsslst}$ | Output delay SPI_SS valid after last clock edge | 8 | — | ns |
| $T_{dio}$ | Master-out slave-in (MOSI) output delay | –1 | 1 | ns |

(86) This value is based on `rx_sample_dly` = 1 and `spi_m_clk` = 120 MHz. `spi_m_clk` is the internal clock that is used by SPI Master to derive it's `SCLK_OUT`. These timings are based on `rx_sample_dly` of 1. This delay can be adjusted as needed to accommodate slower response times from the slave. Note that a delay of 0 is not allowed. The setup time can be used as a reference starting point. It is very crucial to do a calibration to get the correct `rx_sample_dly` value because each SPI slave device may have different output delay and each application board may have different path delay. For more information about `rx_sample_delay`, refer to the SPI Controller chapter in the Hard Processor System Technical Reference Manual.

**Figure 1-12: USB Timing Diagram**

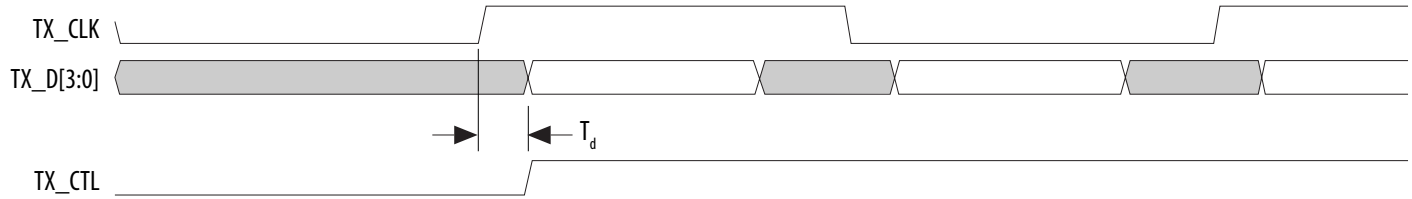



## Ethernet Media Access Controller (EMAC) Timing Characteristics

**Table 1-56: Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements for Arria V Devices**

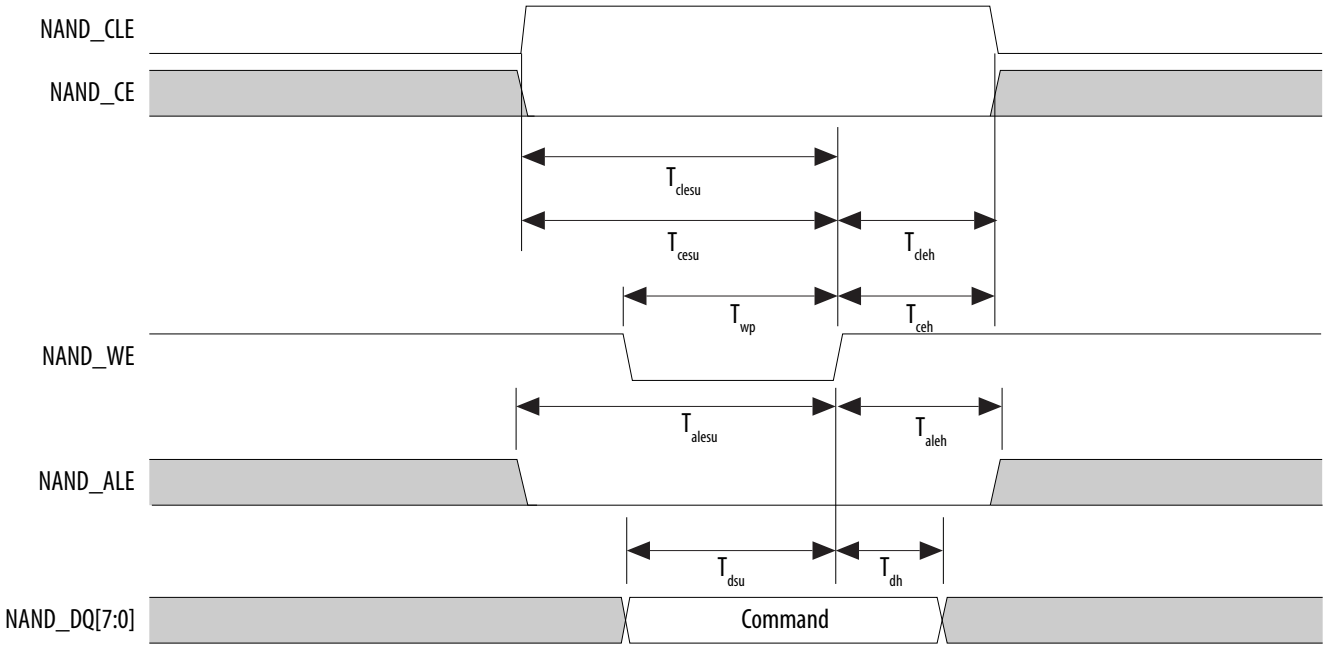
| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{clk}$ (1000Base-T) | TX_CLK clock period | — | 8 | — | ns |
| $T_{clk}$ (100Base-T) | TX_CLK clock period | — | 40 | — | ns |
| $T_{clk}$ (10Base-T) | TX_CLK clock period | — | 400 | — | ns |
| $T_{dutycycle}$ | TX_CLK duty cycle | 45 | — | 55 | % |
| $T_d$ | TX_CLK to TXD/TX_CTL output data delay | –0.85 | — | 0.15 | ns |

**Figure 1-13: RGMII TX Timing Diagram**



| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $T_{dh}$ (89) | Data to write enable hold time | 5 | — | ns |
| $T_{cea}$ | Chip enable to data access time | — | 25 | ns |
| $T_{rea}$ | Read enable to data access time | — | 16 | ns |
| $T_{rhz}$ | Read enable to data high impedance | — | 100 | ns |
| $T_{rr}$ | Ready to read enable low | 20 | — | ns |

**Figure 1-17: NAND Command Latch Timing Diagram**



# FPP Configuration Timing

## DCLK-to-DATA[] Ratio (r) for FPP Configuration

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is *r* times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP ×16 where the *r* is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

**Table 1-65: DCLK-to-DATA[] Ratio for Arria V Devices**

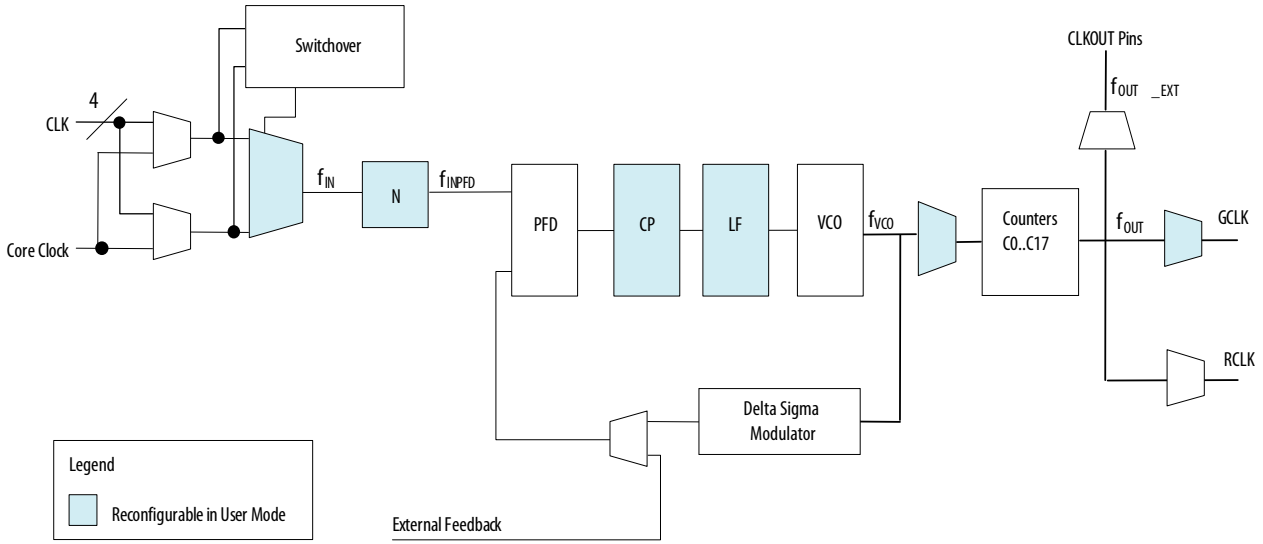
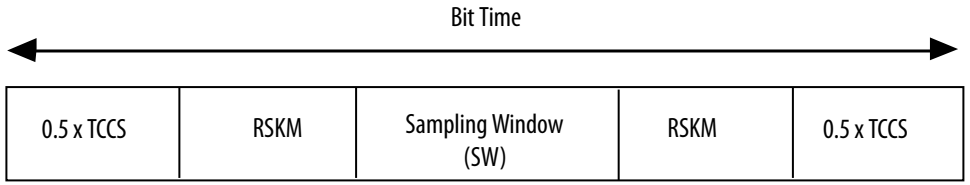
| Configuration Scheme | Encryption | Compression | DCLK-to-DATA[] Ratio (r) |
|---|---|---|---|
| FPP (8-bit wide) | Off | Off | 1 |
| | On | Off | 1 |
| | Off | On | 2 |
| | On | On | 2 |
| FPP (16-bit wide) | Off | Off | 1 |
| | On | Off | 2 |
| | Off | On | 4 |
| | On | On | 4 |

## FPP Configuration Timing when DCLK-to-DATA[] = 1

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8 and FPP ×16. For the respective DCLK-to-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Arria V Devices table.

**Table 1-66: FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Arria V Devices**

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 600 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 600 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |

| Term | Definition |
|---|---|
| PLL specifications | Diagram of PLL specifications<br>  <br><br>**Note:**<br>(1) Core Clock can only be fed by dedicated clock input pins or PLL outputs. |
| $R_L$ | Receiver differential input discrete resistor (external to the Arria V device). |
| Sampling window (SW) | Timing diagram—The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown:<br>  <br> |

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | $V_{CCIO}$ + 0.3 | — | 0.5 × $V_{CCIO}$ | — | 0.4 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.6 × $V_{CCIO}$ | 0.3 | $V_{CCIO}$ + 0.48 |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.26 | 0.26 | 0.5 × $V_{CCIO}$ – 0.12 | 0.5 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ + 0.12 | 0.4 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.6 × $V_{CCIO}$ | 0.44 | 0.44 |

**Table 2-21: Differential I/O Standard Specifications for Arria V GZ Devices**

| I/O Standard | $V_{CCIO}$ (V) (128) | | | $V_{ID}$ (mV) (129) | | | $V_{ICM(DC)}$ (V) | | | $V_{OD}$ (V) (130) | | | $V_{OCM}$ (V) (130) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Condition | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| PCML | Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to the "Transceiver Performance Specifications" section. | | | | | | | | | | | | | | |
| 2.5 V LVDS (131) | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.05 | $D_{MAX}$ ≤ 700 Mbps | 1.8 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| | | | | | | — | 1.05 | $D_{MAX}$ > 700 Mbps | 1.55 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| BLVDS (132) | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — | — |

(128) Differential inputs are powered by VCCPD which requires 2.5 V.
(129) The minimum VID value is applicable over the entire common mode range, VCM.
(130) RL range: 90 ≤ RL ≤ 110 Ω.
(131) For optimized LVDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.
(132) There are no fixed $V_{ICM}$, $V_{OD}$, and $V_{OCM}$ specifications for BLVDS. They depend on the system topology.

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Differential on-chip termination resistors | 85-Ω setting | — | 85 ± 20% | — | — | 85 ± 20% | — | Ω |
| | 100-Ω setting | — | 100 ± 20% | — | — | 100 ± 20% | — | Ω |
| | 120-Ω setting | — | 120 ± 20% | — | — | 120 ± 20% | — | Ω |
| | 150-Ω setting | — | 150 ± 20% | — | — | 150 ± 20% | — | Ω |
| $V_{OCM}$ (AC coupled) | 0.65-V setting | — | 650 | — | — | 650 | — | mV |
| $V_{OCM}$ (DC coupled) | — | — | 650 | — | — | 650 | — | mV |
| Intra-differential pair skew | Tx $V_{CM}$ = 0.5 V and slew rate of 15 ps | — | — | 15 | — | — | 15 | ps |
| Intra-transceiver block transmitter channel-to-channel skew | x6 PMA bonded mode | — | — | 120 | — | — | 120 | ps |
| Inter-transceiver block transmitter channel-to-channel skew | xN PMA bonded mode | — | — | 500 | — | — | 500 | ps |

**Related Information**

**Arria V Device Overview**

For more information about device ordering codes.

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supported data rate range | VCO post-divider L = 2 | 8000 | — | 12500 | 8000 | — | 10312.5 | Mbps |
| | L = 4 | 4000 | — | 6600 | 4000 | — | 6600 | Mbps |
| | L = 8 (155) | 2000 | — | 3300 | 2000 | — | 3300 | Mbps |
| $t_{pll\_powerdown}$ (156) | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll\_lock}$ (157) | — | — | — | 10 | — | — | 10 | µs |

**Related Information**

- **Arria V Device Overview**
  For more information about device ordering codes.
- **Transceiver Clocking in Arria V Devices**
  For more information about clocking ATX PLLs.
- **Dynamic Reconfiguration in Arria V Devices**
  For more information about reconfiguring ATX PLLs.

## Fractional PLL

### Table 2-28: Fractional PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

(155) This clock can be further divided by central or local clock dividers making it possible to use ATX PLL for data rates < 1 Gbps. For more information about ATX PLLs, refer to the Transceiver Clocking in Arria V Devices chapter and the Dynamic Reconfiguration in Arria V Devices chapter.
(156) $t_{pll\_powerdown}$ is the PLL powerdown minimum pulse width.
(157) $t_{pll\_lock}$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

| Description | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Diode ideality factor | 1.006 | 1.008 | 1.010 | — |

# Periphery Performance

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

**Note:** The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

## High-Speed I/O Specification

### High-Speed Clock Specifications

**Table 2-39: High-Speed Clock Specifications for Arria V GZ Devices**

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

Arria V GZ devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 230 Mbps
- True mini-LVDS output standard with data rates of up to 340 Mbps

| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| True Differential I/O Standards - $f_{HSDRDPA}$ (data rate) | SERDES factor J = 3 to 10 (192), (193), (194), (195), (196), (197) | 150 | — | 1250 | 150 | — | 1050 | Mbps |
| | SERDES factor J ≥ 4 LVDS RX with DPA (193), (195), (196), (197) | 150 | — | 1600 | 150 | — | 1250 | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (198) | — | (199) | (198) | — | (199) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (198) | — | (199) | (198) | — | (199) | Mbps |
| $f_{HSDR}$ (data rate) | SERDES factor J = 3 to 10 | (198) | — | (200) | (198) | — | (200) | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (198) | — | (199) | (198) | — | (199) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (198) | — | (199) | (198) | — | (199) | Mbps |

(192) The $F_{MAX}$ specification is based on the fast clock used for serial data. The interface $F_{MAX}$ is also dependent on the parallel clock domain which is design dependent and requires timing analysis.
(193) Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.
(194) Arria V GZ LVDS serialization and de-serialization factor needs to be x4 and above.
(195) Requires package skew compensation with PCB trace length.
(196) Do not mix single-ended I/O buffer within LVDS I/O bank.
(197) Chip-to-chip communication only with a maximum load of 5 pF.
(198) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.
(199) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.
(200) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

## DPA Mode High-Speed I/O Specifications

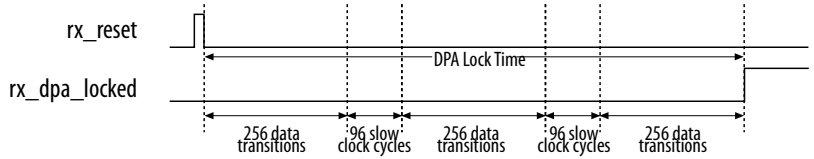
### Table 2-42: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| DPA run length | — | — | — | 10000 | — | — | 10000 | UI |

### Figure 2-3: DPA Lock Time Specification with DPA PLL Calibration Enabled




### Table 2-43: DPA Lock Time Specifications for Arria V GZ Devices

The DPA lock time is for one channel.

One data transition is defined as a 0-to-1 or 1-to-0 transition.

The DPA lock time stated in this table applies to both commercial and industrial grade.

| Standard | Training Pattern | Number of Data Transitions in One Repetition of the Training Pattern | Number of Repetitions per 256 Data Transitions (201) | Maximum |
|---|---|---|---|---|
| SPI-4 | 00000000001111111111 | 2 | 128 | 640 data transitions |

(201) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

## DLL Range Specifications

### Table 2-47: DLL Range Specifications for Arria V GZ Devices

Arria V GZ devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

| Parameter | C3, I3L | C4, I4 | Unit |
|---|---|---|---|
| DLL operating frequency range | 300 – 890 | 300 – 890 | MHz |

## DQS Logic Block Specifications

### Table 2-48: DQS Phase Offset Delay Per Setting for Arria V GZ Devices

The typical value equals the average of the minimum and maximum values.

The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a –3 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 11 ps) ± 20 ps] = 735 ps ± 20 ps.

| Speed Grade | Min | Max | Unit |
|---|---|---|---|
| C3, I3L | 8 | 15 | ps |
| C4, I4 | 8 | 16 | ps |

### Table 2-49: DQS Phase Shift Error Specification for DLL-Delayed Clock ($t_{DQS\_PSERR}$) for Arria V GZ Devices

This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a –3 speed grade is ±84 ps or ±42 ps.

| Number of DQS Delay Buffers | C3, I3L | C4, I4 | Unit |
|---|---|---|---|
| 1 | 30 | 32 | ps |
| 2 | 60 | 64 | ps |
| 3 | 90 | 96 | ps |

| Term | Definition |
|---|---|
| $t_C$ | High-speed receiver and transmitter input and output clock period. |
| TCCS (channel-to-channel-skew) | The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table). |
| $t_{DUTY}$ | High-speed I/O block—Duty cycle on the high-speed transmitter output clock. |
| $t_{FALL}$ | Signal high-to-low transition time (80-20%) |
| $t_{INCCJ}$ | Cycle-to-cycle jitter tolerance on the PLL clock input. |
| $t_{OUTPJ\_IO}$ | Period jitter on the general purpose I/O driven by a PLL. |
| $t_{OUTPJ\_DC}$ | Period jitter on the dedicated clock output driven by a PLL. |
| $t_{RISE}$ | Signal low-to-high transition time (20-80%) |
| Timing Unit Interval (TUI) | The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(receiver input clock frequency multiplication factor) = $t_C$/w) |
| $V_{CM(DC)}$ | DC common mode input voltage. |
| $V_{ICM}$ | Input common mode voltage—The common mode of the differential signal at the receiver. |
| $V_{ID}$ | Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| $V_{DIF(AC)}$ | AC differential input voltage—Minimum AC input differential voltage required for switching. |
| $V_{DIF(DC)}$ | DC differential input voltage— Minimum DC input differential voltage required for switching. |
| $V_{IH}$ | Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high. |
| $V_{IH(AC)}$ | High-level AC input voltage |
| $V_{IH(DC)}$ | High-level DC input voltage |
| $V_{IL}$ | Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low. |
| $V_{IL(AC)}$ | Low-level AC input voltage |
| $V_{IL(DC)}$ | Low-level DC input voltage |

| Term | Definition |
|---|---|
| $V_{OCM}$ | Output common mode voltage—The common mode of the differential signal at the transmitter. |
| $V_{OD}$ | Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. |
| $V_{SWING}$ | Differential input voltage |
| $V_X$ | Input differential cross point voltage |
| $V_{OX}$ | Output differential cross point voltage |
| W | High-speed I/O block—clock boost factor |

## Document Revision History

| Date | Version | Changes |
|---|---|---|
| February 2017 | 2017.02.10 | • Changed the minimum value for $t_{CD2UMC}$ in the “FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1” table.<br>• Changed the minimum value for $t_{CD2UMC}$ in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1" table.<br>• Changed the minimum value for $t_{CD2UMC}$ in the "AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices" table.<br>• Changed the minimum value for $t_{CD2UMC}$ in the "PS Timing Parameters for Arria V GZ Devices" table.<br>• Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices" table. |