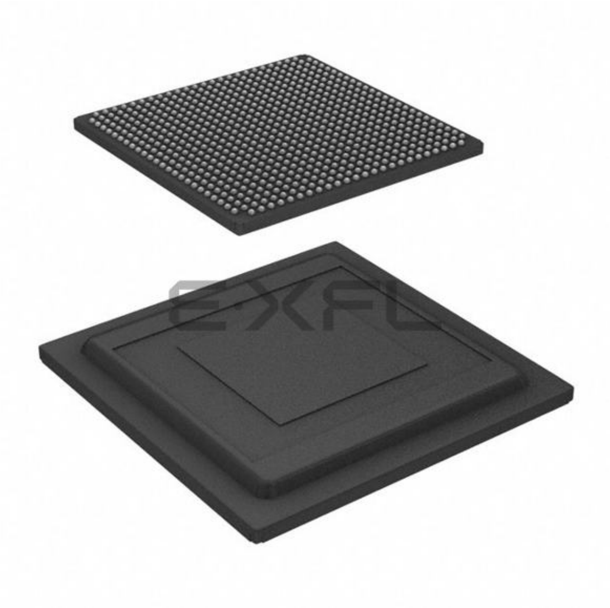

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 3537 |
| Number of Logic Elements/Cells | 75000 |
| Total RAM Bits | 8666112 |
| Number of I/O | 336 |
| Number of Gates | - |
| Voltage - Supply | 1.07V ~ 1.13V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 672-BBGA, FCBGA |
| Supplier Device Package | 672-FBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5agxma1d4f27c4n |

Email: info@E-XFL.COM Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

| Symbol | Description | Condition | Minimum[1] | Typical | Maximum[1] | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O buffers power supply | 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | | 3.0 V | 2.85 | 3.0 | 3.15 | V |
| | | 2.5 V | 2.375 | 2.5 | 2.625 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | V |
| | | 1.5 V | 1.425 | 1.5 | 1.575 | V |
| | | 1.35 V | 1.283 | 1.35 | 1.418 | V |
| | | 1.25 V | 1.19 | 1.25 | 1.31 | V |
| | | 1.2 V | 1.14 | 1.2 | 1.26 | V |
| $V_{CCD\_FPLL}$ | PLL digital voltage regulator power supply | — | 1.425 | 1.5 | 1.575 | V |
| $V_{CCA\_FPLL}$ | PLL analog voltage regulator power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_I$ | DC input voltage | — | –0.5 | — | 3.6 | V |
| $V_O$ | Output voltage | — | 0 | — | $V_{CCIO}$ | V |
| $T_J$ | Operating junction temperature | Commercial | 0 | — | 85 | °C |
| | | Industrial | –40 | — | 100 | °C |
| $t_{RAMP}$[4] | Power supply ramp time | Standard POR | 200 µs | — | 100 ms | — |
| | | Fast POR | 200 µs | — | 4 ms | — |

(1) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(4) This is also applicable to HPS power supply. For HPS power supply, refer to $t_{RAMP}$ specifications for standard POR when `HPS_PORSEL` = 0 and $t_{RAMP}$ specifications for fast POR when `HPS_PORSEL` = 1.

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{SWING(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{SWING(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Max |
| SSTL-125 | 1.19 | 1.25 | 1.31 | 0.18 | (15) | $V_{CCIO}/2 - 0.15$ | $V_{CCIO}/2$ | $V_{CCIO}/2 + 0.15$ | $2(V_{IH(AC)} - V_{REF})$ | $2(V_{IL(AC)} - V_{REF})$ |

## Differential HSTL and HSUL I/O Standards

### Table 1-18: Differential HSTL and HSUL I/O Standards for Arria V Devices

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.78 | — | 1.12 | 0.78 | — | 1.12 | 0.4 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.68 | — | 0.9 | 0.68 | — | 0.9 | 0.4 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | $V_{CCIO} + 0.3$ | — | $0.5 \times V_{CCIO}$ | — | $0.4 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.6 \times V_{CCIO}$ | 0.3 | $V_{CCIO} + 0.48$ |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.26 | 0.26 | $0.5 \times V_{CCIO} - 0.12$ | $0.5 \times V_{CCIO}$ | $0.5 \times V_{CCIO} + 0.12$ | $0.4 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.6 \times V_{CCIO}$ | 0.44 | 0.44 |

## Differential I/O Standard Specifications

### Table 1-19: Differential I/O Standard Specifications for Arria V Devices

Differential inputs are powered by $V_{CCPD}$ which requires 2.5 V.

| Symbol/Description | Condition | Transceiver Speed Grade 4 | | | Transceiver Speed Grade 6 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Minimum differential eye opening at the receiver serial input pins[30] | — | 100 | — | — | 100 | — | — | mV |
| $V_{ICM}$ (AC coupled) | — | — | 0.7/0.75/ 0.8[31] | — | — | 0.7/0.75/ 0.8 [31] | — | mV |
| $V_{ICM}$ (DC coupled) | ≤ 3.2Gbps[32] | 670 | 700 | 730 | 670 | 700 | 730 | mV |
| Differential on-chip termination resistors | 85-Ω setting | — | 85 | — | — | 85 | — | Ω |
| | 100-Ω setting | — | 100 | — | — | 100 | — | Ω |
| | 120-Ω setting | — | 120 | — | — | 120 | — | Ω |
| | 150-Ω setting | — | 150 | — | — | 150 | — | Ω |
| $t_{LTR}$[33] | — | — | — | 10 | — | — | 10 | µs |
| $t_{LTD}$[34] | — | 4 | — | — | 4 | — | — | µs |
| $t_{LTD\_manual}$[35] | — | 4 | — | — | 4 | — | — | µs |
| $t_{LTR\_LTD\_manual}$[36] | — | 15 | — | — | 15 | — | — | µs |
| Programmable ppm detector[37] | — | ±62.5, 100, 125, 200, 250, 300, 500, and 1000 | | | | | | ppm |

(30) The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(31) The AC coupled $V_{ICM}$ = 700 mV for Arria V GX and SX in PCIe mode only. The AC coupled $V_{ICM}$ = 750 mV for Arria V GT and ST in PCIe mode only.

(32) For standard protocol compliance, use AC coupling.

(33) $t_{LTR}$ is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(34) $t_{LTD}$ is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(35) $t_{LTD\_manual}$ is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(36) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

| Symbol/Description | Condition | Transceiver Speed Grade 4 | | | Transceiver Speed Grade 6 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Run length | — | — | — | 200 | — | — | 200 | UI |
| Programmable equalization AC and DC gain | AC gain setting = 0 to 3[38]<br>DC gain setting = 0 to 1 | Refer to CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices and CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices diagrams. | | | | | | dB |

### Table 1-23: Transmitter Specifications for Arria V GX and SX Devices

| Symbol/Description | Condition | Transceiver Speed Grade 4 | | | Transceiver Speed Grade 6 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supported I/O standards | 1.5 V PCML | | | | | | | |
| Data rate | — | 611 | — | 6553.6 | 611 | — | 3125 | Mbps |
| $V_{OCM}$ (AC coupled) | — | — | 650 | — | — | 650 | — | mV |
| $V_{OCM}$ (DC coupled) | ≤ 3.2Gbps[32] | 670 | 700 | 730 | 670 | 700 | 730 | mV |
| Differential on-chip termination resistors | 85-Ω setting | — | 85 | — | — | 85 | — | Ω |
| | 100-Ω setting | — | 100 | — | — | 100 | — | Ω |
| | 120-Ω setting | — | 120 | — | — | 120 | — | Ω |
| | 150-Ω setting | — | 150 | — | — | 150 | — | Ω |
| Intra-differential pair skew | TX $V_{CM}$ = 0.65 V (AC coupled) and slew rate of 15 ps | — | — | 15 | — | — | 15 | ps |
| Intra-transceiver block transmitter channel-to-channel skew | ×6 PMA bonded mode | — | — | 180 | — | — | 180 | ps |

(37) The rate match FIFO supports only up to ±300 parts per million (ppm).
(38) The Quartus Prime software allows AC gain setting = 3 for design with data rate between 611 Mbps and 1.25 Gbps only.

| Symbol/Description | Condition | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $t_{LTD\_manual}$[51] | — | 4 | — | — | µs |
| $t_{LTR\_LTD\_manual}$[52] | — | 15 | — | — | µs |
| Programmable ppm detector[53] | — | ±62.5, 100, 125, 200, 250, 300, 500, and 1000 | | | ppm |
| Run length | — | — | — | 200 | UI |
| Programmable equalization AC and DC gain | AC gain setting = 0 to 3[54]<br>DC gain setting = 0 to 1 | Refer to CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices and CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices diagrams. | | | |

**Table 1-29: Transmitter Specifications for Arria V GT and ST Devices**

| Symbol/Description | Condition | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Supported I/O standards | 1.5 V PCML | | | | |
| Data rate (6-Gbps transceiver) | — | 611 | — | 6553.6 | Mbps |
| Data rate (10-Gbps transceiver) | — | 0.611 | — | 10.3125 | Gbps |
| $V_{OCM}$ (AC coupled) | — | — | 650 | — | mV |
| $V_{OCM}$ (DC coupled) | ≤ 3.2 Gbps[48] | 670 | 700 | 730 | mV |

(51) $t_{LTD\_manual}$ is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(52) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

(53) The rate match FIFO supports only up to ±300 ppm.

(54) The Quartus Prime software allows AC gain setting = 3 for design with data rate between 611 Mbps and 1.25 Gbps only.

| Protocol | Sub-protocol | Data Rate (Mbps) |
|---|---|---|
| Common Public Radio Interface (CPRI) | CPRI E6LV | 614.4 |
| | CPRI E6HV | 614.4 |
| | CPRI E6LVII | 614.4 |
| | CPRI E12LV | 1,228.8 |
| | CPRI E12HV | 1,228.8 |
| | CPRI E12LVII | 1,228.8 |
| | CPRI E24LV | 2,457.6 |
| | CPRI E24LVII | 2,457.6 |
| | CPRI E30LV | 3,072 |
| | CPRI E30LVII | 3,072 |
| | CPRI E48LVII | 4,915.2 |
| | CPRI E60LVII | 6,144 |
| | CPRI E96LVIII[60] | 9,830.4 |
| Gbps Ethernet (GbE) | GbE 1250 | 1,250 |
| OBSAI | OBSAI 768 | 768 |
| | OBSAI 1536 | 1,536 |
| | OBSAI 3072 | 3,072 |
| | OBSAI 6144 | 6,144 |
| Serial digital interface (SDI) | SDI 270 SD | 270 |
| | SDI 1485 HD | 1,485 |
| | SDI 2970 3G | 2,970 |

(60) You can achieve compliance with TX channel restriction of one HSSI channel per six-channel transceiver bank.

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency | –3 speed grade | 5 | — | 800[61] | MHz |
| | | –4 speed grade | 5 | — | 800[61] | MHz |
| | | –5 speed grade | 5 | — | 750[61] | MHz |
| | | –6 speed grade | 5 | — | 625[61] | MHz |
| $f_{INPFD}$ | Integer input clock frequency to the phase frequency detector (PFD) | — | 5 | — | 325 | MHz |
| $f_{FINPFD}$ | Fractional input clock frequency to the PFD | — | 50 | — | 160 | MHz |
| $f_{VCO}$[62] | PLL voltage-controlled oscillator (VCO) operating range | –3 speed grade | 600 | — | 1600 | MHz |
| | | –4 speed grade | 600 | — | 1600 | MHz |
| | | –5 speed grade | 600 | — | 1600 | MHz |
| | | –6 speed grade | 600 | — | 1300 | MHz |
| $t_{EINDUTY}$ | Input clock or external feedback clock input duty cycle | — | 40 | — | 60 | % |
| $f_{OUT}$ | Output frequency for internal global or regional clock | –3 speed grade | — | — | 500[63] | MHz |
| | | –4 speed grade | — | — | 500[63] | MHz |
| | | –5 speed grade | — | — | 500[63] | MHz |
| | | –6 speed grade | — | — | 400[63] | MHz |

(61) This specification is limited in the Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(62) The VCO frequency reported by the Quartus Prime software takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the $f_{VCO}$ specification.

(63) This specification is limited by the lower of the two: I/O $f_{MAX}$ or $F_{OUT}$ of the PLL.

## High-Speed I/O Specifications

### Table 1-40: High-Speed I/O Specifications for Arria V Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block. When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

The Arria V devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 360 Mbps
- True mini-LVDS output standard with data rates of up to 400 Mbps

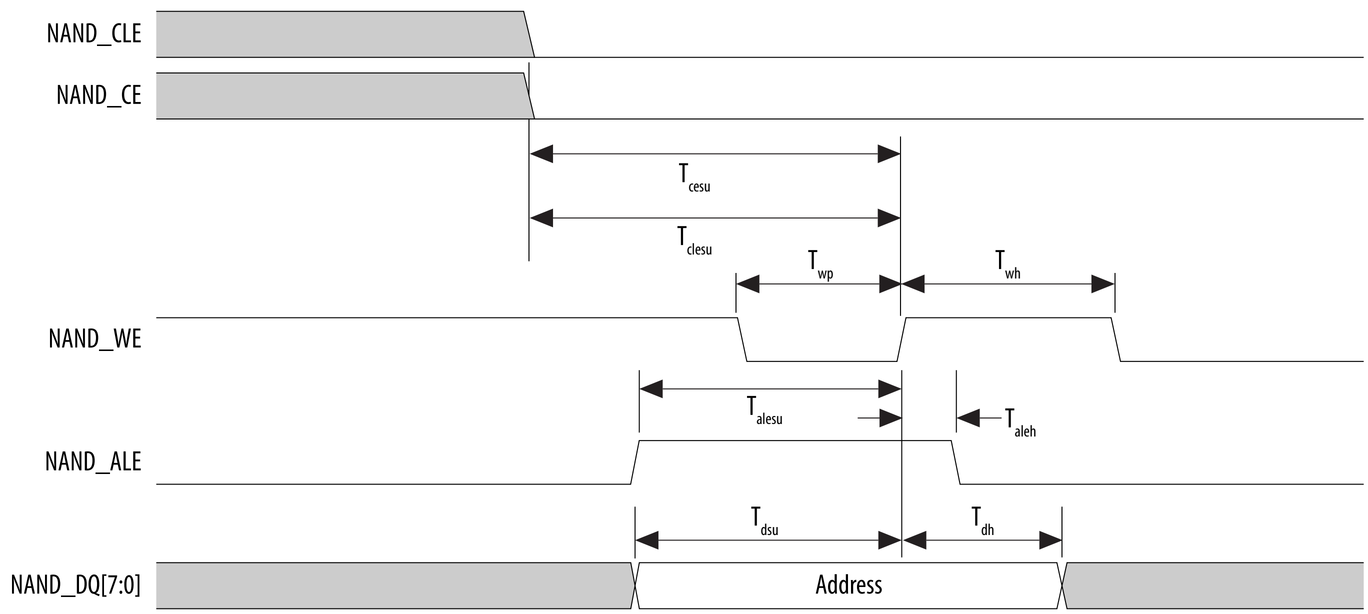
| Symbol | | Condition | –I3, –C4 | | | –I5, –C5 | | | –C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK\_in}$ (input clock frequency) True Differential I/O Standards | | Clock boost factor W = 1 to 40[72] | 5 | — | 800 | 5 | — | 750 | 5 | — | 625 | MHz |
| $f_{HSCLK\_in}$ (input clock frequency) Single-Ended I/O Standards[73] | | Clock boost factor W = 1 to 40[72] | 5 | — | 625 | 5 | — | 625 | 5 | — | 500 | MHz |
| $f_{HSCLK\_in}$ (input clock frequency) Single-Ended I/O Standards[74] | | Clock boost factor W = 1 to 40[72] | 5 | — | 420 | 5 | — | 420 | 5 | — | 420 | MHz |
| $f_{HSCLK\_OUT}$ (output clock frequency) | | — | 5 | — | 625[75] | 5 | — | 625[75] | 5 | — | 500[75] | MHz |
| Transmitter | True Differential I/O Standards - $f_{HSDR}$ (data rate) | SERDES factor J =3 to 10[76] | [77] | — | 1250 | [77] | — | 1250 | [77] | — | 1050 | Mbps |

(72) Clock boost factor (W) is the ratio between the input data rate and the input clock rate.
(73) This applies to DPA and soft-CDR modes only.
(74) This applies to non-DPA mode only.
(75) This is achieved by using the LVDS clock network.
(76) The $F_{max}$ specification is based on the fast clock used for serial data. The interface $F_{max}$ is also dependent on the parallel clock domain which is design dependent and requires timing analysis.
(77) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

| Symbol | Condition | –I3, –C4 | | | –I5, –C5 | | | –C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | SERDES factor J ≥ 8[76][78], LVDS TX with RX DPA | [77] | — | 1600 | [77] | — | 1500 | [77] | — | 1250 | Mbps |
| | SERDES factor J = 1 to 2, Uses DDR Registers | [77] | — | [79] | [77] | — | [79] | [77] | — | [79] | Mbps |
| Emulated Differential I/O Standards with Three External Output Resistor Network - $f_{HSDR}$ (data rate)[80] | SERDES factor J = 4 to 10[81] | [77] | — | 945 | [77] | — | 945 | [77] | — | 945 | Mbps |
| Emulated Differential I/O Standards with One External Output Resistor Network - $f_{HSDR}$ (data rate)[80] | SERDES factor J = 4 to 10[81] | [77] | — | 200 | [77] | — | 200 | [77] | — | 200 | Mbps |
| $t_{x\ Jitter}$ -True Differential I/O Standards | Total Jitter for Data Rate 600 Mbps – 1.25 Gbps | — | — | 160 | — | — | 160 | — | — | 160 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | UI |

(78) The $V_{CC}$ and $V_{CCP}$ must be on a separate power layer and a maximum load of 5 pF for chip-to-chip interface.
(79) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency ($f_{OUT}$), provided you can close the design timing and the signal integrity simulation is clean.
(80) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.
(81) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

**Figure 1-18: NAND Address Latch Timing Diagram**



## I/O Standard Specifications

The $V_{OL}$ and $V_{OH}$ values are valid at the corresponding $I_{OH}$ and $I_{OL}$, respectively.

### Table 2-16: Single-Ended I/O Standards for Arria V GZ Devices

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{IL}$ (V) | | $V_{IH}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| LVTTL | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.6 | 0.4 | 2.4 | 2 | –2 |
| LVCMOS | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| 2.5 V | 2.375 | 2.5 | 2.625 | –0.3 | 0.7 | 1.7 | 3.6 | 0.4 | 2 | 1 | –1 |
| 1.8 V | 1.71 | 1.8 | 1.89 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.45 | $V_{CCIO}$ – 0.45 | 2 | –2 |
| 1.5 V | 1.425 | 1.5 | 1.575 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 2 | –2 |
| 1.2 V | 1.14 | 1.2 | 1.26 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 2 | –2 |

### Table 2-17: Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V GZ Devices

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × VCCIO | 0.51 × $V_{CCIO}$ |

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Differential on-chip termination resistors | 85-Ω setting | — | 85 ± 20% | — | — | 85 ± 20% | — | Ω |
| | 100-Ω setting | — | 100 ± 20% | — | — | 100 ± 20% | — | Ω |
| | 120-Ω setting | — | 120 ± 20% | — | — | 120 ± 20% | — | Ω |
| | 150-Ω setting | — | 150 ± 20% | — | — | 150 ± 20% | — | Ω |
| $V_{OCM}$ (AC coupled) | 0.65-V setting | — | 650 | — | — | 650 | — | mV |
| $V_{OCM}$ (DC coupled) | — | — | 650 | — | — | 650 | — | mV |
| Intra-differential pair skew | Tx $V_{CM}$ = 0.5 V and slew rate of 15 ps | — | — | 15 | — | — | 15 | ps |
| Intra-transceiver block transmitter channel-to-channel skew | x6 PMA bonded mode | — | — | 120 | — | — | 120 | ps |
| Inter-transceiver block transmitter channel-to-channel skew | xN PMA bonded mode | — | — | 500 | — | — | 500 | ps |

**Related Information**

**Arria V Device Overview**

For more information about device ordering codes.

| Symbol | $V_{OD}$ Setting | $V_{OD}$ Value (mV) | $V_{OD}$ Setting | $V_{OD}$ Value (mV) |
|---|---|---|---|---|
| $V_{OD}$ **differential peak to peak typical** | 15 | 300 | 47 | 940 |
| | 16 | 320 | 48 | 960 |
| | 17 | 340 | 49 | 980 |
| | 18 | 360 | 50 | 1000 |
| | 19 | 380 | 51 | 1020 |
| | 20 | 400 | 52 | 1040 |
| | 21 | 420 | 53 | 1060 |
| | 22 | 440 | 54 | 1080 |
| | 23 | 460 | 55 | 1100 |
| | 24 | 480 | 56 | 1120 |
| | 25 | 500 | 57 | 1140 |
| | 26 | 520 | 58 | 1160 |
| | 27 | 540 | 59 | 1180 |
| | 28 | 560 | 60 | 1200 |
| | 29 | 580 | 61 | 1220 |
| | 30 | 600 | 62 | 1240 |
| | 31 | 620 | 63 | 1260 |

# Core Performance Specifications

## Clock Tree Specifications

### Table 2-33: Clock Tree Performance for Arria V GZ Devices

| Symbol | Performance | | Unit |
|---|---|---|---|
| | C3, I3L | C4, I4 | |
| Global and Regional Clock | 650 | 580 | MHz |
| Periphery Clock | 500 | 500 | MHz |

## PLL Specifications

### Table 2-34: PLL Specifications for Arria V GZ Devices

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{IN}$ (167) | Input clock frequency (C3, I3L speed grade) | 5 | — | 800 | MHz |
| | Input clock frequency (C4, I4 speed grade) | 5 | — | 650 | MHz |
| $f_{INPFD}$ | Input frequency to the PFD | 5 | — | 325 | MHz |
| $f_{FINPFD}$ | Fractional Input clock frequency to the PFD | 50 | — | 160 | MHz |
| $f_{VCO}$ (168) | PLL VCO operating range (C3, I3L speed grade) | 600 | — | 1600 | MHz |
| | PLL VCO operating range (C4, I4 speed grade) | 600 | — | 1300 | MHz |
| $t_{EINDUTY}$ | Input clock or external feedback clock input duty cycle | 40 | — | 60 | % |

(167) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(168) The VCO frequency reported by the Quartus II software in the **PLL Usage Summary** section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the $f_{VCO}$ specification.

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $k_{VALUE}$ | Numerator of Fraction | 128 | 8388608 | 2147483648 | — |
| $f_{RES}$ | Resolution of VCO frequency ($f_{INPFD}$ = 100 MHz) | 390625 | 5.96 | 0.023 | Hz |

**Related Information**

- Duty Cycle Distortion (DCD) Specifications on page 2-56
- DLL Range Specifications on page 2-53

## DSP Block Specifications

### Table 2-35: DSP Block Performance Specifications for Arria V GZ Devices

| Mode | Performance | | | Unit |
|---|---|---|---|---|
| | C3, I3L | C4 | I4 | |
| **Modes using One DSP Block** | | | | |
| Three 9 × 9 | 480 | 420 | | MHz |
| One 18 × 18 | 480 | 420 | 400 | MHz |
| Two partial 18 × 18 (or 16 × 16) | 480 | 420 | 400 | MHz |
| One 27 × 27 | 400 | 350 | | MHz |
| One 36 × 18 | 400 | 350 | | MHz |
| One sum of two 18 × 18 (One sum of two 16 × 16) | 400 | 350 | | MHz |
| One sum of square | 400 | 350 | | MHz |
| One 18 × 18 plus 36 (a × b) + c | 400 | 350 | | MHz |
| **Modes using Two DSP Blocks** | | | | |
| Three 18 × 18 | 400 | 350 | | MHz |
| One sum of four 18 × 18 | 380 | 300 | | MHz |

| Number of DQS Delay Buffers | C3, I3L | C4, I4 | Unit |
|---|---|---|---|
| 4 | 120 | 128 | ps |

## Memory Output Clock Jitter Specifications

### Table 2-50: Memory Output Clock Jitter Specification for Arria V GZ Devices

The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

| Clock Network | Parameter | Symbol | C3, I3L | | C4, I4 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| Regional | Clock period jitter | $t_{JIT(per)}$ | –55 | 55 | –55 | 55 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | –110 | 110 | –110 | 110 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | –82.5 | 82.5 | –82.5 | 82.5 | ps |
| Global | Clock period jitter | $t_{JIT(per)}$ | –82.5 | 82.5 | –82.5 | 82.5 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | –165 | 165 | –165 | 165 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | –90 | 90 | –90 | 90 | ps |
| PHY Clock | Clock period jitter | $t_{JIT(per)}$ | –30 | 30 | –35 | 35 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | –60 | 60 | –70 | 70 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | –45 | 45 | –56 | 56 | ps |

**Table 2-57: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1**

Use these timing parameters when you use the decompression and design security features.

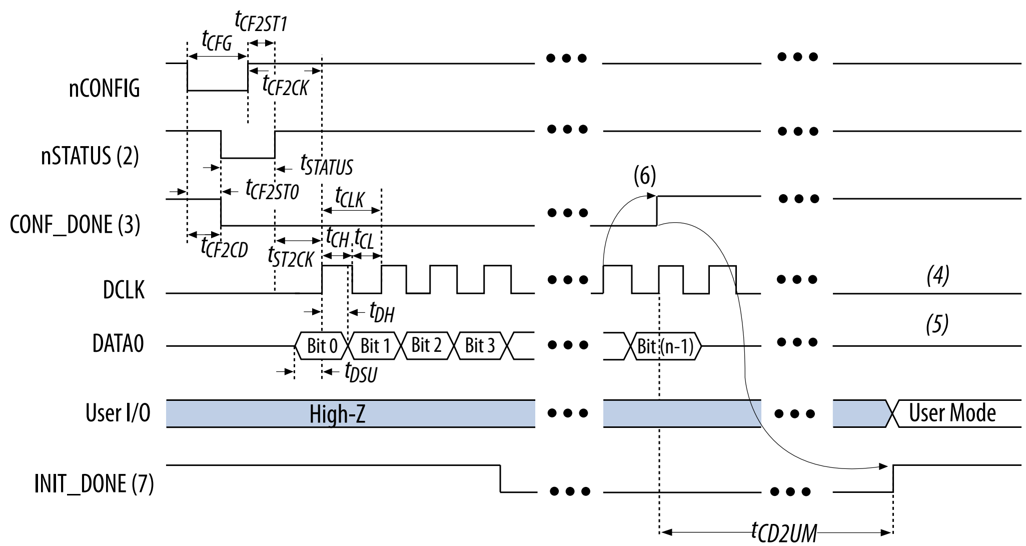
| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 600 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 600 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 1,506 (210) | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 1,506 (211) | µs |
| $t_{CF2CK}$ (212) | nCONFIG high to first rising edge on DCLK | 1,506 | — | µs |
| $t_{ST2CK}$ (212) | nSTATUS high to first rising edge of DCLK | 2 | — | µs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | $N-1/f_{DCLK}$ (213) | — | s |
| $t_{CH}$ | DCLK high time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | $1/f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency (FPP ×8/×16) | — | 125 | MHz |
| | DCLK frequency (FPP ×32) | — | 100 | MHz |
| $t_R$ | Input rise time | — | 40 | ns |
| $t_F$ | Input fall time | — | 40 | ns |
| $t_{CD2UM}$ | CONF_DONE high to user mode (214) | 175 | 437 | µs |

(210) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(211) You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.
(212) If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.
(213) N is the DCLK-to-DATA ratio and $f_{DCLK}$ is the DCLK frequency the system is operating.
(214) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

# Passive Serial Configuration Timing

## Figure 2-10: PS Configuration Timing Waveform

Timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.




Notes:
1. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
2. After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.
3. After power-up, before and during configuration, CONF_DONE is low.
4. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
5. DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the Device and Pins Option.
6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
7. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

**Related Information**

- **Configuration, Design Security, and Remote System Upgrades in Arria V Devices**
  For more information about the reconfiguration input for the ALTREMOTE_UPDATE IP core, refer to the "User Watchdog Timer" section.
- **Configuration, Design Security, and Remote System Upgrades in Arria V Devices**
  For more information about the `reset_timer` input for the ALTREMOTE_UPDATE IP core, refer to the "Remote System Upgrade State Machine" section.

## User Watchdog Internal Oscillator Frequency Specification

**Table 2-65: User Watchdog Internal Oscillator Frequency Specifications**

| Minimum | Typical | Maximum | Unit |
|---|---|---|---|
| 5.3 | 7.9 | 12.5 | MHz |

# I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

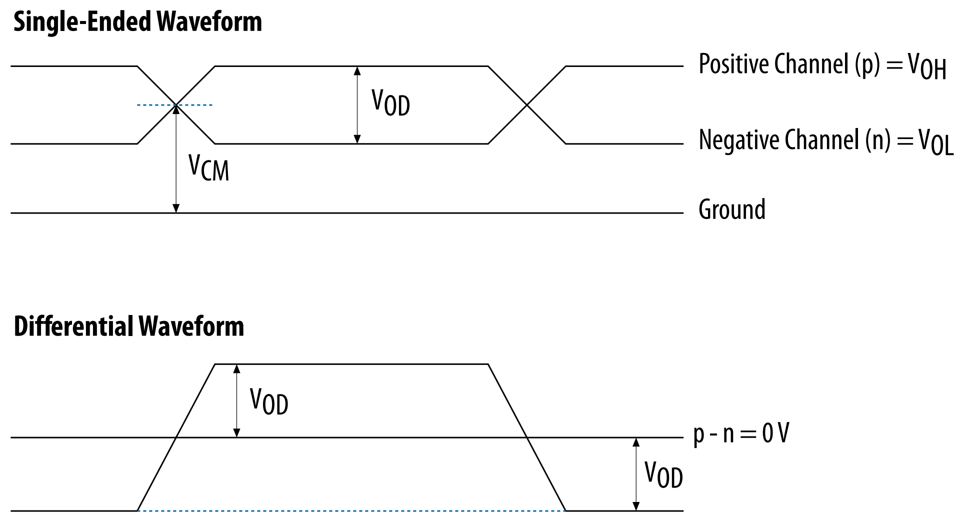
The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

**Related Information**

**Arria V Devices Documentation page**
For the Excel-based I/O Timing spreadsheet

(226) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification. For more information, refer to the "Remote System Upgrade State Machine" section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

(227) This is equivalent to strobing the reset_timer input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification. For more information, refer to the "User Watchdog Timer" section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

| Term | Definition |
|---|---|
| |  |
| $f_{HSCLK}$ | Left and right PLL input clock frequency. |
| $f_{HSDR}$ | High-speed I/O block—Maximum and minimum LVDS data transfer rate ($f_{HSDR}$ = 1/TUI), non-DPA. |
| $f_{HSDRDPA}$ | High-speed I/O block—Maximum and minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA. |
| J | High-speed I/O block—Deserialization factor (width of parallel data bus). |