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Intel - 5AGXMA1D4F31C4N Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	3537
Number of Logic Elements/Cells	75000
Total RAM Bits	8666112
Number of I/O	416
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxma1d4f31c4n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1-1: Absolute Maximum Ratings for Arria V Devices

Symbol	Description	Minimum	Maximum	Unit
V _{CC}	Core voltage power supply	-0.50	1.43	V
V _{CCP}	Periphery circuitry, PCIe [®] hardIP block, and transceiver physical coding sublayer (PCS) power supply	-0.50	1.43	V
V _{CCPGM}	Configuration pins power supply	-0.50	3.90	V
V _{CC_AUX}	Auxiliary supply	-0.50	3.25	V
V _{CCBAT}	Battery back-up power supply for design security volatile key register	-0.50	3.90	V
V _{CCPD}	I/O pre-driver power supply	-0.50	3.90	V
V _{CCIO}	I/O power supply	-0.50	3.90	V
V _{CCD_FPLL}	Phase-locked loop (PLL) digital power supply	-0.50	1.80	V
V _{CCA_FPLL}	PLL analog power supply	-0.50	3.25	V
V _{CCA_GXB}	Transceiver high voltage power	-0.50	3.25	V
V _{CCH_GXB}	Transmitter output buffer power	-0.50	1.80	V
V _{CCR_GXB}	Receiver power	-0.50	1.50	V
V _{CCT_GXB}	Transmitter power	-0.50	1.50	V
V _{CCL_GXB}	Transceiver clock network power	-0.50	1.50	V
VI	DC input voltage	-0.50	3.80	V
V _{CC_HPS}	HPS core voltage and periphery circuitry power supply	-0.50	1.43	V
V _{CCPD_HPS}	HPS I/O pre-driver power supply	-0.50	3.90	V
V _{CCIO_HPS}	HPS I/O power supply	-0.50	3.90	V
V _{CCRSTCLK_HPS}	HPS reset and clock input pins power supply	-0.50	3.90	V



Symbol	Description	Condition	Minimum ⁽⁷⁾	Typical	Maximum ⁽⁷⁾	Unit
V _{CC_AUX_SHARED}	HPS auxiliary power supply	_	2.375	2.5	2.625	V

Related Information

Recommended Operating Conditions on page 1-4 Provides the steady-state voltage values for the FPGA portion of the device.

DC Characteristics

Supply Current and Power Consumption

Altera offers two ways to estimate power for your design-the Excel-based Early Power Estimator (EPE) and the Quartus® Prime PowerPlay Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the resources you use.

The Quartus Prime PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-androute. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

Related Information

- PowerPlay Early Power Estimator User Guide Provides more information about power estimation tools.
- PowerPlay Power Analysis chapter, Quartus Prime Handbook Provides more information about power estimation tools.



⁽⁷⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Symbol/Description	Condition	Tran	Unit		
Symbol/Description	Condition	Min	Тур	Max	Ont
	85- Ω setting	—	85	—	Ω
Differential on-chip termination	100- Ω setting	—	100	—	Ω
resistors	120-Ω setting	—	120	—	Ω
	150-Ω setting		150	_	Ω
Intra-differential pair skew	TX V_{CM} = 0.65 V (AC coupled) and slew rate of 15 ps			15	ps
Intra-transceiver block transmitter channel-to-channel skew	×6 PMA bonded mode			180	ps
Inter-transceiver block transmitter channel-to-channel skew ⁽⁵⁵⁾	× <i>N</i> PMA bonded mode			500	ps

Table 1-30: CMU PLL Specifications for Arria V GT and ST Devices

Symbol/Description	Transceiver S	peed Grade 3	Unit	
Symbol Description	Min	Max	onit	
Supported data range	0.611	10.3125	Gbps	
fPLL supported data range	611	3125	Mbps	

⁽⁵⁵⁾ This specification is only applicable to channels on one side of the device across two transceiver banks.



Typical TX V_{OD} Setting for Arria V Transceiver Channels with termination of 100 Ω

Table 1-32: Typical TX Vor	Setting for Arria V Tran	sceiver Channels with	termination of 100 Ω

Symbol	V _{OD} Setting ⁽⁵⁸⁾	V _{OD} Value (mV)	V _{OD} Setting ⁽⁵⁸⁾	V _{OD} Value (mV)
	6 ⁽⁵⁹⁾	120	34	680
	7 ⁽⁵⁹⁾	140	35	700
	8(59)	160	36	720
	9	180	37	740
	10	200	38	760
	11	220	39	780
	12	240	40	800
	13	260	41	820
	14	280	42	840
V _{OD} differential peak-to-peak typical	15	300	43	860
71	16	320	44	880
	17	340	45	900
	18	360	46	920
	19	380	47	940
	20	400	48	960
	21	420	49	980
	22	440	50	1000
	23	460	51	1020
	24	480	52	1040

⁽⁵⁸⁾ Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

⁽⁵⁹⁾ Only valid for data rates \leq 5 Gbps.



Symbol	V _{OD} Setting ⁽⁵⁸⁾	V _{OD} Value (mV)	V _{OD} Setting ⁽⁵⁸⁾	V _{OD} Value (mV)
	25	500	53	1060
	26	520	54	1080
	27	540	55	1100
	28	560	56	1120
	29	580	57	1140
	30	600	58	1160
	31	620	59	1180
	32	640	60	1200
	33	660		

Transmitter Pre-Emphasis Levels

The following table lists the simulation data on the transmitter pre-emphasis levels in dB for the first post tap under the following conditions:

- Low-frequency data pattern—five 1s and five 0s
- Data rate—2.5 Gbps

The levels listed are a representation of possible pre-emphasis levels under the specified conditions only and the pre-emphasis levels may change with data pattern and data rate.

Arria V devices only support 1st post tap pre-emphasis with the following conditions:

- The 1st post tap pre-emphasis settings must satisfy $|B| + |C| \le 60$ where $|B| = V_{OD}$ setting with termination value, $R_{TERM} = 100 \Omega$ and |C| = 1st post tap pre-emphasis setting.
- |B| |C| > 5 for data rates < 5 Gbps and |B| |C| > 8.25 for data rates > 5 Gbps.
- $(V_{MAX}/V_{MIN} 1)\% < 600\%$, where $V_{MAX} = |B| + |C|$ and $V_{MIN} = |B| |C|$.

Exception for PCIe Gen2 design: V_{OD} setting = 43 and pre-emphasis setting = 19 are allowed for PCIe Gen2 design with transmit de-emphasis – 6dB setting (pipe_txdeemp = 1'b0) using Altera PCIe Hard IP and PIPE IP cores.



⁽⁵⁸⁾ Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

1-62 SPI Timing Characteristics

Symbol	Description	Min	Max	Unit
T _h	SPI MISO hold time	1	_	ns
T _{dutycycle}	SPI_CLK duty cycle	45	55	%
T _{dssfrst}	Output delay SPI_SS valid before first clock edge	8		ns
T _{dsslst}	Output delay SPI_SS valid after last clock edge	8		ns
T _{dio}	Master-out slave-in (MOSI) output delay	-1	1	ns

Altera Corporation

Arria V GX, GT, SX, and ST Device Datasheet



⁽⁸⁶⁾ This value is based on rx_sample_dly = 1 and spi_m_clk = 120 MHz. spi_m_clk is the internal clock that is used by SPI Master to derive it's SCLK_OUT. These timings are based on rx_sample_dly of 1. This delay can be adjusted as needed to accommodate slower response times from the slave. Note that a delay of 0 is not allowed. The setup time can be used as a reference starting point. It is very crucial to do a calibration to get the correct rx_sample_dly value because each SPI slave device may have different output delay and each application board may have different path delay. For more information about rx_sample_delay, refer to the SPI Controller chapter in the Hard Processor System Technical Reference Manual.

Figure 1-11: SD/MMC Timing Diagram



Related Information

Booting and Configuration Chapter, Arria V Hard Processor System Technical Reference Manual Provides more information about CSEL pin settings in the SD/MMC Controller CSEL Pin Settings table.

USB Timing Characteristics

PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board.

Table 1-55: USB Timing Requirements for Arria V Devices

Symbol	Description	Min	Тур	Мах	Unit
T _{clk}	USB CLK clock period	—	16.67	_	ns
T _d	CLK to USB_STP/USB_DATA[7:0] output delay	4.4	_	11	ns
T _{su}	Setup time for USB_DIR/USB_NXT/USB_DATA[7:0]	2			ns
T _h	Hold time for USB_DIR/USB_NXT/USB_DATA[7:0]	1			ns



Table 1-57: RGMII RX Timing Requirements for Arria V Devices

Symbol	Description	Min	Тур	Unit
T _{clk} (1000Base-T)	RX_CLK clock period		8	ns
T _{clk} (100Base-T)	RX_CLK clock period		40	ns
T _{clk} (10Base-T)	RX_CLK clock period		400	ns
T _{su}	RX_D/RX_CTL setup time	1		ns
T _h	RX_D/RX_CTL hold time	1		ns

Figure 1-14: RGMII RX Timing Diagram



Table 1-58: Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices

Symbol	Description	Min	Тур	Мах	Unit
T _{clk}	MDC clock period	—	400	_	ns
T _d	MDC to MDIO output data delay	10		20	ns
T _s	Setup time for MDIO data	10	_		ns
T _h	Hold time for MDIO data	0			ns



Figure 1-18: NAND Address Latch Timing Diagram







2-2 Absolute Maximum Ratings

Lower number refers to faster speed grade.

L = Low power devices.

Transcoiver Speed Grade		Core Speed Grade							
	C3	C4	I3L	14					
2	Yes	_	Yes	_					
3		Yes		Yes					

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Arria V GZ devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions other than those listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 2-2: Absolute Maximum Ratings for Arria V GZ Devices

Symbol	Description	Minimum	Maximum	Unit
V _{CC}	Power supply for core voltage and periphery circuitry	-0.5	1.35	V
V _{CCPT}	Power supply for programmable power technology	-0.5	1.8	V
V _{CCPGM}	Power supply for configuration pins	-0.5	3.9	V
V _{CC_AUX}	Auxiliary supply for the programmable power technology	-0.5	3.4	V
V _{CCBAT}	Battery back-up power supply for design security volatile key register	-0.5	3.9	V
V _{CCPD}	I/O pre-driver power supply	-0.5	3.9	V
V _{CCIO}	I/O power supply	-0.5	3.9	V
V _{CCD_FPLL}	PLL digital power supply	-0.5	1.8	V
V _{CCA_FPLL}	PLL analog power supply	-0.5	3.4	V



Symbol	Description	Minimum	Maximum	Unit
V _I	DC input voltage	-0.5	3.8	V
T _J	Operating junction temperature	-55	125	°C
T _{STG}	Storage temperature (No bias)	-65	150	°C
I _{OUT}	DC output current per pin	-25	40	mA

Table 2-3: Transceiver Power Supply Absolute Conditions for Arria V GZ Devices

Symbol	Description	Minimum	Maximum	Unit
V _{CCA_GXBL}	Transceiver channel PLL power supply (left side)	-0.5	3.75	V
V _{CCA_GXBR}	Transceiver channel PLL power supply (right side)	-0.5	3.75	V
V _{CCHIP_L}	Transceiver hard IP power supply (left side)	-0.5	1.35	V
V _{CCHSSI_L}	Transceiver PCS power supply (left side)	-0.5	1.35	V
V _{CCHSSI_R}	Transceiver PCS power supply (right side)	-0.5	1.35	V
V _{CCR_GXBL}	Receiver analog power supply (left side)	-0.5	1.35	V
V _{CCR_GXBR}	Receiver analog power supply (right side)	-0.5	1.35	V
V _{CCT_GXBL}	Transmitter analog power supply (left side)		1.35	V
V _{CCT_GXBR}	Transmitter analog power supply (right side)		1.35	V
V _{CCH_GXBL}	Transmitter output buffer power supply (left side)	-0.5	1.8	V
V _{CCH_GXBR}	Transmitter output buffer power supply (right side)	-0.5	1.8	V

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in the following table. They may also undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.



Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
Symbol/Description	Conditions	Min	Тур	Max	Min	Тур	Max	Onit
fixedclk clock frequency	PCIe Receiver Detect	_	100 or 125	_	_	100 or 125	_	MHz
Reconfiguration clock (mgmt_clk_ clk) frequency	—	100		125	100	_	125	MHz

Related Information

Arria V Device Overview

For more information about device ordering codes.

Receiver

Table 2-24: Receiver Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
Symbol/Description	Conditions	Min	Тур	Max	Min	Тур	Мах	Onic
Supported I/O Standards	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS							
Data rate (Standard PCS) (143), (144)	—	600		9900	600	_	8800	Mbps
Data rate (10G PCS) (143), (144)	_	600		12500	600	_	10312.5	Mbps
Absolute $\mathrm{V}_{\mathrm{MAX}}$ for a receiver pin $^{(145)}$	—			1.2			1.2	V
Absolute V_{MIN} for a receiver pin	_	-0.4	_		-0.4	_	_	V

⁽¹⁴³⁾ The line data rate may be limited by PCS-FPGA interface speed grade.

⁽¹⁴⁴⁾ To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.



⁽¹⁴⁵⁾ The device cannot tolerate prolonged operation at this absolute maximum.

Table 2-26: CMU PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the Arria V Device Overview.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transc	Unit		
	Conditions	Min	Тур	Max	Min	Тур	Мах	
Supported data range	_	600	_	12500	600	_	10312.5	Mbps
t _{pll_powerdown} ⁽¹⁵³⁾	—	1			1	_		μs
t _{pll_lock} ⁽¹⁵⁴⁾	_			10			10	μs

Related Information

Arria V Device Overview

For more information about device ordering codes.

ATX PLL

Table 2-27: ATX PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the Arria V Device Overview.

Arria V GZ Device Datasheet



 $t_{pll_powerdown}$ is the PLL powerdown minimum pulse width. (153)

⁽¹⁵⁴⁾ $t_{\text{pll} \text{ lock}}$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

Symbol	V _{OD} Setting	V _{OD} Value (mV)	V _{OD} Setting	V _{OD} Value (mV)
	15	300	47	940
	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
V_{OD} differential peak to peak typical	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260



Figure 2-2: AC Gain Curves for Arria V GZ Channels (full bandwidth)







t_{ARESET}

Symbol	Parameter	Min	Тур	Max	Unit
f	Output frequency for an internal global or regional clock (C3, I3L speed grade)	_	_	650	MHz
OUT	Output frequency for an internal global or regional clock (C4, I4 speed grade)	_		580	MHz
f (169)	Output frequency for an external clock output (C3, I3L speed grade)		_	667	MHz
LOUT_EXT	Output frequency for an external clock output (C4, I4 speed grade)	_	_	533	MHz
toutduty	Duty cycle for a dedicated external clock output (when set to 50%)	45	50	55	%
t _{FCOMP}	External feedback clock compensation time	—		10	ns
f _{DYCONFIGCLK}	Dynamic configuration clock for mgmt_clk and scanclk	_	_	100	MHz
t _{LOCK}	Time required to lock from the end-of-device configuration or deassertion of areset		_	1	ms
Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/ delays)		_	—	1	ms
	PLL closed-loop low bandwidth	_	0.3		MHz
f _{CLBW}	PLL closed-loop medium bandwidth	—	1.5		MHz
	PLL closed-loop high bandwidth (170)	_	4		MHz
t _{PLL_PSERR}	Accuracy of PLL phase shift	_	_	±50	ps

10

_

Minimum pulse width on the areset signal





ns

 $^{^{(169)}}$ This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.

⁽¹⁷⁰⁾ High bandwidth PLL settings are not supported in external feedback mode.

Momony	Modo	Resources Used			Unit			
Memory	moue	ALUTs	Memory	C3	C4	I3L	14	
	Single-port, all supported widths	0	1	650	550	500	450	MHz
Simple dual-port, all supported widths		0	1	650	550	500	450	MHz
	Simple dual-port with the read-during-write option set to Old Data , all supported widths	0	1	455	400	455	400	MHz
M20K Block	Simple dual-port with ECC enabled, 512×32	0	1	400	350	400	350	MHz
Diock	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	0	1	500	450	500	450	MHz
	True dual port, all supported widths	0	1	650	550	500	450	MHz
	ROM, all supported widths	0	1	650	550	500	450	MHz

Temperature Sensing Diode Specifications

Table 2-37: Internal Temperature Sensing Diode Specification

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
-40°C to 100°C	±8°C	No	1 MHz, 500 kHz	< 100 ms	8 bits	8 bits

Table 2-38: External Temperature Sensing Diode Specifications for Arria V GZ Devices

Description	Min	Тур	Max	Unit
I _{bias} , diode source current	8		200	μΑ
V _{bias,} voltage across diode	0.3		0.9	V
Series resistance		_	< 1	Ω



2-70 Remote System Upgrades Circuitry Timing Specification

Table 2-62: Uncompressed .rbf Sizes for Arria V GZ Devices

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ⁽²²³⁾
Arria V GZ	E1	137,598,880	562,208
	E3	137,598,880	562,208
	E5	213,798,880	561,760
	E7	213,798,880	561,760

Table 2-63: Minimum Configuration Time Estimation for Arria V GZ Devices

	Member Code	Active Serial ⁽²²⁴⁾			Fast Passive Parallel ⁽²²⁵⁾		
Variant		Width	DCLK (MHz)	Min Config Time (ms)	Width	DCLK (MHz)	Min Config Time (ms)
Arria V GZ	E1	4	100	344	32	100	43
	E3	4	100	344	32	100	43
	E5	4	100	534	32	100	67
	E7	4	100	534	32	100	67

Remote System Upgrades Circuitry Timing Specification

Table 2-64: Remote System Upgrade Circuitry Timing Specifications

Parameter	Minimum	Maximum	Unit
t _{RU_nCONFIG} ⁽²²⁶⁾	250	—	ns
t _{RU_nRSTIMER} ⁽²²⁷⁾	250	_	ns

⁽²²³⁾ The IOCSR **.rbf** size is specifically for the Configuration via Protocol (CvP) feature.

⁽²²⁴⁾ DCLK frequency of 100 MHz using external CLKUSR.

⁽²²⁵⁾ Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.



Related Information

- Configuration, Design Security, and Remote System Upgrades in Arria V Devices For more information about the reconfiguration input for the ALTREMOTE_UPDATE IP core, refer to the "User Watchdog Timer" section.
- Configuration, Design Security, and Remote System Upgrades in Arria V Devices For more information about the reset_timer input for the ALTREMOTE_UPDATE IP core, refer to the "Remote System Upgrade State Machine" section.

User Watchdog Internal Oscillator Frequency Specification

Table 2-65: User Watchdog Internal Oscillator Frequency Specifications

Minimum	Typical	Maximum	Unit	
5.3	7.9	12.5	MHz	

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete placeand-route.

Related Information

Arria V Devices Documentation page

For the Excel-based I/O Timing spreadsheet

Arria V GZ Device Datasheet



⁽²²⁶⁾ This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification. For more information, refer to the "Remote System Upgrade State Machine" section in the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.

⁽²²⁷⁾ This is equivalent to strobing the reset_timer input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification. For more information, refer to the "User Watchdog Timer" section in the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.

Glossary

Table 2-68: Glossary



