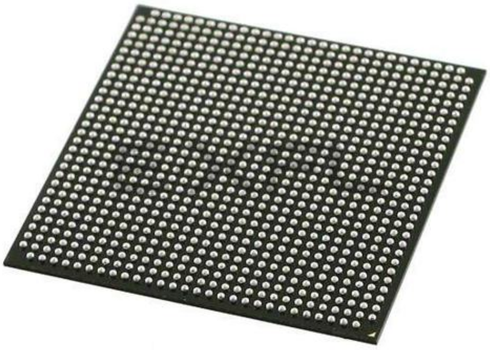

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	3537
Number of Logic Elements/Cells	75000
Total RAM Bits	8666112
Number of I/O	416
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxma1d6f31c6n

Symbol	Description	Minimum	Maximum	Unit
V_{CCPLL_HPS}	HPS PLL analog power supply	–0.50	3.25	V
$V_{CC\_AUX\_SHARED}$	HPS auxiliary power supply	–0.50	3.25	V
I_{OUT}	DC output current per pin	–25	40	mA
T_J	Operating junction temperature	–55	125	°C
T_{STG}	Storage temperature (no bias)	–65	150	°C

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 4.00 V can only be at 4.00 V for ~15% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 1.5 years.

Table 1-2: Maximum Allowed Overshoot During Transitions for Arria V Devices

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-125	1.19	1.25	1.31	0.18	(15)	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$

Differential HSTL and HSUL I/O Standards

Table 1-18: Differential HSTL and HSUL I/O Standards for Arria V Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	$V_{CCIO} + 0.3$	—	$0.5 \times V_{CCIO}$	—	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$	0.3	$V_{CCIO} + 0.48$
HSUL-12	1.14	1.2	1.3	0.26	0.26	$0.5 \times V_{CCIO} - 0.12$	$0.5 \times V_{CCIO}$	$0.5 \times V_{CCIO} + 0.12$	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$	0.44	0.44

Differential I/O Standard Specifications

Table 1-19: Differential I/O Standard Specifications for Arria V Devices

Differential inputs are powered by V_{CCPD} which requires 2.5 V.

- **Transceiver Specifications for Arria V GT and ST Devices** on page 1-29
  Provides the specifications for transmitter, receiver, and reference clock I/O pin.

Switching Characteristics

This section provides performance characteristics of Arria V core and periphery blocks.

Transceiver Performance Specifications

Transceiver Specifications for Arria V GX and SX Devices

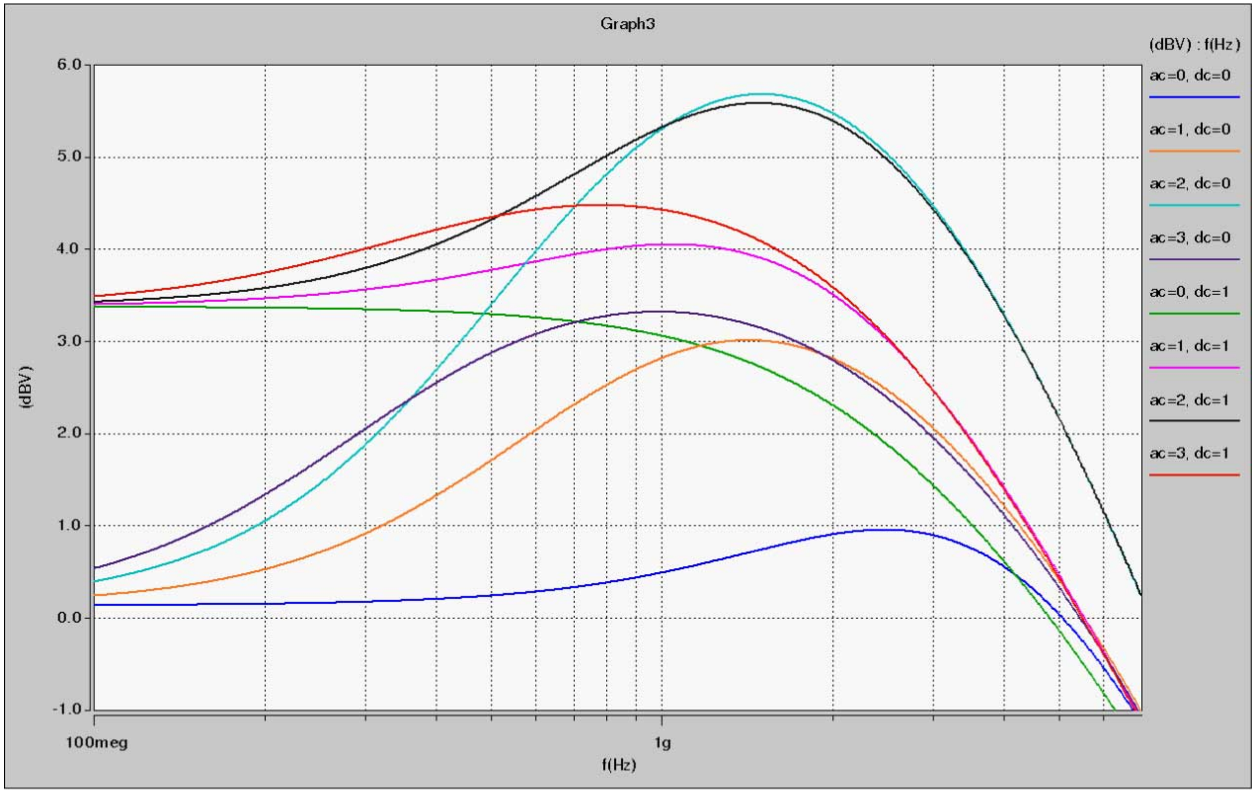
Table 1-20: Reference Clock Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported I/O standards	1.2 V PCML, 1.4 V PCML,1.5 V PCML, 2.5 V PCML, Differential LVPECL(23), HCSL, and LVDS							
Input frequency from REFCLK input pins	—	27	—	710	27	—	710	MHz
Rise time	Measure at ±60 mV of differential signal(24)	—	—	400	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal(24)	—	—	400	—	—	400	ps
Duty cycle	—	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	300(25)/ 2000	200	—	300(25)/ 2000	mV

(23) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.
(24) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
(25) The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain

Figure 1-3: CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices



Typical TX V_{OD} Setting for Arria V Transceiver Channels with termination of 100 Ω

Table 1-32: Typical TX V_{OD} Setting for Arria V Transceiver Channels with termination of 100 Ω

Symbol	V_{OD} Setting[58]	V_{OD} Value (mV)	V_{OD} Setting[58]	V_{OD} Value (mV)
V_{OD} differential peak-to-peak typical	6[59]	120	34	680
	7[59]	140	35	700
	8[59]	160	36	720
	9	180	37	740
	10	200	38	760
	11	220	39	780
	12	240	40	800
	13	260	41	820
	14	280	42	840
	15	300	43	860
	16	320	44	880
	17	340	45	900
	18	360	46	920
	19	380	47	940
	20	400	48	960
	21	420	49	980
	22	440	50	1000
	23	460	51	1020
	24	480	52	1040

(58) Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.
(59) Only valid for data rates ≤ 5 Gbps.

For example, when V_{OD} = 800 mV, the corresponding V_{OD} value setting is 40. The following conditions show that the 1st post tap pre-emphasis setting = 2 is valid:

- $|B| + |C| \leq 60 \rightarrow 40 + 2 = 42$
- $|B| - |C| > 5 \rightarrow 40 - 2 = 38$
- $(V_{MAX}/V_{MIN} - 1)\% < 600\% \rightarrow (42/38 - 1)\% = 10.52\%$

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Arria V HSSI HSPICE models.

Table 1-33: Transmitter Pre-Emphasis Levels for Arria V Devices

Quartus Prime 1st Post Tap Pre-Emphasis Setting	Quartus Prime V_{OD} Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
0	0	0	0	0	0	0	0	dB
1	1.97	0.88	0.43	0.32	0.24	0.19	0.13	dB
2	3.58	1.67	0.95	0.76	0.61	0.5	0.41	dB
3	5.35	2.48	1.49	1.2	1	0.83	0.69	dB
4	7.27	3.31	2	1.63	1.36	1.14	0.96	dB
5	—	4.19	2.55	2.1	1.76	1.49	1.26	dB
6	—	5.08	3.11	2.56	2.17	1.83	1.56	dB
7	—	5.99	3.71	3.06	2.58	2.18	1.87	dB
8	—	6.92	4.22	3.47	2.93	2.48	2.11	dB
9	—	7.92	4.86	4	3.38	2.87	2.46	dB
10	—	9.04	5.46	4.51	3.79	3.23	2.77	dB
11	—	10.2	6.09	5.01	4.23	3.61	—	dB
12	—	11.56	6.74	5.51	4.68	3.97	—	dB
13	—	12.9	7.44	6.1	5.12	4.36	—	dB
14	—	14.44	8.12	6.64	5.57	4.76	—	dB
15	—	—	8.87	7.21	6.06	5.14	—	dB

Quartus Prime 1st Post Tap Pre-Emphasis Setting	Quartus Prime V_{OD} Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
16	—	—	9.56	7.73	6.49	—	—	dB
17	—	—	10.43	8.39	7.02	—	—	dB
18	—	—	11.23	9.03	7.52	—	—	dB
19	—	—	12.18	9.7	8.02	—	—	dB
20	—	—	13.17	10.34	8.59	—	—	dB
21	—	—	14.2	11.1	—	—	—	dB
22	—	—	15.38	11.87	—	—	—	dB
23	—	—	—	12.67	—	—	—	dB
24	—	—	—	13.48	—	—	—	dB
25	—	—	—	14.37	—	—	—	dB
26	—	—	—	—	—	—	—	dB
27	—	—	—	—	—	—	—	dB
28	—	—	—	—	—	—	—	dB
29	—	—	—	—	—	—	—	dB
30	—	—	—	—	—	—	—	dB
31	—	—	—	—	—	—	—	dB

Related Information

SPICE Models for Altera Devices

Provides the Arria V HSSI HSPICE models.

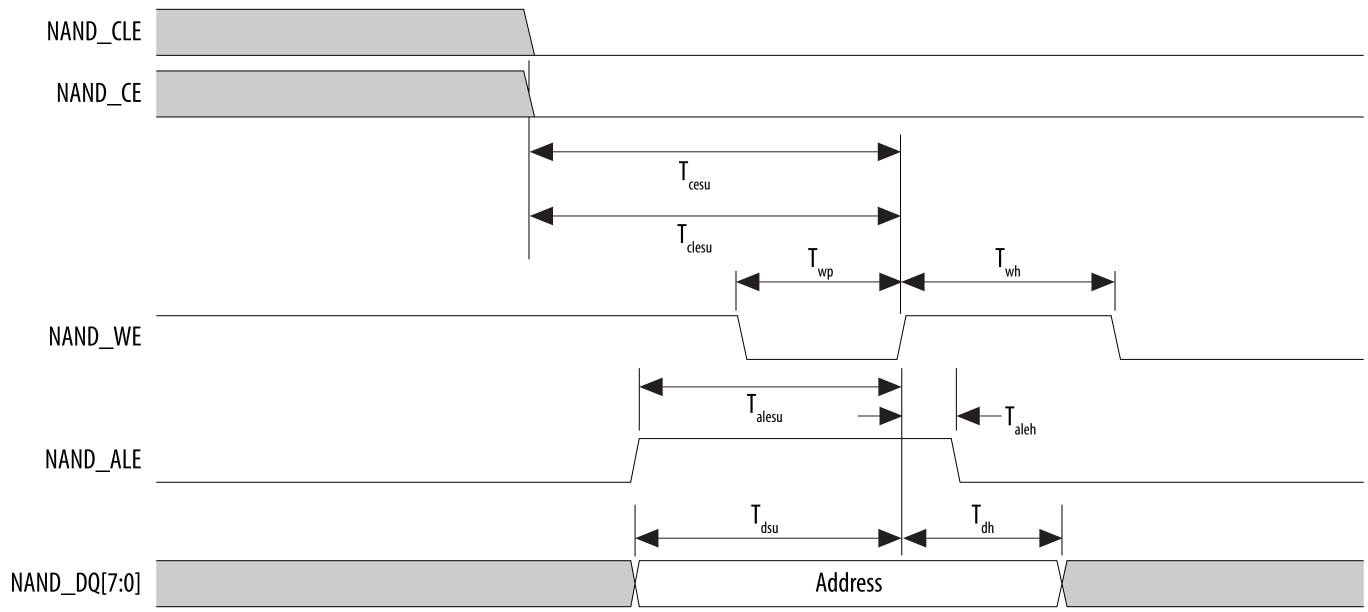
Transceiver Compliance Specification

The following table lists the physical medium attachment (PMA) specification compliance of all supported protocol for Arria V GX, GT, SX, and ST devices. For more information about the protocol parameter details and compliance specifications, contact your Altera Sales Representative.

Symbol	Condition	–I3, –C4			–I5, –C5			–C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{x\ Jitter}$ -Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate 600 Mbps – 1.25 Gbps	—	—	260	—	—	300	—	—	350	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.16	—	—	0.18	—	—	0.21	UI
$t_{x\ Jitter}$ -Emulated Differential I/O Standards with One External Output Resistor Network	—	—	—	0.15	—	—	0.15	—	—	0.15	UI
t_{DUTY}	TX output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	%
t_{RISE} and t_{FALL}	True Differential I/O Standards[82]	—	—	160	—	—	180	—	—	200	ps
	Emulated Differential I/O Standards with Three External Output Resistor Network	—	—	250	—	—	250	—	—	300	ps
	Emulated Differential I/O Standards with One External Output Resistor Network	—	—	500	—	—	500	—	—	500	ps

(82) This applies to default pre-emphasis and V_{OD} settings only.

Figure 1-18: NAND Address Latch Timing Diagram



POR Delay	Minimum	Maximum	Unit
Standard	100	300	ms

Related Information

MSEL Pin Settings

Provides more information about POR delay based on MSEL pin settings for each configuration scheme.

FPGA JTAG Configuration Timing

Table 1-64: FPGA JTAG Timing Parameters and Values for Arria V Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30, 167(92)	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	12(93)	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14(93)	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14(93)	ns

(92) The minimum TCK clock period is 167 ns if V_{CCBAT} is within the range 1.2 V – 1.5 V when you perform the volatile key programming.

(93) A 1-ns adder is required for each VCCIO voltage step down from 3.0 V. For example, tJPCO= 13 ns if VCCIO of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

The Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

Arria V I/O Timing Spreadsheet
Provides the Arria V Excel-based I/O timing spreadsheet.

Programmable IOE Delay

Table 1-76: I/O element (IOE) Programmable Delay for Arria V Devices

Parameter(112)	Available Settings	Minimum Offset(113)	Fast Model		Slow Model					Unit
			Industrial	Commercial	–C4	–C5	–C6	–I3	–I5	
D1	32	0	0.508	0.517	0.870	1.063	1.063	0.872	1.057	ns
D3	8	0	1.763	1.795	2.999	3.496	3.571	3.031	3.643	ns
D4	32	0	0.508	0.518	0.869	1.063	1.063	1.063	1.057	ns
D5	32	0	0.508	0.517	0.870	1.063	1.063	0.872	1.057	ns

Programmable Output Buffer Delay

Table 1-77: Programmable Output Buffer Delay for Arria V Devices

This table lists the delay chain settings that control the rising and falling edge delays of the output buffer.

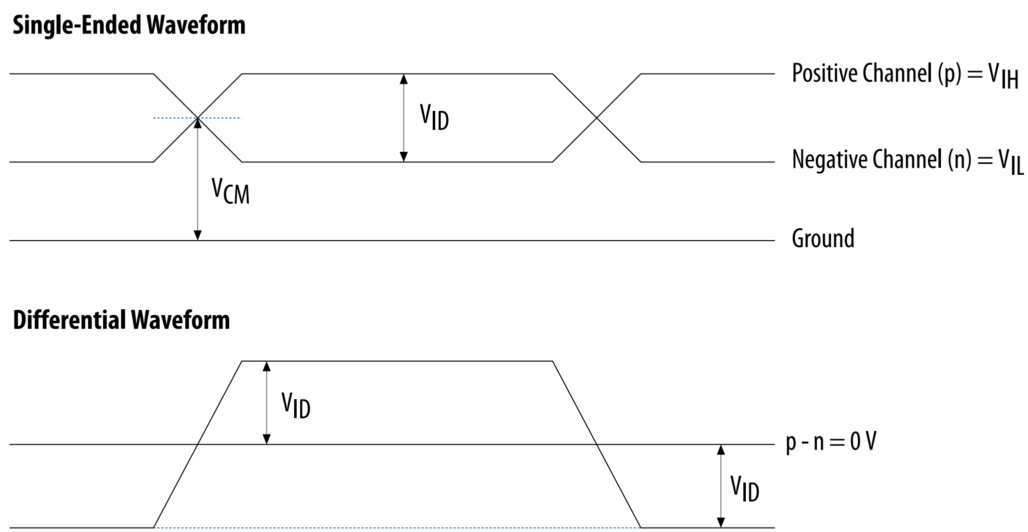
You can set the programmable output buffer delay in the Quartus Prime software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

(112) You can set this value in the Quartus Prime software by selecting **D1**, **D3**, **D4**, and **D5** in the **Assignment Name** column of **Assignment Editor**.
(113) Minimum offset does not include the intrinsic delay.

Symbol	Parameter	Typical	Unit
D_{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

Glossary

Table 1-78: Glossary

Term	Definition
Differential I/O standards	Receiver Input Waveforms 

Term	Definition
t_{FALL}	Signal high-to-low transition time (80–20%)
t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input
t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL
t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL
t_{RISE}	Signal low-to-high transition time (20–80%)
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w)
$V_{CM(DC)}$	DC common mode input voltage.
V_{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.
V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
$V_{IH(AC)}$	High-level AC input voltage
$V_{IH(DC)}$	High-level DC input voltage
V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{IL(AC)}$	Low-level AC input voltage
$V_{IL(DC)}$	Low-level DC input voltage
V_{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter.
V_{SWING}	Differential input voltage
V_X	Input differential cross point voltage

Date	Version	Changes

December 2015	2015.12.16	• Updated Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices table.
		  • Updated F_{clk}, $T_{dutycycle}$, and $T_{dssfrst}$ specifications.
		  • Added T_{qspi_clk}, T_{din_start}, and T_{din_end} specifications.
		  • Removed T_{dinmax} specifications.
		• Updated the minimum specification for T_{clk} to 16.67 ns and removed the maximum specification in SPI Master Timing Requirements for Arria V Devices table.
		• Updated Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices table.
		  • Updated T_{clk} to $T_{sdmmc\_clk\_out}$ symbol.
		  • Updated $T_{sdmmc\_clk\_out}$ and T_d specifications.
		  • Added T_{sdmmc_clk}, T_{su}, and T_h specifications.
		  • Removed T_{dinmax} specifications.
		• Updated the following diagrams:
		  • Quad SPI Flash Timing Diagram
		  • SD/MMC Timing Diagram
		• Updated configuration .rbf sizes for Arria V devices.
		• Changed instances of *Quartus II* to *Quartus Prime*.

Date	Version	Changes
July 2014	3.8	• Added a note in Table 3, Table 4, and Table 5: The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements. • Updated V_{CC_HPS} specification in Table 5. • Added a note in Table 19: Differential inputs are powered by V_{CCPD} which requires 2.5 V. • Updated "Minimum differential eye opening at the receiver serial input pins" specification in Table 20 and Table 21. • Updated description in “HPS PLL Specifications” section. • Updated VCO range maximum specification in Table 39. • Updated T_d and T_h specifications in Table 45. • Added T_h specification in Table 47 and Figure 13. • Updated a note in Figure 20, Figure 21, and Figure 23 as follows: Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required. • Removed “Remote update only in AS mode” specification in Table 58. • Added DCLK device initialization clock source specification in Table 60. • Added description in “Configuration Files” section: The IOCSR `.rbf` size is specifically for the Configuration via Protocol (CvP) feature. • Removed $f_{MAX\_RU\_CLK}$ specification in Table 63.
February 2014	3.7	• Updated $V_{CCRSTCLK\_HPS}$ maximum specification in Table 1. • Added $V_{CC\_AUX\_SHARED}$ specification in Table 1.
December 2013	3.6	• Added “HPS PLL Specifications”. • Added Table 24, Table 39, and Table 40. • Updated Table 1, Table 3, Table 5, Table 19, Table 20, Table 21, Table 38, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, Table 51, Table 55, Table 56, and Table 59. • Updated Figure 7, Figure 13, Figure 15, Figure 16, and Figure 19. • Removed table: GPIO Pulse Width for Arria V Devices.

Date	Version	Changes

November 2012	3.0	• Updated Table 2, Table 4, Table 9, Table 14, Table 16, Table 17, Table 20, Table 21, Table 25, Table 29, Table 36, Table 56, Table 57, and Table 60.
		• Removed table: Transceiver Block Jitter Specifications for Arria V Devices.
		• Added HPS information:
		  • Added "HPS Specifications" section.
		  • Added Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, and Table 50.
		  • Added Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19.
		  • Updated Table 3 and Table 5.

October 2012	2.4	• Updated Arria V GX $V_{CCR\_GXBL/R}$, $V_{CCT\_GXBL/R}$, and $V_{CCL\_GXBL/R}$ minimum and maximum values, and data rate in Table 4. • Added receiver V_{ICM} (AC coupled) and V_{ICM} (DC coupled) values, and transmitter V_{OCM} (AC coupled) and V_{OCM} (DC coupled) values in Table 20 and Table 21.
August 2012	2.3	Updated the SERDES factor condition in Table 30.
July 2012	2.2	• Updated the maximum voltage for V_I (DC input voltage) in Table 1. • Updated Table 20 to include the Arria V GX -I3 speed grade. • Updated the minimum value of the fixedclk clock frequency in Table 20 and Table 21. • Updated the SERDES factor condition in Table 30. • Updated Table 50 to include the IOE programmable delay settings for the Arria V GX -I3 speed grade.
June 2012	2.1	Updated $V_{CCR\_GXBL/R}$, $V_{CCT\_GXBL/R}$, and $V_{CCL\_GXBL/R}$ values in Table 4.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{ICM} (AC and DC coupled)	V_{CCR_GXB} = 0.85 V full bandwidth	—	600	—	—	600	—	mV
	V_{CCR_GXB} = 0.85 V half bandwidth	—	600	—	—	600	—	mV
	V_{CCR_GXB} = 1.0 V full bandwidth	—	700	—	—	700	—	mV
	V_{CCR_GXB} = 1.0 V half bandwidth	—	700	—	—	700	—	mV
t_{LTR} (149)	—	—	—	10	—	—	10	µs
t_{LTD} (150)	—	4	—	—	4	—	—	µs
t_{LTD_manual} (151)	—	4	—	—	4	—	—	µs
$t_{LTR\_LTD\_manual}$ (152)	—	15	—	—	15	—	—	µs
Programmable equalization (AC Gain)	Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz)	—	—	16	—	—	16	dB

(149) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
(150) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.
(151) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.
(152) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

Symbol	Parameter	Min	Typ	Max	Unit
t_{OUTPJ_IO}, [173], [175]	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
t_{FOUTPJ_IO} [173], [175], [176]	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
t_{OUTCCJ_IO} [173], [175]	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{FOUTCCJ\_IO}$ [173], [175], [176]	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{CASC\_OUTPJ\_DC}$ [173], [177]	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period Jitter for a dedicated clock output in cascaded PLLS ($f_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits

(175) The external memory interface clock output jitter specifications use a different measurement method, which is available in the "Memory Output Clock Jitter Specification for Arria V GZ Devices" table.

(176) This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05–0.95 must be ≥ 1000 MHz.

(177) The cascaded PLL specification is only applicable with the following condition:
a. Upstream PLL: 0.59Mhz ≤ Upstream PLL BW < 1 MHz
b. Downstream PLL: Downstream PLL BW > 2 MHz

Mode	Performance			Unit
	C3, I3L	C4	I4	
One sum of two 27 × 27	380	300	290	MHz
One sum of two 36 × 18	380	300		MHz
One complex 18 × 18	400	350		MHz
One 36 × 36	380	300		MHz
Modes using Three DSP Blocks				
One complex 18 × 25	340	275	265	MHz
Modes using Four DSP Blocks				
One complex 27 × 27	350	310		MHz

Memory Block Specifications

Table 2-36: Memory Block Performance Specifications for Arria V GZ Devices

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.

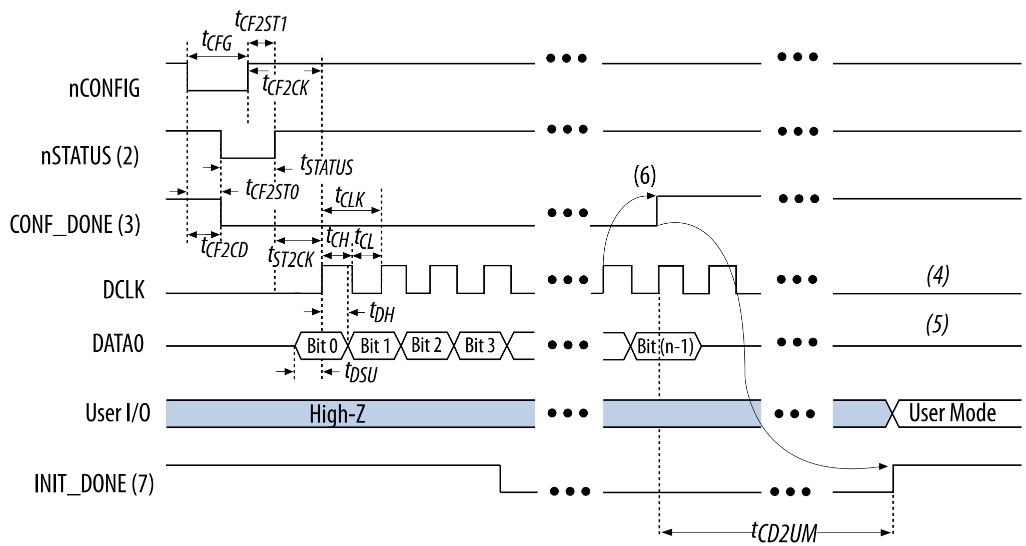
Memory	Mode	Resources Used		Performance				Unit
		ALUTs	Memory	C3	C4	I3L	I4	
MLAB	Single port, all supported widths	0	1	400	315	400	315	MHz
	Simple dual-port, x32/x64 depth	0	1	400	315	400	315	MHz
	Simple dual-port, x16 depth [178]	0	1	533	400	533	400	MHz
	ROM, all supported widths	0	1	500	450	500	450	MHz

(178) The F_{MAX} specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

Passive Serial Configuration Timing

Figure 2-10: PS Configuration Timing Waveform

Timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.



Notes:

1. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
2. After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.
3. After power-up, before and during configuration, CONF_DONE is low.
4. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
5. DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the Device and Pins Option.
6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
7. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.