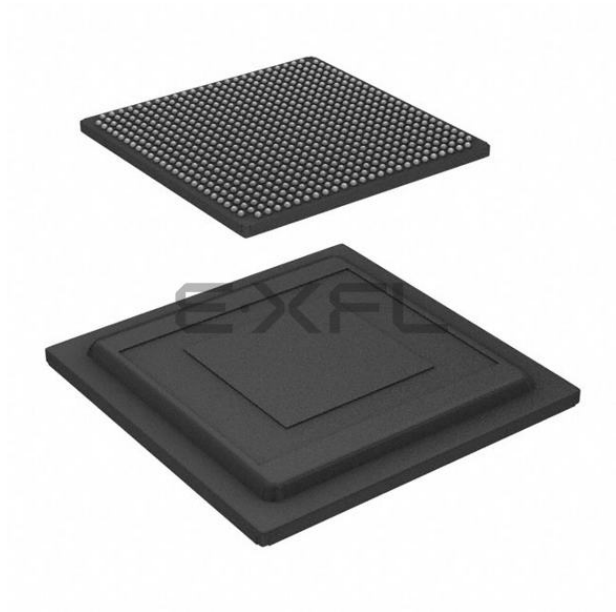
# Intel - 5AGXMA3D4F27C4G Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 7362 |
| Number of Logic Elements/Cells | 156000 |
| Total RAM Bits | 11746304 |
| Number of I/O | 336 |
| Number of Gates | - |
| Voltage - Supply | 1.07V ~ 1.13V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 672-BBGA, FCBGA |
| Supplier Device Package | 672-FBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5agxma3d4f27c4g |

| Symbol | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $V_{CCPLL\_HPS}$ | HPS PLL analog power supply | –0.50 | 3.25 | V |
| $V_{CC\_AUX\_SHARED}$ | HPS auxiliary power supply | –0.50 | 3.25 | V |
| $I_{OUT}$ | DC output current per pin | –25 | 40 | mA |
| $T_J$ | Operating junction temperature | –55 | 125 | °C |
| $T_{STG}$ | Storage temperature (no bias) | –65 | 150 | °C |

## Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 4.00 V can only be at 4.00 V for ~15% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 1.5 years.

### Table 1-2: Maximum Allowed Overshoot During Transitions for Arria V Devices

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

| Symbol | Description | Condition (V) | Calibration Accuracy | | | Unit |
|---|---|---|---|---|---|---|
| | | | –I3, –C4 | –I5, –C5 | –C6 | |
| 60-Ω and 120-Ω $R_T$ | Internal parallel termination with calibration (60-Ω and 120-Ω setting) | $V_{CCIO}$ = 1.2 | –10 to +40 | –10 to +40 | –10 to +40 | % |
| 25-Ω $R_{S\_left\_shift}$ | Internal left shift series termination with calibration (25-Ω $R_{S\_left\_shift}$ setting) | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 | ±15 | ±15 | ±15 | % |

## OCT Without Calibration Resistance Tolerance Specifications

### Table 1-9: OCT Without Calibration Resistance Tolerance Specifications for Arria V Devices

This table lists the Arria V OCT without calibration resistance tolerance to PVT changes.

| Symbol | Description | Condition (V) | ResistanceTolerance | | | Unit |
|---|---|---|---|---|---|---|
| | | | –I3, –C4 | –I5, –C5 | –C6 | |
| 25-Ω $R_S$ | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 3.0, 2.5 | ±30 | ±40 | ±40 | % |
| 25-Ω $R_S$ | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 1.8, 1.5 | ±30 | ±40 | ±40 | % |
| 25-Ω $R_S$ | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 1.2 | ±35 | ±50 | ±50 | % |
| 50-Ω $R_S$ | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 3.0, 2.5 | ±30 | ±40 | ±40 | % |
| 50-Ω $R_S$ | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.8, 1.5 | ±30 | ±40 | ±40 | % |
| 50-Ω $R_S$ | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.2 | ±35 | ±50 | ±50 | % |
| 100-Ω $R_D$ | Internal differential termination (100-Ω setting) | $V_{CCIO}$ = 2.5 | ±25 | ±40 | ±40 | % |

**Figure 1-1: Equation for OCT Variation Without Recalibration**

$$R_{OCT} = R_{SCAL}\left(1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle\right)$$

The definitions for the equation are as follows:

- The $R_{OCT}$ value calculated shows the range of OCT resistance with the variation of temperature and $V_{CCIO}$.
- $R_{SCAL}$ is the OCT resistance value at power-up.
- $\Delta T$ is the variation of temperature with respect to the temperature at power up.
- $\Delta V$ is the variation of voltage with respect to the $V_{CCIO}$ at power up.
- dR/dT is the percentage change of $R_{SCAL}$ with temperature.
- dR/dV is the percentage change of $R_{SCAL}$ with voltage.

## OCT Variation after Power-Up Calibration

**Table 1-10: OCT Variation after Power-Up Calibration for Arria V Devices**

This table lists OCT variation with temperature and voltage after power-up calibration. The OCT variation is valid for a $V_{CCIO}$ range of ±5% and a temperature range of 0°C to 85°C.

| Symbol | Description | $V_{CCIO}$ (V) | Value | Unit |
|---|---|---|---|---|
| dR/dV | OCT variation with voltage without recalibration | 3.0 | 0.100 | %/mV |
| | | 2.5 | 0.100 | |
| | | 1.8 | 0.100 | |
| | | 1.5 | 0.100 | |
| | | 1.35 | 0.150 | |
| | | 1.25 | 0.150 | |
| | | 1.2 | 0.150 | |

- **Transceiver Specifications for Arria V GT and ST Devices** on page 1-29
  Provides the specifications for transmitter, receiver, and reference clock I/O pin.

# Switching Characteristics

This section provides performance characteristics of Arria V core and periphery blocks.

## Transceiver Performance Specifications

### Transceiver Specifications for Arria V GX and SX Devices

**Table 1-20: Reference Clock Specifications for Arria V GX and SX Devices**

| Symbol/Description | Condition | Transceiver Speed Grade 4 | | | Transceiver Speed Grade 6 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supported I/O standards | 1.2 V PCML, 1.4 V PCML,1.5 V PCML, 2.5 V PCML, Differential LVPECL[23], HCSL, and LVDS | | | | | | | |
| Input frequency from REFCLK input pins | — | 27 | — | 710 | 27 | — | 710 | MHz |
| Rise time | Measure at ±60 mV of differential signal[24] | — | — | 400 | — | — | 400 | ps |
| Fall time | Measure at ±60 mV of differential signal[24] | — | — | 400 | — | — | 400 | ps |
| Duty cycle | — | 45 | — | 55 | 45 | — | 55 | % |
| Peak-to-peak differential input voltage | — | 200 | — | 300[25]/ 2000 | 200 | — | 300[25]/ 2000 | mV |

(23) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.
(24) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
(25) The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

| Symbol | $V_{OD}$ Setting[58] | $V_{OD}$ Value (mV) | $V_{OD}$ Setting[58] | $V_{OD}$ Value (mV) |
|---|---|---|---|---|
| | 25 | 500 | 53 | 1060 |
| | 26 | 520 | 54 | 1080 |
| | 27 | 540 | 55 | 1100 |
| | 28 | 560 | 56 | 1120 |
| | 29 | 580 | 57 | 1140 |
| | 30 | 600 | 58 | 1160 |
| | 31 | 620 | 59 | 1180 |
| | 32 | 640 | 60 | 1200 |
| | 33 | 660 | | |

## Transmitter Pre-Emphasis Levels

The following table lists the simulation data on the transmitter pre-emphasis levels in dB for the first post tap under the following conditions:

- Low-frequency data pattern—five 1s and five 0s
- Data rate—2.5 Gbps

The levels listed are a representation of possible pre-emphasis levels under the specified conditions only and the pre-emphasis levels may change with data pattern and data rate.

Arria V devices only support 1st post tap pre-emphasis with the following conditions:

- The 1st post tap pre-emphasis settings must satisfy $|B| + |C| \leq 60$ where $|B| = V_{OD}$ setting with termination value, $R_{TERM} = 100\ \Omega$ and $|C|$ = 1st post tap pre-emphasis setting.
- $|B| - |C| > 5$ for data rates < 5 Gbps and $|B| - |C| > 8.25$ for data rates > 5 Gbps.
- $(V_{MAX}/V_{MIN} - 1)\% < 600\%$, where $V_{MAX} = |B| + |C|$ and $V_{MIN} = |B| - |C|$.

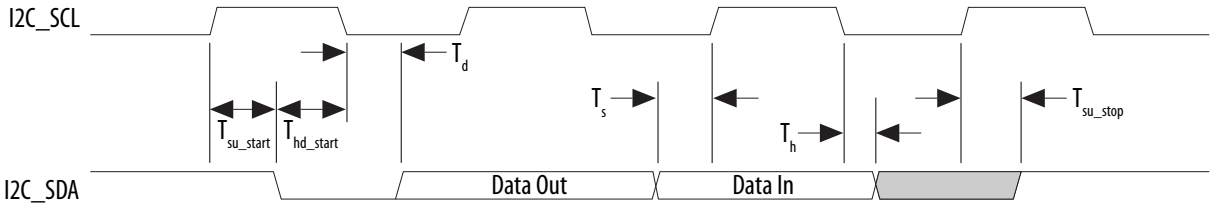
Exception for PCIe Gen2 design: $V_{OD}$ setting = 43 and pre-emphasis setting = 19 are allowed for PCIe Gen2 design with transmit de-emphasis – 6dB setting (`pipe_txdeemp` = 1'b0) using Altera PCIe Hard IP and PIPE IP cores.

[58] Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

| Symbol | Condition | –I3, –C4 | | | –I5, –C5 | | | –C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | SERDES factor J ≥ 8[76][78], LVDS TX with RX DPA | [77] | — | 1600 | [77] | — | 1500 | [77] | — | 1250 | Mbps |
| | SERDES factor J = 1 to 2, Uses DDR Registers | [77] | — | [79] | [77] | — | [79] | [77] | — | [79] | Mbps |
| Emulated Differential I/O Standards with Three External Output Resistor Network - $f_{HSDR}$ (data rate)[80] | SERDES factor J = 4 to 10[81] | [77] | — | 945 | [77] | — | 945 | [77] | — | 945 | Mbps |
| Emulated Differential I/O Standards with One External Output Resistor Network - $f_{HSDR}$ (data rate)[80] | SERDES factor J = 4 to 10[81] | [77] | — | 200 | [77] | — | 200 | [77] | — | 200 | Mbps |
| $t_{x\ Jitter}$ -True Differential I/O Standards | Total Jitter for Data Rate 600 Mbps – 1.25 Gbps | — | — | 160 | — | — | 160 | — | — | 160 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | UI |

(78) The $V_{CC}$ and $V_{CCP}$ must be on a separate power layer and a maximum load of 5 pF for chip-to-chip interface.
(79) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency ($f_{OUT}$), provided you can close the design timing and the signal integrity simulation is clean.
(80) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.
(81) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

**Figure 1-16: I²C Timing Diagram**




## NAND Timing Characteristics

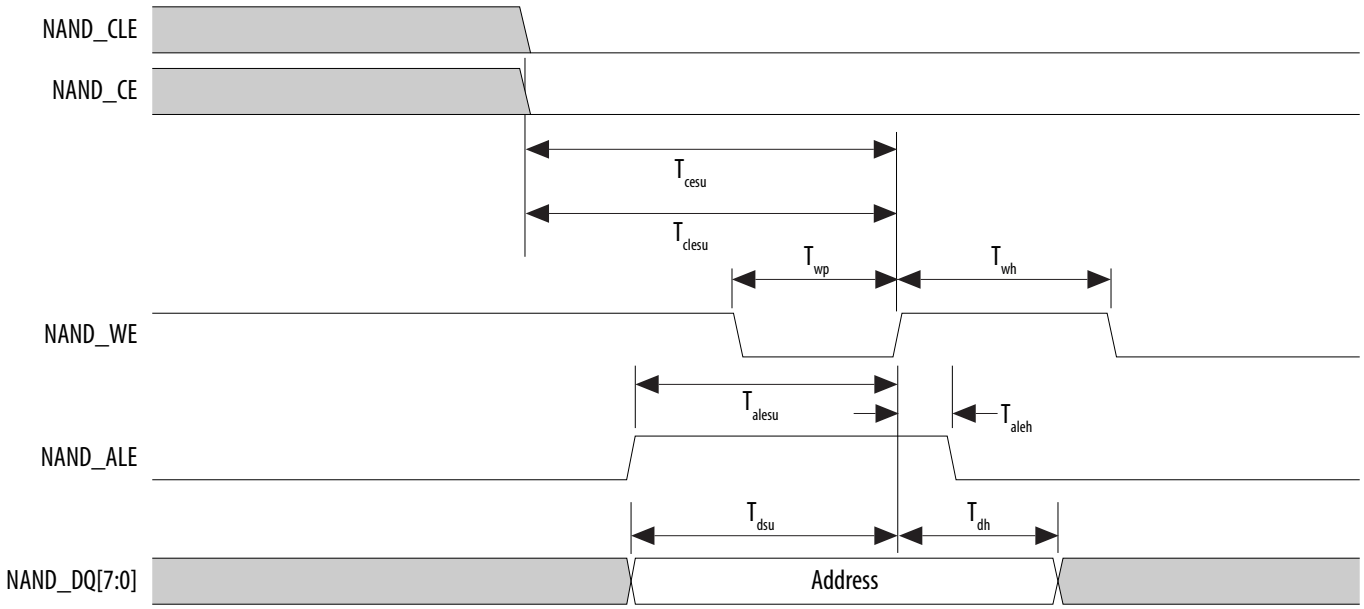
**Table 1-60: NAND ONFI 1.0 Timing Requirements for Arria V Devices**

The NAND controller supports Open NAND FLASH Interface (ONFI) 1.0 Mode 5 timing as well as legacy NAND devices. This table lists the requirements for ONFI 1.0 mode 5 timing. The HPS NAND controller can meet this timing by programming the C4 output of the main HPS PLL and timing registers provided in the NAND controller.

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $T_{wp}$ (89) | Write enable pulse width | 10 | — | ns |
| $T_{wh}$ (89) | Write enable hold time | 7 | — | ns |
| $T_{rp}$ (89) | Read enable pulse width | 10 | — | ns |
| $T_{reh}$ (89) | Read enable hold time | 7 | — | ns |
| $T_{clesu}$ (89) | Command latch enable to write enable setup time | 10 | — | ns |
| $T_{cleh}$ (89) | Command latch enable to write enable hold time | 5 | — | ns |
| $T_{cesu}$ (89) | Chip enable to write enable setup time | 15 | — | ns |
| $T_{ceh}$ (89) | Chip enable to write enable hold time | 5 | — | ns |
| $T_{alesu}$ (89) | Address latch enable to write enable setup time | 10 | — | ns |
| $T_{aleh}$ (89) | Address latch enable to write enable hold time | 5 | — | ns |
| $T_{dsu}$ (89) | Data to write enable setup time | 10 | — | ns |

(89) Timing of the NAND interface is controlled through the NAND configuration registers.

**Figure 1-18: NAND Address Latch Timing Diagram**



| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 1506(94) | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 1506(95) | µs |
| $t_{CF2CK}$(96) | nCONFIG high to first rising edge on DCLK | 1506 | — | µs |
| $t_{ST2CK}$(96) | nSTATUS high to first rising edge of DCLK | 2 | — | µs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | 0 | — | ns |
| $t_{CH}$ | DCLK high time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | $1/f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency (FPP ×8/ ×16) | — | 125 | MHz |
| $t_{CD2UM}$ | CONF_DONE high to user mode(97) | 175 | 437 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4× maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + ($T_{init}$ × CLKUSR period) | — | — |
| $T_{init}$ | Number of clock cycles required for device initialization | 8,576 | — | Cycles |

**Related Information**

**FPP Configuration Timing**

Provides the FPP configuration timing waveforms.

(94) You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.
(95) You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.
(96) If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.
(97) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

| Variant | Member Code | Active Serial[108] | | | Fast Passive Parallel[109] | | |
|---|---|---|---|---|---|---|---|
| | | Width | DCLK (MHz) | Minimum Configuration Time (ms) | Width | DCLK (MHz) | Minimum Configuration Time (ms) |
| Arria V GX | A1 | 4 | 100 | 178 | 16 | 125 | 36 |
| | A3 | 4 | 100 | 178 | 16 | 125 | 36 |
| | A5 | 4 | 100 | 255 | 16 | 125 | 51 |
| | A7 | 4 | 100 | 255 | 16 | 125 | 51 |
| | B1 | 4 | 100 | 344 | 16 | 125 | 69 |
| | B3 | 4 | 100 | 344 | 16 | 125 | 69 |
| | B5 | 4 | 100 | 465 | 16 | 125 | 93 |
| | B7 | 4 | 100 | 465 | 16 | 125 | 93 |
| Arria V GT | C3 | 4 | 100 | 178 | 16 | 125 | 36 |
| | C7 | 4 | 100 | 255 | 16 | 125 | 51 |
| | D3 | 4 | 100 | 344 | 16 | 125 | 69 |
| | D7 | 4 | 100 | 465 | 16 | 125 | 93 |
| Arria V SX | B3 | 4 | 100 | 465 | 16 | 125 | 93 |
| | B5 | 4 | 100 | 465 | 16 | 125 | 93 |
| Arria V ST | D3 | 4 | 100 | 465 | 16 | 125 | 93 |
| | D5 | 4 | 100 | 465 | 16 | 125 | 93 |

**Related Information**

**Configuration Files** on page 1-83

(108) DCLK frequency of 100 MHz using external CLKUSR.

(109) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

| Date | Version | Changes |
|---|---|---|
| August 2013 | 3.5 | • Removed "Pending silicon characterization" note in Table 29.<br>• Updated Table 25. |
| August 2013 | 3.4 | • Removed Preliminary tags for Table 1, Table 2, Table 3, Table 4, Table 5, Table 6, Table 7, Table 9, Table 12, Table 13, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, Table 21, Table 22, Table 23, Table 24, Table 25, Table 26, Table 27, Table 28, Table 29, Table 30, Table 31, Table 35, Table 36, Table 51, Table 53, Table 54, Table 55, Table 56, Table 57, Table 60, Table 62, and Table 64.<br>• Updated Table 1, Table 3, Table 11, Table 19, Table 20, Table 21, Table 22, Table 25, and Table 29. |
| June 2013 | 3.3 | Updated Table 20, Table 21, Table 25, and Table 38. |
| May 2013 | 3.2 | • Added Table 37.<br>• Updated Figure 8, Figure 9, Figure 20, Figure 22, and Figure 23.<br>• Updated Table 1, Table 5, Table 10, Table 13, Table 19, Table 20, Table 21, Table 23, Table 29, Table 39, Table 40, Table 46, Table 56, Table 57, Table 60, and Table 64.<br>• Updated industrial junction temperature range for –I3 speed grade in "PLL Specifications" section. |
| March 2013 | 3.1 | • Added HPS reset information in the "HPS Specifications" section.<br>• Added Table 60.<br>• Updated Table 1, Table 3, Table 17, Table 20, Table 29, and Table 59.<br>• Updated Figure 21. |

| Date | Version | Changes |
|---|---|---|
| June 2012 | 2.0 | • Updated for the Quartus II software v12.0 release:<br>• Restructured document.<br>• Updated "Supply Current and Power Consumption" section.<br>• Updated Table 20, Table 21, Table 24, Table 25, Table 26, Table 35, Table 39, Table 43, and Table 52.<br>• Added Table 22, Table 23, and Table 33.<br>• Added Figure 1–1 and Figure 1–2.<br>• Added "Initialization" and "Configuration Files" sections. |
| February 2012 | 1.3 | • Updated Table 2–1.<br>• Updated Transceiver-FPGA Fabric Interface rows in Table 2–20.<br>• Updated $V_{CCP}$ description. |
| December 2011 | 1.2 | Updated Table 2–1 and Table 2–3. |
| November 2011 | 1.1 | • Updated Table 2–1, Table 2–19, Table 2–26, and Table 2–36.<br>• Added Table 2–5.<br>• Added Figure 2–4. |
| August 2011 | 1.0 | Initial release. |

# Arria V GZ Device Datasheet

2

2017.02.10

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This document covers the electrical and switching characteristics for Arria V GZ devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, core, and periphery performance. This document also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

**Related Information**

**Arria V Device Overview**
For information regarding the densities and packages of devices in the Arria V GZ family.

## Electrical Characteristics

### Operating Conditions

When you use Arria V GZ devices, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Arria V GZ devices, you must consider the operating requirements described in this datasheet.

Arria V GZ devices are offered in commercial and industrial temperature grades.

Commercial devices are offered in –3 (fastest) and –4 core speed grades. Industrial devices are offered in –3L and –4 core speed grades. Arria V GZ devices are offered in –2 and –3 transceiver speed grades.

**Table 2-1: Commercial and Industrial Speed Grade Offering for Arria V GZ Devices**

C = Commercial temperature grade; I = Industrial temperature grade.

| Symbol | Description | Conditions | Resistance Tolerance | | Unit |
|---|---|---|---|---|---|
| | | | C3, I3L | C4, I4 | |
| 25-Ω $R_S$ | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 1.8 and 1.5 V | ±40 | ±40 | % |
| 25-Ω $R_S$ | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 1.2 V | ±50 | ±50 | % |
| 50-Ω $R_S$ | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.8 and 1.5 V | ±40 | ±40 | % |
| 50-Ω $R_S$ | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.2 V | ±50 | ±50 | % |
| 100-Ω $R_D$ | Internal differential termination (100-Ω setting) | $V_{CCIO}$ = 2.5 V | ±25 | ±25 | % |

**Figure 2-1: OCT Variation Without Re-Calibration for Arria V GZ Devices**

$$R_{OCT} = R_{SCAL}\left(1 + \left(\frac{dR}{dT} \times \triangle T\right) \pm \left(\frac{dR}{dV} \times \triangle V\right)\right)$$

Notes:
1. The $R_{OCT}$ value shows the range of OCT resistance with the variation of temperature and $V_{CCIO}$.
2. $R_{SCAL}$ is the OCT resistance value at power-up.
3. ΔT is the variation of temperature with respect to the temperature at power-up.
4. ΔV is the variation of voltage with respect to the $V_{CCIO}$ at power-up.
5. dR/dT is the percentage change of $R_{SCAL}$ with temperature.
6. dR/dV is the percentage change of $R_{SCAL}$ with voltage.

**Table 2-12: OCT Variation after Power-Up Calibration for Arria V GZ Devices**

Valid for a $V_{CCIO}$ range of ±5% and a temperature range of 0° to 85°C.

| I/O Standard | $V_{CCIO}$ (V) [128] | | | $V_{ID}$ (mV) [129] | | | $V_{ICM(DC)}$ (V) | | | $V_{OD}$ (V) [130] | | | $V_{OCM}$ (V) [130] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Condition | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| RSDS (HIO) [133] | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.3 | — | 1.4 | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.4 |
| Mini-LVDS (HIO) [134] | 2.375 | 2.5 | 2.625 | 200 | — | 600 | 0.4 | — | 1.325 | 0.25 | — | 0.6 | 1 | 1.2 | 1.4 |
| LVPECL [135], [136] | — | — | — | 300 | — | — | 0.6 | $D_{MAX} \leq$ 700 Mbps | 1.8 | — | — | — | — | — | — |
| | — | — | — | 300 | — | — | 1 | $D_{MAX} >$ 700 Mbps | 1.6 | — | — | — | — | — | — |

**Related Information**

**Glossary** on page 2-73

[128] Differential inputs are powered by VCCPD which requires 2.5 V.
[129] The minimum VID value is applicable over the entire common mode range, VCM.
[130] RL range: 90 ≤ RL ≤ 110 Ω.
[133] For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.
[134] For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.
[135] LVPECL is only supported on dedicated clock input pins.
[136] For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Differential on-chip termination resistors | 85-Ω setting | — | 85 ± 20% | — | — | 85 ± 20% | — | Ω |
| | 100-Ω setting | — | 100 ± 20% | — | — | 100 ± 20% | — | Ω |
| | 120-Ω setting | — | 120 ± 20% | — | — | 120 ± 20% | — | Ω |
| | 150-Ω setting | — | 150 ± 20% | — | — | 150 ± 20% | — | Ω |
| $V_{OCM}$ (AC coupled) | 0.65-V setting | — | 650 | — | — | 650 | — | mV |
| $V_{OCM}$ (DC coupled) | — | — | 650 | — | — | 650 | — | mV |
| Intra-differential pair skew | Tx $V_{CM}$ = 0.5 V and slew rate of 15 ps | — | — | 15 | — | — | 15 | ps |
| Intra-transceiver block transmitter channel-to-channel skew | x6 PMA bonded mode | — | — | 120 | — | — | 120 | ps |
| Inter-transceiver block transmitter channel-to-channel skew | xN PMA bonded mode | — | — | 500 | — | — | 500 | ps |

**Related Information**

**Arria V Device Overview**

For more information about device ordering codes.

| Mode [164] | Transceiver Speed Grade | PMA Width | 20 | 20 | 16 | 16 | 10 | 10 | 8 | 8 |
|---|---|---|---|---|---|---|---|---|---|---|
| | | PCS/Core Width | 40 | 20 | 32 | 16 | 20 | 10 | 16 | 8 |
| Register | 2 | C3, I3L core speed grade | 9.9 | 9 | 7.92 | 7.2 | 4.9 | 4.,5 | 3.92 | 3.6 |
| | 3 | C4, I4 core speed grade | 8.8 | 8.2 | 7.04 | 6.56 | 4.4 | 4.1 | 3.52 | 3.28 |

**Related Information**

**Operating Conditions** on page 2-1

## 10G PCS Data Rate

**Table 2-31: 10G PCS Approximate Maximum Data Rate (Gbps) for Arria V GZ Devices**

| Mode [165] | Transceiver Speed Grade | PMA Width | 64 | 40 | 40 | 40 | 32 | 32 |
|---|---|---|---|---|---|---|---|---|
| | | PCS Width | 64 | 66/67 | 50 | 40 | 64/66/67 | 32 |
| FIFO | 2 | C3, I3L core speed grade | 12.5 | 12.5 | 10.69 | 12.5 | 10.88 | 10.88 |
| | 3 | C4, I4 core speed grade | 10.3125 | 10.3125 | 10.69 | 10.3125 | 9.92 | 9.92 |
| Register | 2 | C3, I3L core speed grade | 12.5 | 12.5 | 10.69 | 12.5 | 10.88 | 10.88 |
| | 3 | C4, I4 core speed grade | 10.3125 | 10.3125 | 10.69 | 10.3125 | 9.92 | 9.92 |

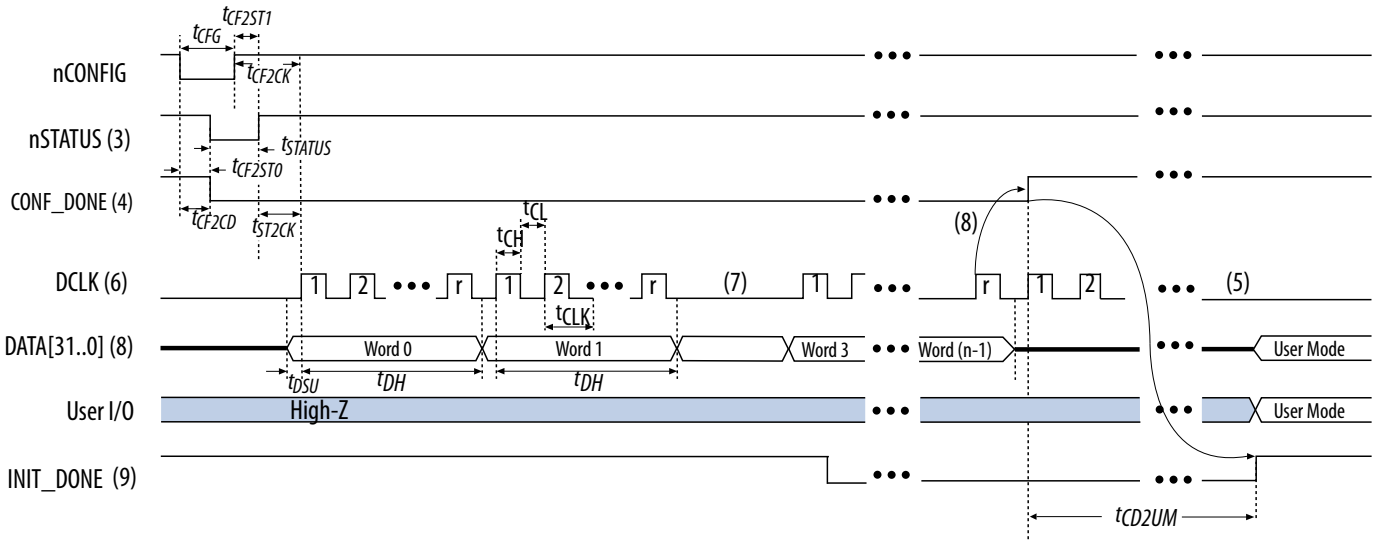
(164) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

(165) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

## FPP Configuration Timing when DCLK to DATA[] > 1

### Figure 2-8: FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 ,

Timing when using a MAX II device, MAX V device, or microprocessor as an external host.



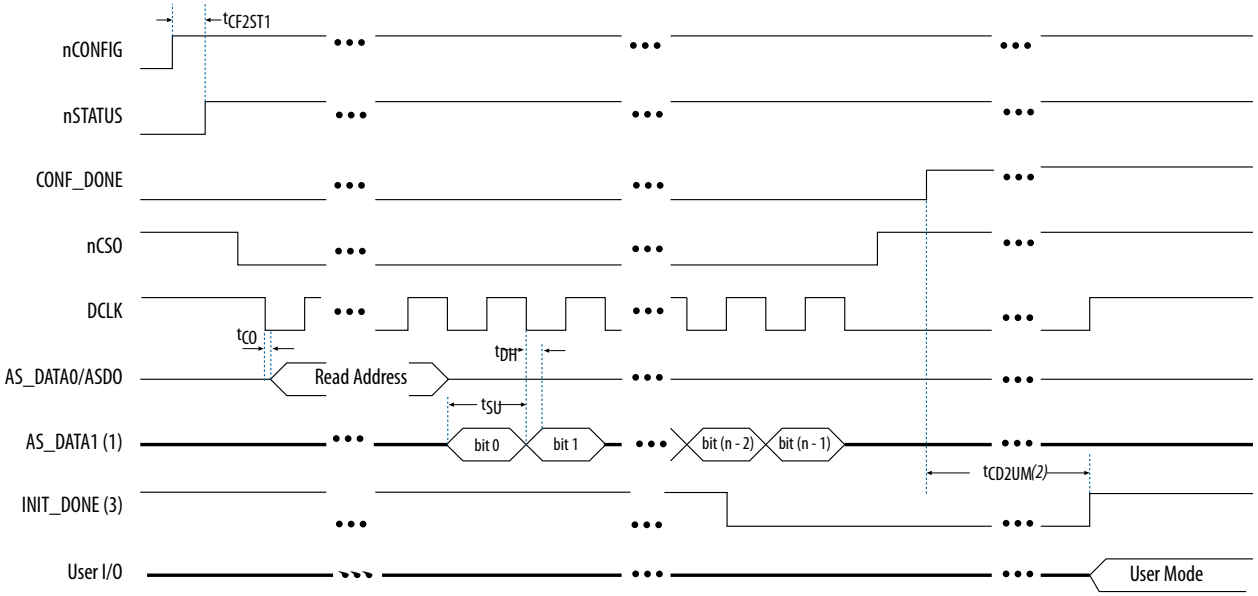

Notes:

1. To find out the DCLK-to-DATA[] ratio for your system, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
2. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
3. After power-up, the Arria V GZ device holds nSTATUS low for the time as specified by the POR delay.
4. After power-up, before and during configuration, CONF_DONE is low.
5. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
6. "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
7. If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31..0] pins prior to sending the first DCLK rising edge.
8. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
9. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

# Active Serial Configuration Timing

## Figure 2-9: AS Configuration Timing

Timing waveform for the active serial (AS) x1 mode and AS x4 mode configuration timing.

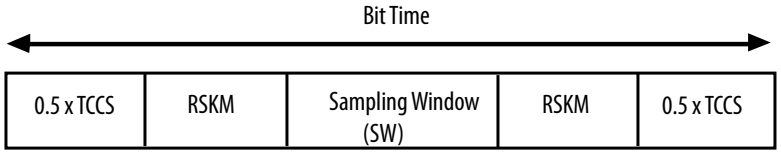
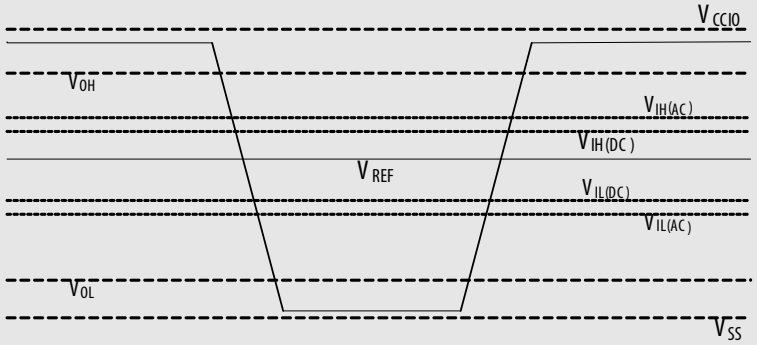



Notes:
1. If you are using AS ×4 mode, this signal represents the AS_DATA[3..0] and EPCQ sends in 4-bits of data for each DCLK cycle.
2. The initialization clock can be from internal oscillator or CLKUSR pin.
3. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

## Table 2-58: AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices

The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

$t_{CF2CD}$, $t_{CF2ST0}$, $t_{CFG}$, $t_{STATUS}$, and $t_{CF2ST1}$ timing parameters are identical to the timing parameters for PS mode listed in the "PS Timing Parameters for Arria V GZ Devices" table.

| Term | Definition |
|---|---|
| $R_L$ | Receiver differential input discrete resistor (external to the Arria V GZ device). |
| SW (sampling window) | Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:<br>  |
| Single-ended voltage referenced I/O standard | The JEDEC standard for SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.<br>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:<br>Single-Ended Voltage Referenced I/O Standard<br>  |