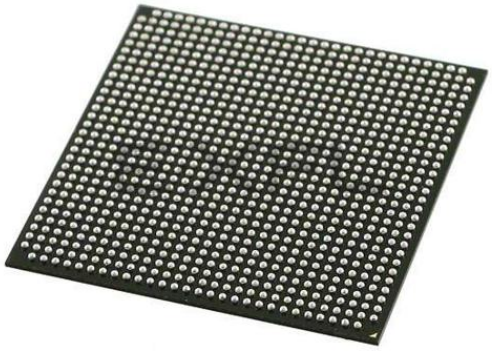

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	7362
Number of Logic Elements/Cells	156000
Total RAM Bits	11746304
Number of I/O	416
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxma3d4f31c4g

Symbol	Description	Condition	Minimum[1]	Typical	Maximum[1]	Unit
V_{CC}	Core voltage power supply	–C4, –I5, –C5, –C6	1.07	1.1	1.13	V
		–I3	1.12	1.15	1.18	V
V_{CCP}	Periphery circuitry, PCIe hard IP block, and transceiver PCS power supply	–C4, –I5, –C5, –C6	1.07	1.1	1.13	V
		–I3	1.12	1.15	1.18	V
V_{CCPGM}	Configuration pins power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
V_{CC_AUX}	Auxiliary supply	—	2.375	2.5	2.625	V
V_{CCBAT}[2]	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V
V_{CCPD}[3]	I/O pre-driver power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V

(1) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.
(2) If you do not use the design security feature in Arria V devices, connect V_{CCBAT} to a 1.5-V, 2.5-V, or 3.0-V power supply. Arria V power-on reset (POR) circuitry monitors V_{CCBAT}. Arria V devices do not exit POR if V_{CCBAT} is not powered up.
(3) V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25, or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V. V_{CCPD} must be 3.3 V when V_{CCIO} is 3.3 V.

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Spread-spectrum modulating clock frequency	PCI Express® (PCIe)	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	Ω
V_{ICM} (AC coupled)	—	—	1.1/1.15[26]	—	—	1.1/1.15[26]	—	V
V_{ICM} (DC coupled)	HCSL I/O standard for the PCIe reference clock	250	—	550	250	—	550	mV
Transmitter REFCLK phase noise[27]	10 Hz	—	—	–50	—	—	–50	dBc/Hz
	100 Hz	—	—	–80	—	—	–80	dBc/Hz
	1 KHz	—	—	–110	—	—	–110	dBc/Hz
	10 KHz	—	—	–120	—	—	–120	dBc/Hz
	100 KHz	—	—	–120	—	—	–120	dBc/Hz
	≥1 MHz	—	—	–130	—	—	–130	dBc/Hz
R_{REF}	—	—	2000 ±1%	—	—	2000 ±1%	—	Ω

(26) For data rate ≤3.2 Gbps, connect $V_{CCR\_GXBL/R}$ to either 1.1-V or 1.15-V power supply. For data rate >3.2 Gbps, connect $V_{CCR\_GXBL/R}$ to a 1.15-V power supply. For details, refer to the Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines.

(27) The transmitter REFCLK phase jitter is 30 ps p-p at bit error rate (BER) 10^{-12}.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Transmitter REFCLK phase noise(43)	10 Hz	—	—	–50	dBc/Hz
	100 Hz	—	—	–80	dBc/Hz
	1 KHz	—	—	–110	dBc/Hz
	10 KHz	—	—	–120	dBc/Hz
	100 KHz	—	—	–120	dBc/Hz
	≥ 1 MHz	—	—	–130	dBc/Hz
R_{REF}	—	—	2000 ±1%	—	Ω

Table 1-27: Transceiver Clocks Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
fixedclk clock frequency	PCIe Receiver Detect	—	125	—	MHz
Transceiver Reconfiguration Controller IP (mgmt_clk_clk) clock frequency	—	75	—	125	MHz

Table 1-28: Receiver Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS				
Data rate (6-Gbps transceiver)(44)	—	611	—	6553.6	Mbps

(43) The transmitter REFCLK phase jitter is 30 ps p-p (5 ps RMS) with bit error rate (BER) 10^{-12}, equivalent to 14 sigma.
(44) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Quartus Prime 1st Post Tap Pre-Emphasis Setting	Quartus Prime V_{OD} Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
16	—	—	9.56	7.73	6.49	—	—	dB
17	—	—	10.43	8.39	7.02	—	—	dB
18	—	—	11.23	9.03	7.52	—	—	dB
19	—	—	12.18	9.7	8.02	—	—	dB
20	—	—	13.17	10.34	8.59	—	—	dB
21	—	—	14.2	11.1	—	—	—	dB
22	—	—	15.38	11.87	—	—	—	dB
23	—	—	—	12.67	—	—	—	dB
24	—	—	—	13.48	—	—	—	dB
25	—	—	—	14.37	—	—	—	dB
26	—	—	—	—	—	—	—	dB
27	—	—	—	—	—	—	—	dB
28	—	—	—	—	—	—	—	dB
29	—	—	—	—	—	—	—	dB
30	—	—	—	—	—	—	—	dB
31	—	—	—	—	—	—	—	dB

Related Information

SPICE Models for Altera Devices
Provides the Arria V HSSI HSPICE models.

Transceiver Compliance Specification

The following table lists the physical medium attachment (PMA) specification compliance of all supported protocol for Arria V GX, GT, SX, and ST devices. For more information about the protocol parameter details and compliance specifications, contact your Altera Sales Representative.

Protocol	Sub-protocol	Data Rate (Mbps)
SONET	SONET 155	155.52
	SONET 622	622.08
	SONET 2488	2,488.32
Gigabit-capable passive optical network (GPON)	GPON 155	155.52
	GPON 622	622.08
	GPON 1244	1,244.16
	GPON 2488	2,488.32
QSGMII	QSGMII 5000	5,000

Core Performance Specifications

Clock Tree Specifications

Table 1-35: Clock Tree Specifications for Arria V Devices

Parameter	Performance			Unit
	–I3, –C4	–I5, –C5	–C6	
Global clock and Regional clock	625	625	525	MHz
Peripheral clock	450	400	350	MHz

PLL Specifications

Table 1-36: PLL Specifications for Arria V Devices

This table lists the Arria V PLL block specifications. Arria V PLL block does not include HPS PLL.

LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications

Figure 1-5: LVDS Soft-Clock Data Recovery (CDR)/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Equal to 1.25 Gbps

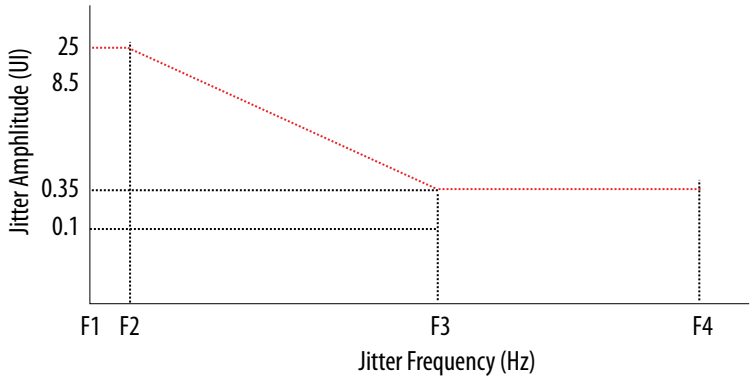
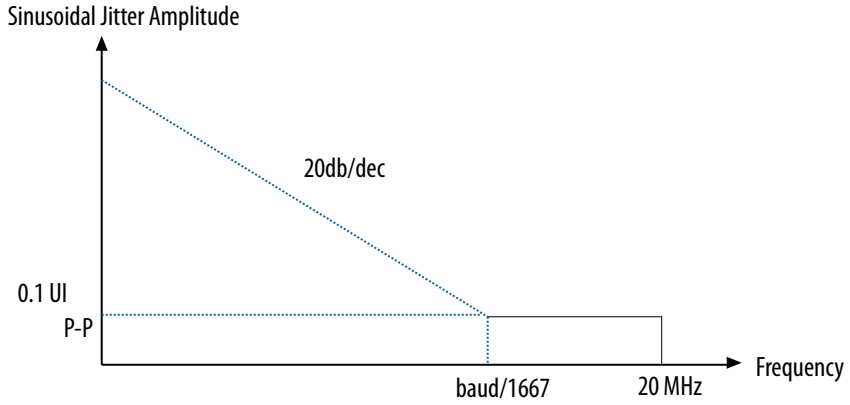


Table 1-42: LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.25 Gbps

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Figure 1-6: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Less than 1.25 Gbps



DLL Frequency Range Specifications

Table 1-43: DLL Frequency Range Specifications for Arria V Devices

Parameter	–I3, –C4	–I5, –C5	–C6	Unit
DLL operating frequency range	200 – 667	200 – 667	200 – 667	MHz

DQS Logic Block Specifications

Table 1-44: DQS Phase Shift Error Specifications for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria V Devices

This error specification is the absolute maximum and minimum error.

Number of DQS Delay Buffer	–I3, –C4	–I5, –C5	–C6	Unit
2	40	80	80	ps

HPS Clock Performance

Table 1-48: HPS Clock Performance for Arria V Devices

Symbol/Description	–I3	–C4	–C5, –I5	–C6	Unit
mpu_base_clk (microprocessor unit clock)	1050	925	800	700	MHz
main_base_clk (L3/L4 interconnect clock)	400	400	400	350	MHz
h2f_user0_clk	100	100	100	100	MHz
h2f_user1_clk	100	100	100	100	MHz
h2f_user2_clk	200	200	200	160	MHz

HPS PLL Specifications

HPS PLL VCO Frequency Range

Table 1-49: HPS PLL VCO Frequency Range for Arria V Devices

Description	Speed Grade	Minimum	Maximum	Unit
VCO range	–C5, –I5, –C6	320	1,600	MHz
	–C4	320	1,850	MHz
	–I3	320	2,100	MHz

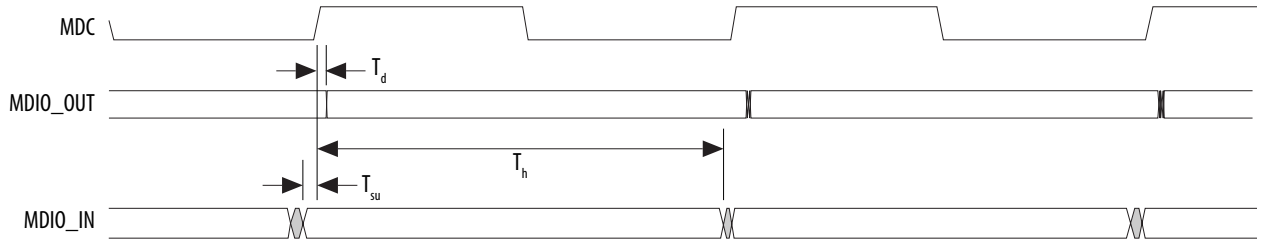
HPS PLL Input Clock Range

The HPS PLL input clock range is 10 – 50 MHz. This clock range applies to both HPS_CLK1 and HPS_CLK2 inputs.

Related Information

Clock Select, Booting and Configuration chapter
Provides more information about the clock range for different values of clock select (CSEL).

Figure 1-15: MDIO Timing Diagram



I²C Timing Characteristics

Table 1-59: I²C Timing Requirements for Arria V Devices

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T_{clk}	Serial clock (SCL) clock period	10	—	2.5	—	µs
$T_{clkhigh}$	SCL high time	4.7	—	0.6	—	µs
T_{clklow}	SCL low time	4	—	1.3	—	µs
T_s	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1	—	µs
T_h	Hold time for SCL to SDA data	0	3.45	0	0.9	µs
T_d	SCL to SDA output data delay	—	0.2	—	0.2	µs
T_{su_start}	Setup time for a repeated start condition	4.7	—	0.6	—	µs
T_{hd_start}	Hold time for a repeated start condition	4	—	0.6	—	µs
T_{su_stop}	Setup time for a stop condition	4	—	0.6	—	µs

POR Delay	Minimum	Maximum	Unit
Standard	100	300	ms

Related Information

MSEL Pin Settings
Provides more information about POR delay based on MSEL pin settings for each configuration scheme.

FPGA JTAG Configuration Timing

Table 1-64: FPGA JTAG Timing Parameters and Values for Arria V Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30, 167[92]	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	12[93]	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14[93]	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14[93]	ns

(92) The minimum TCK clock period is 167 ns if V_{CCBAT} is within the range 1.2 V – 1.5 V when you perform the volatile key programming.
(93) A 1-ns adder is required for each VCCIO voltage step down from 3.0 V. For example, tJPCO= 13 ns if VCCIO of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

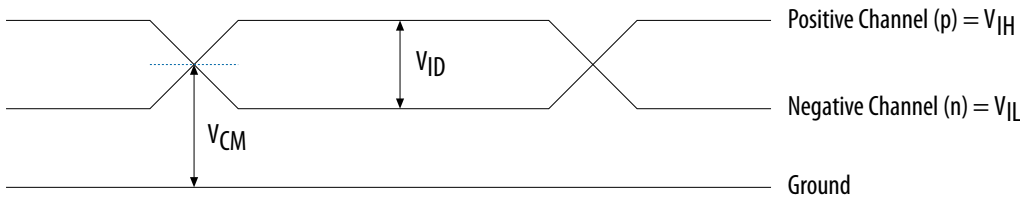
Symbol	Parameter	Typical	Unit
D_{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

Glossary

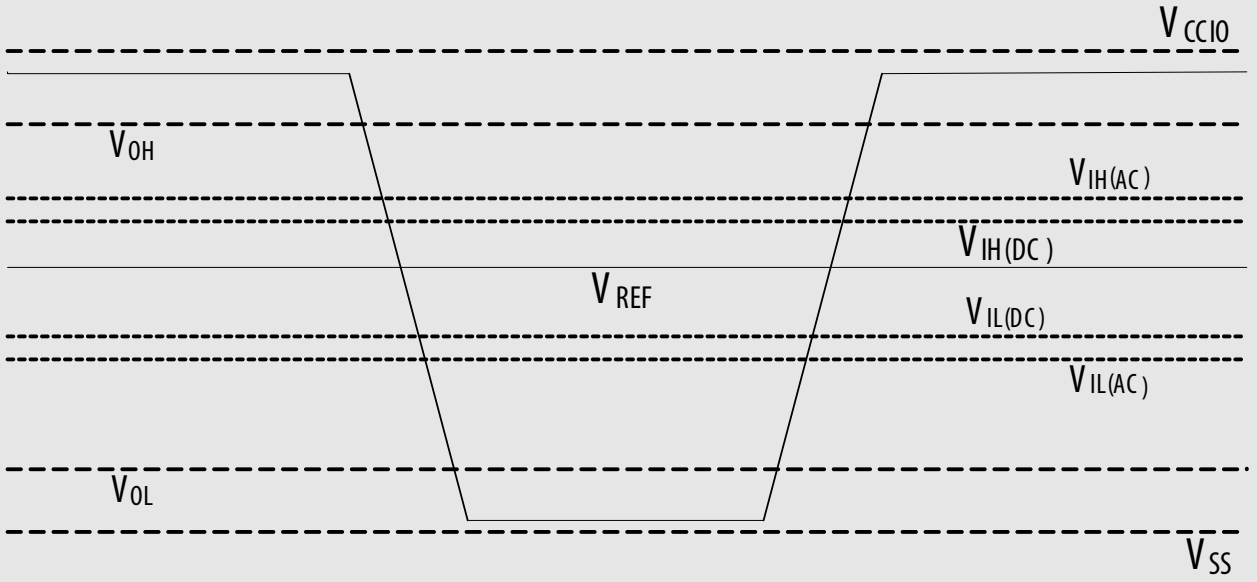
Table 1-78: Glossary

Term	Definition
Differential I/O standards	Receiver Input Waveforms

Single-Ended Waveform



Differential Waveform

Term	Definition
Single-ended voltage referenced I/O standard	The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing. Single-Ended Voltage Referenced I/O Standard 
t_C	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t_{DUTY}	High-speed I/O block—Duty cycle on high-speed transmitter output clock.

Bus Hold Specifications

Table 2-9: Bus Hold Parameters for Arria V GZ Devices

Parameter	Symbol	Conditions	V_{CCIO}										Unit
			1.2 V		1.5 V		1.8 V		2.5 V		3.0 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (maximum)	22.5	—	25.0	—	30.0	—	50.0	—	70.0	—	µA
High sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (minimum)	–22.5	—	–25.0	—	–30.0	—	–50.0	—	–70.0	—	µA
Low overdrive current	I_{ODL}	$0V < V_{IN} < V_{CCIO}$	—	120	—	160	—	200	—	300	—	500	µA
High overdrive current	I_{ODH}	$0V < V_{IN} < V_{CCIO}$	—	–120	—	–160	—	–200	—	–300	—	–500	µA
Bus-hold trip point	V_{TRIP}	—	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block.

Table 2-10: OCT Calibration Accuracy Specifications for Arria V GZ Devices

OCT calibration accuracy is valid at the time of calibration only.

Symbol	Description	V_{CCIO} (V)	Typical	Unit
dR/dV	OCT variation with voltage without re-calibration	3.0	0.0297	%/mV
		2.5	0.0344	
		1.8	0.0499	
		1.5	0.0744	
		1.2	0.1241	
dR/dT	OCT variation with temperature without re-calibration	3.0	0.189	%/°C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.2	0.317	

Pin Capacitance

Table 2-13: Pin Capacitance for Arria V GZ Devices

Symbol	Description	Maximum	Unit
C_{IOTB}	Input capacitance on the top and bottom I/O pins	6	pF
C_{IOLR}	Input capacitance on the left and right I/O pins	6	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output and feedback pins	6	pF

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Programmable DC gain	DC gain setting = 0	—	0	—	—	0	—	dB
	DC gain setting = 1	—	2	—	—	2	—	dB
	DC gain setting = 2	—	4	—	—	4	—	dB
	DC gain setting = 3	—	6	—	—	6	—	dB
	DC gain setting = 4	—	8	—	—	8	—	dB

Related Information

Arria V Device Overview
For more information about device ordering codes.

Transmitter

Table 2-25: Transmitter Specifications for Arria V GZ Devices

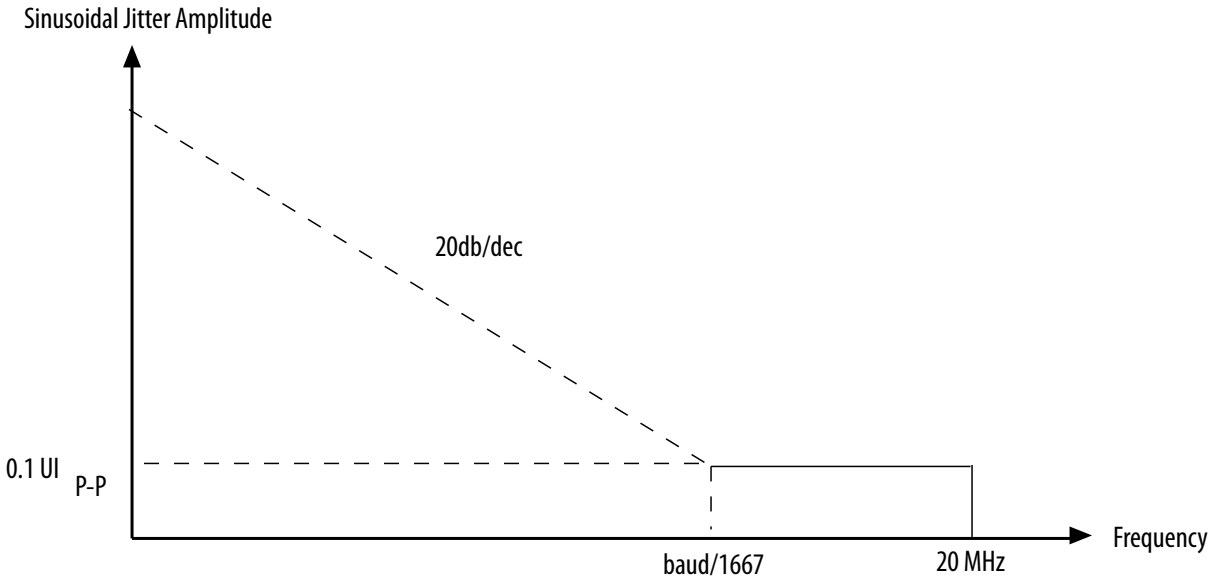
Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported I/O Standards	1.4-V and 1.5-V PCML							
Data rate (Standard PCS)	—	600	—	9900	600	—	8800	Mbps
Data rate (10G PCS)	—	600	—	12500	600	—	10312.5	Mbps

Symbol	Parameter	Min	Typ	Max	Unit
f_{OUT} (169)	Output frequency for an internal global or regional clock (C3, I3L speed grade)	—	—	650	MHz
	Output frequency for an internal global or regional clock (C4, I4 speed grade)	—	—	580	MHz
f_{OUT_EXT} (169)	Output frequency for an external clock output (C3, I3L speed grade)	—	—	667	MHz
	Output frequency for an external clock output (C4, I4 speed grade)	—	—	533	MHz
$t_{OUTDUTY}$	Duty cycle for a dedicated external clock output (when set to 50%)	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	10	ns
$f_{DYCONFIGCLK}$	Dynamic configuration clock for `mgmt_clk` and `scanclk`	—	—	100	MHz
t_{LOCK}	Time required to lock from the end-of-device configuration or deassertion of `areset`	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/ delays)	—	—	1	ms
f_{CLBW}	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth (170)	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the `areset` signal	10	—	—	ns

(169) This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.
(170) High bandwidth PLL settings are not supported in external feedback mode.

Figure 2-5: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate < 1.25 Gbps



Non DPA Mode High-Speed I/O Specifications

Table 2-46: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Sampling Window	—	—	—	300	—	—	300	ps

Symbol	Parameter	Minimum	Maximum	Unit
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (8576 × CLKUSR period) (215)	—	—

Related Information

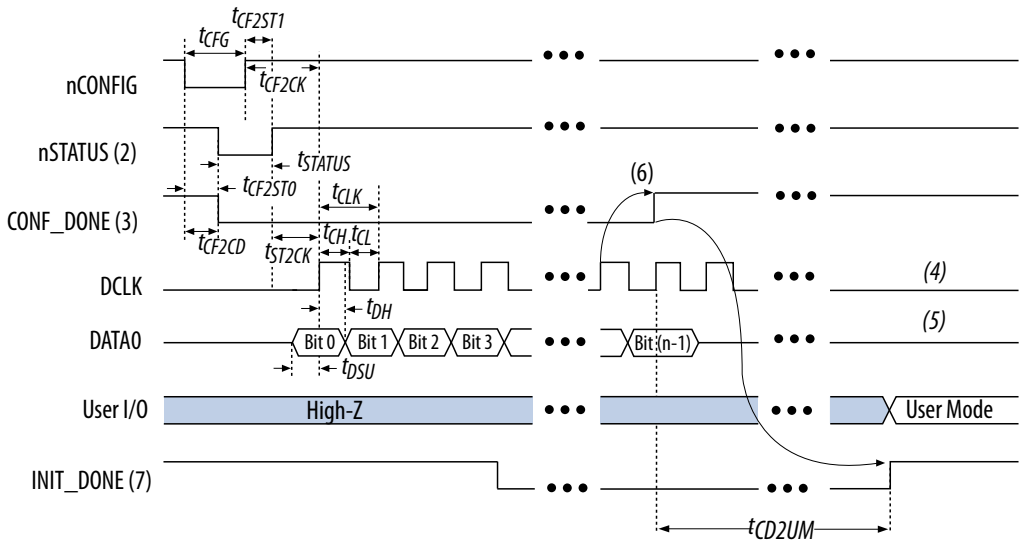
- **DCLK-to-DATA[] Ratio (r) for FPP Configuration** on page 2-57
- **Configuration, Design Security, and Remote System Upgrades in Arria V Devices**

(215) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Passive Serial Configuration Timing

Figure 2-10: PS Configuration Timing Waveform

Timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.



Notes:

1. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
2. After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.
3. After power-up, before and during configuration, CONF_DONE is low.
4. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
5. DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the Device and Pins Option.
6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
7. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Term	Definition
V_{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
V_{SWING}	Differential input voltage
V_X	Input differential cross point voltage
V_{OX}	Output differential cross point voltage
W	High-speed I/O block—clock boost factor

Document Revision History

Date	Version	Changes
February 2017	2017.02.10	• Changed the minimum value for t_{CD2UMC} in the “FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1” table. • Changed the minimum value for t_{CD2UMC} in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1" table. • Changed the minimum value for t_{CD2UMC} in the "AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices" table. • Changed the minimum value for t_{CD2UMC} in the "PS Timing Parameters for Arria V GZ Devices" table. • Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices" table.