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Intel - 5AGXMA5G4F31C4N Datasheet



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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8962
Number of Logic Elements/Cells	190000
Total RAM Bits	13284352
Number of I/O	384
Number of Gates	
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxma5g4f31c4n

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Arria V GX, GT, SX, and ST Device Datasheet



This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Arria® V devices.

Arria V devices are offered in commercial and industrial grades. Commercial devices are offered in -C4 (fastest), -C5, and -C6 speed grades. Industrial grade devices are offered in the -I3 and -I5 speed grades.

Related Information

Arria V Device Overview

Provides more information about the densities and packages of devices in the Arria V family.

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Arria V devices.

Operating Conditions

Arria V devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Arria V devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Arria V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms.

The functional operation of the device is not implied for these conditions.

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Symbol/Description	Condition	Transceiver Speed Grade 4		Transceiver Speed Grade 6			Unit	
		Min	Тур	Max	Min	Тур	Max	Onic
Inter-transceiver block transmitter channel-to- channel skew ⁽³⁹⁾	×N PMA bonded mode			500		_	500	ps

Table 1-24: CMU PLL Specifications for Arria V GX and SX Devices

Symbol/Description	Transceiver Speed Grade 4		Transceiver S	peed Grade 6	Unit	
Symbol/Description	Min	Мах	Min	Мах	Ont	
Supported data range	611	6553.6	611	3125	Mbps	
fPLL supported data range	611	3125	611	3125	Mbps	

Table 1-25: Transceiver-FPGA Fabric Interface Specifications for Arria V GX and SX Devices

Symbol/Description	Transceiver Spee	ed Grade 4 and 6	Unit	
Symbol Description	Min	Max		
Interface speed (single-width mode)	25	187.5	MHz	
Interface speed (double-width mode)	25	163.84	MHz	

Related Information

- CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain on page 1-35
- CTLE Response at Data Rates \leq 3.25 Gbps across Supported AC Gain and DC Gain on page 1-36
- Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines Provides more information about the power supply connection for different data rates.



⁽³⁹⁾ This specification is only applicable to channels on one side of the device across two transceiver banks.

Sumbol/Decertistics	Condition	Т	Unit		
Symbol/Description	Condition	Min	Тур	Мах	Unit
Data rate (10-Gbps transceiver) ⁽⁴⁴⁾	—	0.611	_	10.3125	Gbps
Absolute $\mathrm{V}_{\mathrm{MAX}}$ for a receiver $\mathrm{pin}^{\scriptscriptstyle{(45)}}$	—	_		1.2	V
Absolute $\mathrm{V}_{\mathrm{MIN}}$ for a receiver pin	—	-0.4		—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	_	_	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	_	_	_	2.2	V
Minimum differential eye opening at the receiver serial input pins ⁽⁴⁶⁾	—	100		_	mV
V _{ICM} (AC coupled)	—	_	750 ⁽⁴⁷⁾ /800	—	mV
V _{ICM} (DC coupled)	\leq 3.2Gbps ⁽⁴⁸⁾	670	700	730	mV
	85- Ω setting		85		Ω
Differential on-chip termination	100- Ω setting		100		Ω
resistors	120- Ω setting		120		Ω
	150-Ω setting		150		Ω
$t_{LTR}^{(49)}$	_	_		10	μs
$t_{LTD}^{(50)}$	—	4	—	—	μs

⁽⁴⁵⁾ The device cannot tolerate prolonged operation at this absolute maximum.



⁽⁴⁶⁾ The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

 $^{^{(47)}}$ The AC coupled $V_{\rm ICM}$ is 750 mV for PCIe mode only.

⁽⁴⁸⁾ For standard protocol compliance, use AC coupling.

 $^{^{(49)}}$ t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

⁽⁵⁰⁾ t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.

Protocol	Sub-protocol	Data Rate (Mbps)
	SONET 155	155.52
SONET	SONET 622	622.08
	SONET 2488	2,488.32
Gigabit-capable passive optical network (GPON)	GPON 155	155.52
	GPON 622	622.08
	GPON 1244	1,244.16
	GPON 2488	2,488.32
QSGMII	QSGMII 5000	5,000

Core Performance Specifications

Clock Tree Specifications

Table 1-35: Clock Tree Specifications for Arria V Devices

Darameter		Unit		
Falameter	-I3, -C4	–I5, –C5	-C6	omt
Global clock and Regional clock	625	625	525	MHz
Peripheral clock	450	400	350	MHz

PLL Specifications

Table 1-36: PLL Specifications for Arria V Devices

This table lists the Arria V PLL block specifications. Arria V PLL block does not include HPS PLL.



DPA Lock Time Specifications

Figure 1-4: Dynamic Phase Alignment (DPA) Lock Time Specifications with DPA PLL Calibration Enabled



Table 1-41: DPA Lock Time Specifications for Arria V Devices

The specifications are applicable to both commercial and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽⁸⁴⁾	Maximum Data Transition
SPI-4	00000000001111111111	2	128	640
Parallel Rapid I/O	00001111	2	128	640
	10010000	4	64	640
Miscellaneous	10101010	8	32	640
witscenaricous	01010101	8	32	640

⁽⁸⁴⁾ This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.



HPS PLL Input Jitter

Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate. The divide value (N) is the value programmed into the denominator field of the VCO register for each PLL. The PLL input reference clock is divided by this value. The range of the denominator is 1 to 64.

Maximum input jitter = Input clock period × Divide value (N) × 0.02

Table 1-50: Examples of Maximum Input Jitter

Input Reference Clock Period	Divide Value (N)	Maximum Jitter	Unit
40 ns	1	0.8	ns
40 ns	2	1.6	ns
40 ns	4	3.2	ns

Quad SPI Flash Timing Characteristics

Table 1-51: Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices

Symbol	Description	Min	Тур	Max	Unit
F _{clk}	SCLK_OUT clock frequency (External clock)	_	_	108	MHz
T _{qspi_clk}	QSPI_CLK clock period (Internal reference clock)	2.32			ns
T _{dutycycle}	SCLK_OUT duty cycle	45		55	%
T _{dssfrst}	Output delay QSPI_SS valid before first clock edge		1/2 cycle of SCLK_OUT		ns
T _{dsslst}	Output delay QSPI_SS valid after last clock edge	-1		1	ns
T _{dio}	I/O data output delay	-1		1	ns
T _{din_start}	Input data valid start			$(2 + R_{delay}) \times T_{qspi_clk} - 7.52^{(85)}$	ns



After the Boot ROM code exits and control is passed to the preloader, software can adjust the value of drvsel and smplsel via the system manager. drvsel can be set from 1 to 7 and smplsel can be set from 0 to 7. While the preloader is executing, the values for SDMMC_CLK and SDMMC_CLK_OUT increase to a maximum of 200 MHz and 50 MHz respectively.

The SD/MMC interface calibration support will be available in a future release of the preloader through the SoC EDS software update.

Symbol	Description	Min	Мах	Unit
	SDMMC_CLK clock period (Identification mode)	20	_	ns
T _{sdmmc_clk} (internal reference clock)	SDMMC_CLK clock period (Default speed mode)	5	—	ns
	SDMMC_CLK clock period (High speed mode)	5	_	ns
	SDMMC_CLK_OUT clock period (Identification mode)	2500	—	ns
T _{sdmmc_clk_out} (interface output clock)	SDMMC_CLK_OUT clock period (Default speed mode)	40	_	ns
	SDMMC_CLK_OUT clock period (High speed mode)	20	—	ns
T _{dutycycle}	SDMMC_CLK_OUT duty cycle	45	55	%
T _d	SDMMC_CMD/SDMMC_D output delay	$\frac{(T_{sdmmc_clk} \times drvsel)/2}{-1.23}$	$\begin{array}{l}(\mathrm{T}_{sdmmc_clk}\times\texttt{drvsel})/2\\+1.69^{\ (87)}\end{array}$	ns
T _{su}	Input setup time	$1.05 - (T_{sdmmc_clk} \times smplsel)/2^{(88)}$	_	ns
T _h	Input hold time	$\frac{(T_{sdmmc_clk} \times smplsel)}{2^{(88)}}$	_	ns



⁽⁸⁷⁾ drvsel is the drive clock phase shift select value.

⁽⁸⁸⁾ smplsel is the sample clock phase shift select value.

1-80 AS Configuration Timing

Symbol	Parameter	Minimum	Maximum	Unit
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times maximum$ DCLK period	—	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + ($T_{init} \times CLKUSR$ period)		
T _{init}	Number of clock cycles required for device initialization	8,576		Cycles

Related Information

FPP Configuration Timing

Provides the FPP configuration timing waveforms.

AS Configuration Timing

Table 1-68: AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices

The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

The t_{CF2CD} , t_{CF2ST0} , t_{CFG} , t_{STATUS} , and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in PS Timing Parameters for Arria V Devices table. You can obtain the t_{CF2ST1} value if you do not delay configuration by externally holding nSTATUS low.

Symbol	Parameter	Minimum	Maximum	Unit
t _{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	2	ns
t _{SU}	Data setup time before the falling edge on DCLK	1.5		ns
t _{DH}	Data hold time after the falling edge on DCLK	0	_	ns
t _{CD2UM}	CONF_DONE high to user mode	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	_	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + ($T_{init} \times CLKUSR$ period)	_	—
T _{init}	Number of clock cycles required for device initialization	8,576		Cycles



Related Information

- PS Configuration Timing on page 1-81
- AS Configuration Timing

Provides the AS configuration timing waveform.

DCLK Frequency Specification in the AS Configuration Scheme

Table 1-69: DCLK Frequency Specification in the AS Configuration Scheme

This table lists the internal clock frequency specification for the AS configuration scheme. The DCLK frequency specification applies when you use the internal oscillator as the configuration clock source. The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Parameter	Minimum	Typical	Maximum	Unit
	5.3	7.9	12.5	MHz
DOLY frequency in AS configuration scheme	10.6	15.7	25.0	MHz
belk frequency in AS configuration scheme	21.3	31.4	50.0	MHz
	42.6	62.9	100.0	MHz

PS Configuration Timing

Table 1-70: PS Timing Parameters for Arria V Devices

Symbol	Parameter	Minimum	Maximum	Unit
t _{CF2CD}	nCONFIG low to CONF_DONE low	_	600	ns
t _{CF2ST0}	nconfig low to nstatus low	—	600	ns
t _{CFG}	nCONFIG low pulse width	2	_	μs
t _{STATUS}	nSTATUS low pulse width	268	1506 ⁽¹⁰³⁾	μs
t _{CF2ST1}	nCONFIG high to nSTATUS high	_	1506(104)	μs

 $^{^{(103)}\,}$ You can obtain this value if you do not delay configuration by extending the <code>nCONFIG</code> or <code>nSTATUS</code> low pulse width.



⁽¹⁰⁴⁾ You can obtain this value if you do not delay configuration by externally holding nSTATUS low.

1-94 Document Revision History

Term	Definition
V _{OX}	Output differential cross point voltage
W	High-speed I/O block—Clock boost factor

Document Revision History

Date	Version	Changes
December 2016	2016.12.09	 Updated V_{ICM} (AC coupled) specifications in Receiver Specifications for Arria V GX and SX Devices table. Added maximum specification for T_d in Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices table. Updated T_{init} specifications in the following tables: FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Arria V Devices FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices PS Timing Parameters for Arria V Devices
June 2016	2016.06.10	 Changed pin capacitance to maximum values. Updated SPI Master Timing Requirements for Arria V Devices table. Added T_{su} and T_h specifications. Removed T_{dinmax} specifications. Updated SPI Master Timing Diagram. Updated T_{clk} spec from maximum to minimum in I²C Timing Requirements for Arria V Devices table.





Transceiver Power Supply Requirements

Table 2-7: Transceiver Power Supply Voltage Requirements for Arria V GZ Devices

Conditions	VCCR_GXB and VCCT_GXB ⁽¹²²⁾	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true:	1.05			
• Data rate > 10.3 Gbps.				
• DFE is used.				
If ANY of the following conditions are true ⁽¹²³⁾ :	1.0	3.0		
 ATX PLL is used. Data rate > 6.5Gbps. DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used. 			1.5	V
If ALL of the following conditions are true:	0.85	2.5		
 ATX PLL is not used. Data rate ≤ 6.5Gbps. DFE, AEQ, and EyeQ are not used. 				

DC Characteristics

Supply Current

Standby current is the current drawn from the respective power rails used for power budgeting.

Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.



⁽¹²²⁾ If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to 0.85 V, they can be shared with the VCC core supply.

⁽¹²³⁾ Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

Bus Hold Specifications

Table 2-9: Bus Hold Parameters for Arria V GZ Devices

			V _{cCIO}										
Parameter	Symbol	Conditions	1.2	2 V	1.5	5 V	1.8	3 V	2.5	5 V	3.0	V	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I _{SUSL}	V _{IN} > V _{IL} (maximum)	22.5	_	25.0	_	30.0		50.0	_	70.0	_	μΑ
High sustaining current	I _{SUSH}	V _{IN} < V _{IH} (minimum)	-22.5	_	-25.0	_	-30.0	_	-50.0	_	-70.0	_	μΑ
Low overdrive current	I _{ODL}	$0V < V_{IN} < V_{CCIO}$	_	120	_	160	_	200	_	300	_	500	μΑ
High overdrive current	I _{ODH}	$0V < V_{IN} < V_{CCIO}$	—	-120	_	-160	_	-200		-300	_	-500	μΑ
Bus-hold trip point	V _{TRIP}		0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block.

Table 2-10: OCT Calibration Accuracy Specifications for Arria V GZ Devices

OCT calibration accuracy is valid at the time of calibration only.





I/O Standard		V _{CCIO} (V)			V _{REF} (V)			V _T	_T (V)
	Min	Тур	Max	Min	Тур	Max	Min	Тур	Мах
SSTL-135 Class I, II	1.283	1.35	1.418	$0.49 \times V_{CCIO}$	$0.5 imes V_{ m CCIO}$	$0.51 imes V_{ m CCIO}$	0.49 × V _{CCIO}	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
SSTL-125 Class I, II	1.19	1.25	1.26	$0.49 \times V_{CCIO}$	$0.5 imes V_{ m CCIO}$	$0.51 \times V_{ m CCIO}$	$0.49 \times V_{ m CCIO}$	0.5 × VCCIO	$0.51 \times V_{CCIO}$
SSTL-12 Class I, II	1.14	1.20	1.26	$0.49 \times V_{CCIO}$	$0.5 imes V_{ m CCIO}$	$0.51 \times V_{ m CCIO}$	0.49 × V _{CCIO}	0.5 × VCCIO	$0.51 \times V_{CCIO}$
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	_	V _{CCIO} /2	_
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	_	V _{CCIO} /2	_
HSTL-12 Class I, II	1.14	1.2	1.26	$0.47 \times V_{CCIO}$	$0.5 imes V_{ m CCIO}$	$0.53 \times V_{ m CCIO}$	_	V _{CCIO} /2	_
HSUL-12	1.14	1.2	1.3	$0.49 \times V_{CCIO}$	$0.5 \times V_{ m CCIO}$	$0.51 \times V_{ m CCIO}$			_

Table 2-18: Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Arria V GZ Devices

I/O Standard	V _{IL(D}	_{C)} (V)	V _{IH(D}	_{_)} (V)	V _{IL(AC)} (V)	V _{IH(AC)} (V)	V _{OL} (V)	V _{OH} (V)	L.(mA)	I. (mA)
	Min	Max	Min	Max	Мах	Min	Max	Min	י _{סן} (וווא)	
SSTL-2 Class I	-0.3	V _{REF} – 0.15	V _{REF} + 0.15	V _{CCIO} + 0.3	V _{REF} – 0.31	V _{REF} + 0.31	V _{TT} – 0.608	V _{TT} + 0.608	8.1	-8.1
SSTL-2 Class II	-0.3	V _{REF} – 0.15	V _{REF} + 0.15	V _{CCIO} + 0.3	V _{REF} – 0.31	V _{REF} + 0.31	V _{TT} – 0.81	V _{TT} + 0.81	16.2	-16.2
SSTL-18 Class I	-0.3	V _{REF} – 0.125	V _{REF} + 0.125	V _{CCIO} + 0.3	V _{REF} – 0.25	V _{REF} + 0.25	V _{TT} – 0.603	V _{TT} + 0.603	6.7	-6.7



Sumbol/Description	Conditions	Trans	ceiver Spee	d Grade 2	Transo	Unit		
Symbol/Description	Conditions	Min	Тур	Max	Min	Тур	Max	
fixedclk clock frequency	PCIe Receiver Detect	_	100 or 125	_	_	100 or 125	_	MHz
Reconfiguration clock (mgmt_clk_ clk) frequency	—	100		125	100	_	125	MHz

Related Information

Arria V Device Overview

For more information about device ordering codes.

Receiver

Table 2-24: Receiver Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Trans	ceiver Spee	d Grade 2	Transc	Unit		
Symbol Description	Conditions	Min	Тур	Max	Min	Тур	Max	Onic
Supported I/O Standards	1.4-V PCML, 1.5-V PCML, 2.5	-V PCML,	LVPECL, a	and LVDS				
Data rate (Standard PCS) (143), (144)	—	600		9900	600	_	8800	Mbps
Data rate (10G PCS) (143), (144)	_	600		12500	600	_	10312.5	Mbps
Absolute $\mathrm{V}_{\mathrm{MAX}}$ for a receiver pin $^{(145)}$	—			1.2			1.2	V
Absolute V_{MIN} for a receiver pin	_	-0.4	_		-0.4	_	_	V

⁽¹⁴³⁾ The line data rate may be limited by PCS-FPGA interface speed grade.

⁽¹⁴⁴⁾ To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.



⁽¹⁴⁵⁾ The device cannot tolerate prolonged operation at this absolute maximum.

Sumbol	Conditions -	C3, I3L		C4, I4			Unit	
Symbol		Min	Тур	Max	Min	Тур	Max	Onit
True Differential I/O Standards - f _{HSDR} (data rate)	SERDES factor J = 3 to 10 (182), (183)	(184)	—	1250	(184)	—	1050	Mbps
	SERDES factor $J \ge 4$ LVDS TX with DPA (185), (186), (187), (188)	(184)		1600	(184)	_	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(184)	—	(189)	(184)	_	(189)	Mbps
	SERDES factor J = 1, uses SDR Register	(184)	—	(189)	(184)		(189)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f _{HSDR} (data rate) (190)	SERDES factor J = 4 to 10 ⁽¹⁹¹⁾	(184)		840	(184)		840	Mbps

⁽¹⁸²⁾ If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

- ⁽¹⁸⁵⁾ Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.
- Requires package skew compensation with PCB trace length. (186)
- (187)Do not mix single-ended I/O buffer within LVDS I/O bank.
- Chip-to-chip communication only with a maximum load of 5 pF. (188)
- ⁽¹⁸⁹⁾ The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.
- ⁽¹⁹⁰⁾ You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.
- ⁽¹⁹¹⁾ When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.



⁽¹⁸³⁾ The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

⁽¹⁸⁴⁾ The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

Number of DQS Delay Buffers	C3, I3L	C4, I4	Unit
4	120	128	ps

Memory Output Clock Jitter Specifications

Table 2-50: Memory Output Clock Jitter Specification for Arria V GZ Devices

The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

Clock Notwork	Parameter	Symbol	C3, I3L		C4, I4		Unit
CIOCK NELWOIK			Min	Мах	Min	Мах	
Regional	Clock period jitter	t _{JIT(per)}	-55	55	-55	55	ps
	Cycle-to-cycle period jitter	t _{JIT(cc)}	-110	110	-110	110	ps
	Duty cycle jitter	t _{JIT(duty)}	-82.5	82.5	-82.5	82.5	ps
Global	Clock period jitter	t _{JIT(per)}	-82.5	82.5	-82.5	82.5	ps
	Cycle-to-cycle period jitter	t _{JIT(cc)}	-165	165	-165	165	ps
	Duty cycle jitter	t _{JIT(duty)}	-90	90	-90	90	ps
PHY Clock	Clock period jitter	t _{JIT(per)}	-30	30	-35	35	ps
	Cycle-to-cycle period jitter	t _{JIT(cc)}	-60	60	-70	70	ps
	Duty cycle jitter	t _{JIT(duty)}	-45	45	-56	56	ps



Symbol	Parameter	Minimum	Maximum	Unit
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times maximum$	—	_
		DCLK period		
t _{CD2UM} C	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (8576 × CLKUSR period) (209)		_

Related Information

- DCLK-to-DATA[] Ratio (r) for FPP Configuration on page 2-57 ٠
- Configuration, Design Security, and Remote System Upgrades in Arria V Devices

Arria V GZ Device Datasheet

Altera Corporation



⁽²⁰⁸⁾ The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

⁽²⁰⁹⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.

Symbol	Parameter	Minimum	Maximum	Unit
t _{CO}	DCLK falling edge to AS_DATA0/ASDO output	_	4	ns
t _{SU}	Data setup time before falling edge on DCLK	1.5		ns
t _H	Data hold time after falling edge on DCLK	0	—	ns
t _{CD2UM}	CONF_DONE high to user mode ⁽²¹⁶⁾	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK}$ period	—	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (8576 × clkusr period)	_	_

Table 2-59: DCLK Frequency Specification in the AS Configuration Scheme

This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

The AS multi-device configuration scheme does not support ${\tt DCLK}$ frequency of 100 MHz.

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

Related Information

- Passive Serial Configuration Timing on page 2-67
- Configuration, Design Security, and Remote System Upgrades in Arria V Devices





⁽²¹⁶⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Programmable IOE Delay

Fast Model Slow Model Available Parameter (228) Min Offset (229) Unit Settings Industrial Commercial C3 C4 I3L 14 D1 64 0 0.464 0.493 0.924 1.011 0.921 1.006 ns 0 D2 32 0.230 0.244 0.459 0.503 0.456 0.500 ns D3 8 0 1.699 2.992 3.192 1.587 3.047 3.257 ns 0 D4 64 0.464 0.492 0.924 1.011 0.920 1.006 ns D5 64 0 0.464 0.493 0.924 1.011 0.921 1.006 ns 0.499 D6 32 0 0.244 0.503 0.229 0.458 0.456 ns

Table 2-66: IOE Programmable Delay for Arria V GZ Devices

Programmable Output Buffer Delay

Table 2-67: Programmable Output Buffer Delay for Arria V GZ Devices

You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

Symbol	Parameter	Typical	Unit
		0 (default)	ps
D _{OUTBUF}	Rising and/or falling edge delay	50	ps
		100	ps
		150	ps

⁽²²⁸⁾ You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D4**, **D5**, and **D6** in the **Assignment Name** column of **Assignment Editor**.





⁽²²⁹⁾ Minimum offset does not include the intrinsic delay.

Date	Version	Changes
July 2014	3.8	 Updated Table 21. Updated Table 22 V_{OCM} (DC Coupled) condition. Updated the DCLK note to Figure 6, Figure 7, and Figure 9. Added note to Table 5 and Table 6. Added the DCLK specification to Table 50. Added note to Table 51. Updated the list of parameters in Table 53.
February 2014	3.7	Updated Table 28.
December 2013	3.6	 Updated Table 2, Table 13, Table 18, Table 19, Table 22, Table 30, Table 33, Table 37, Table 38, Table 45, Table 46, Table 47, Table 56, Table 49. Updated "PLL Specifications".
August 2013	3.5	Updated Table 28.
August 2013	3.4	 Removed Preliminary tags for Table 2, Table 4, Table 5, Table 14, Table 27, Table 28, Table 29, Table 31, Table 32, Table 43, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, and Table 54. Updated Table 2 and Table 28.
June 2013	3.3	Updated Table 23, Table 28, Table 51, and Table 55.
May 2013	3.2	 Added Table 23. Updated Table 5, Table 22, Table 26, and Table 57. Updated Figure 6, Figure 7, Figure 8, and Figure 9.
March 2013	3.1	 Updated Table 2, Table 6, Table 7, Table 8, Table 19, Table 22, Table 26, Table 29, Table 52. Updated "Maximum Allowed Overshoot and Undershoot Voltage".
December 2012	3.0	Initial release.

