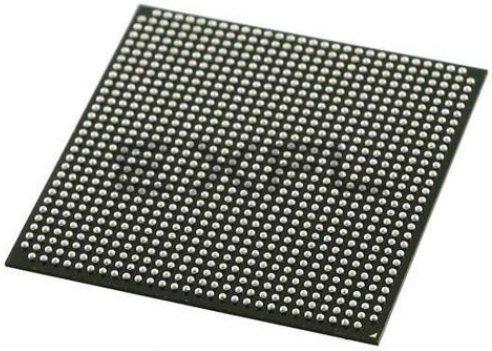

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8962
Number of Logic Elements/Cells	190000
Total RAM Bits	13284352
Number of I/O	384
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxma5g4f31i5

Symbol	Description	Condition	Minimum[1]	Typical	Maximum[1]	Unit
V_{CC}	Core voltage power supply	–C4, –I5, –C5, –C6	1.07	1.1	1.13	V
		–I3	1.12	1.15	1.18	V
V_{CCP}	Periphery circuitry, PCIe hard IP block, and transceiver PCS power supply	–C4, –I5, –C5, –C6	1.07	1.1	1.13	V
		–I3	1.12	1.15	1.18	V
V_{CCPGM}	Configuration pins power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
V_{CC_AUX}	Auxiliary supply	—	2.375	2.5	2.625	V
V_{CCBAT}[2]	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V
V_{CCPD}[3]	I/O pre-driver power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V

(1) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.
(2) If you do not use the design security feature in Arria V devices, connect V_{CCBAT} to a 1.5-V, 2.5-V, or 3.0-V power supply. Arria V power-on reset (POR) circuitry monitors V_{CCBAT}. Arria V devices do not exit POR if V_{CCBAT} is not powered up.
(3) V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25, or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V. V_{CCPD} must be 3.3 V when V_{CCIO} is 3.3 V.

Parameter	Symbol	Condition	V_{CCIO} (V)												Unit
			1.2		1.5		1.8		2.5		3.0		3.3		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 1-8: OCT Calibration Accuracy Specifications for Arria V Devices

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (V)	Calibration Accuracy			Unit
			–I3, –C4	–I5, –C5	–C6	
25-Ω R_S	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
50-Ω R_S	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	±15	±15	±15	%
48-Ω, 60-Ω, and 80-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, and 80-Ω setting)	V_{CCIO} = 1.2	±15	±15	±15	%
50-Ω R_T	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 2.5, 1.8, 1.5, 1.2	–10 to +40	–10 to +40	–10 to +40	%
20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25	–10 to +40	–10 to +40	–10 to +40	%

Symbol	Description	Maximum	Unit
$I_{XCVR\text{-}RX\ (DC)}$	DC current per transceiver receiver (RX) pin	50	mA

Internal Weak Pull-Up Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up.

Table 1-13: Internal Weak Pull-Up Resistor Values for Arria V Devices

Symbol	Description	Condition (V)[11]	Value[12]	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V_{CCIO} = 3.3 ±5%	25	kΩ
		V_{CCIO} = 3.0 ±5%	25	kΩ
		V_{CCIO} = 2.5 ±5%	25	kΩ
		V_{CCIO} = 1.8 ±5%	25	kΩ
		V_{CCIO} = 1.5 ±5%	25	kΩ
		V_{CCIO} = 1.35 ±5%	25	kΩ
		V_{CCIO} = 1.25 ±5%	25	kΩ
		V_{CCIO} = 1.2 ±5%	25	kΩ

Related Information

Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines

Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.

(10) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C\ dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

(11) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(12) Valid with ±10% tolerances to cover changes over PVT.

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Spread-spectrum modulating clock frequency	PCI Express® (PCIe)	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	Ω
V_{ICM} (AC coupled)	—	—	1.1/1.15[26]	—	—	1.1/1.15[26]	—	V
V_{ICM} (DC coupled)	HCSL I/O standard for the PCIe reference clock	250	—	550	250	—	550	mV
Transmitter REFCLK phase noise[27]	10 Hz	—	—	–50	—	—	–50	dBc/Hz
	100 Hz	—	—	–80	—	—	–80	dBc/Hz
	1 KHz	—	—	–110	—	—	–110	dBc/Hz
	10 KHz	—	—	–120	—	—	–120	dBc/Hz
	100 KHz	—	—	–120	—	—	–120	dBc/Hz
	≥1 MHz	—	—	–130	—	—	–130	dBc/Hz
R_{REF}	—	—	2000 ±1%	—	—	2000 ±1%	—	Ω

(26) For data rate ≤3.2 Gbps, connect $V_{CCR\_GXBL/R}$ to either 1.1-V or 1.15-V power supply. For data rate >3.2 Gbps, connect $V_{CCR\_GXBL/R}$ to a 1.15-V power supply. For details, refer to the Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines.

(27) The transmitter REFCLK phase jitter is 30 ps p-p at bit error rate (BER) 10^{-12}.

Quartus Prime 1st Post Tap Pre-Emphasis Setting	Quartus Prime V_{OD} Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
16	—	—	9.56	7.73	6.49	—	—	dB
17	—	—	10.43	8.39	7.02	—	—	dB
18	—	—	11.23	9.03	7.52	—	—	dB
19	—	—	12.18	9.7	8.02	—	—	dB
20	—	—	13.17	10.34	8.59	—	—	dB
21	—	—	14.2	11.1	—	—	—	dB
22	—	—	15.38	11.87	—	—	—	dB
23	—	—	—	12.67	—	—	—	dB
24	—	—	—	13.48	—	—	—	dB
25	—	—	—	14.37	—	—	—	dB
26	—	—	—	—	—	—	—	dB
27	—	—	—	—	—	—	—	dB
28	—	—	—	—	—	—	—	dB
29	—	—	—	—	—	—	—	dB
30	—	—	—	—	—	—	—	dB
31	—	—	—	—	—	—	—	dB

Related Information

SPICE Models for Altera Devices
Provides the Arria V HSSI HSPICE models.

Transceiver Compliance Specification

The following table lists the physical medium attachment (PMA) specification compliance of all supported protocol for Arria V GX, GT, SX, and ST devices. For more information about the protocol parameter details and compliance specifications, contact your Altera Sales Representative.

Table 1-34: Transceiver Compliance Specification for All Supported Protocol for Arria V GX, GT, SX, and ST Devices

Protocol	Sub-protocol	Data Rate (Mbps)
PCIe	PCIe Gen1	2,500
	PCIe Gen2	5,000
	PCIe Cable	2,500
XAUI	XAUI 2135	3,125
Serial RapidIO® (SRIO)	SRIO 1250 SR	1,250
	SRIO 1250 LR	1,250
	SRIO 2500 SR	2,500
	SRIO 2500 LR	2,500
	SRIO 3125 SR	3,125
	SRIO 3125 LR	3,125
	SRIO 5000 SR	5,000
	SRIO 5000 MR	5,000
	SRIO 5000 LR	5,000
	SRIO_6250_SR	6,250
	SRIO_6250_MR	6,250
	SRIO_6250_LR	6,250

Protocol	Sub-protocol	Data Rate (Mbps)
Common Public Radio Interface (CPRI)	CPRI E6LV	614.4
	CPRI E6HV	614.4
	CPRI E6LVII	614.4
	CPRI E12LV	1,228.8
	CPRI E12HV	1,228.8
	CPRI E12LVII	1,228.8
	CPRI E24LV	2,457.6
	CPRI E24LVII	2,457.6
	CPRI E30LV	3,072
	CPRI E30LVII	3,072
	CPRI E48LVII	4,915.2
	CPRI E60LVII	6,144
	CPRI E96LVIII(60)	9,830.4
Gbps Ethernet (GbE)	GbE 1250	1,250
OBSAI	OBSAI 768	768
	OBSAI 1536	1,536
	OBSAI 3072	3,072
	OBSAI 6144	6,144
Serial digital interface (SDI)	SDI 270 SD	270
	SDI 1485 HD	1,485
	SDI 2970 3G	2,970

(60) You can achieve compliance with TX channel restriction of one HSSI channel per six-channel transceiver bank.

Symbol		Condition	–I3, –C4			–I5, –C5			–C6			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	TCCS	True Differential I/O Standards	—	—	150	—	—	150	—	—	150	ps
		Emulated Differential I/O Standards	—	—	300	—	—	300	—	—	300	ps
Receiver	True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J =3 to 10(76)	150	—	1250	150	—	1250	150	—	1050	Mbps
		SERDES factor J ≥ 8 with DPA(76)(78)	150	—	1600	150	—	1500	150	—	1250	Mbps
	f_{HSDR} (data rate)	SERDES factor J = 3 to 10	(77)	—	(83)	(77)	—	(83)	(77)	—	(83)	Mbps
		SERDES factor J = 1 to 2, uses DDR registers	(77)	—	(79)	(77)	—	(79)	(77)	—	(79)	Mbps
DPA Mode	DPA run length	—	—	—	10000	—	—	10000	—	—	10000	UI
Soft-CDR Mode	Soft-CDR ppm tolerance	—	—	—	300	—	—	300	—	—	300	±ppm
Non-DPA Mode	Sampling Window	—	—	—	300	—	—	300	—	—	300	ps

(83) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

Arria V GZ Device Datasheet

2

2017.02.10

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This document covers the electrical and switching characteristics for Arria V GZ devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, core, and periphery performance. This document also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

Related Information

Arria V Device Overview
For information regarding the densities and packages of devices in the Arria V GZ family.

Electrical Characteristics

Operating Conditions

When you use Arria V GZ devices, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Arria V GZ devices, you must consider the operating requirements described in this datasheet.

Arria V GZ devices are offered in commercial and industrial temperature grades.

Commercial devices are offered in –3 (fastest) and –4 core speed grades. Industrial devices are offered in –3L and –4 core speed grades. Arria V GZ devices are offered in –2 and –3 transceiver speed grades.

Table 2-1: Commercial and Industrial Speed Grade Offering for Arria V GZ Devices

C = Commercial temperature grade; I = Industrial temperature grade.

Lower number refers to faster speed grade.

L = Low power devices.

Transceiver Speed Grade	Core Speed Grade			
	C3	C4	I3L	I4
2	Yes	—	Yes	—
3	—	Yes	—	Yes

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Arria V GZ devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions other than those listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 2-2: Absolute Maximum Ratings for Arria V GZ Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Power supply for core voltage and periphery circuitry	–0.5	1.35	V
V_{CCPT}	Power supply for programmable power technology	–0.5	1.8	V
V_{CCPGM}	Power supply for configuration pins	–0.5	3.9	V
V_{CC_AUX}	Auxiliary supply for the programmable power technology	–0.5	3.4	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	–0.5	3.9	V
V_{CCPD}	I/O pre-driver power supply	–0.5	3.9	V
V_{CCIO}	I/O power supply	–0.5	3.9	V
V_{CCD_FPLL}	PLL digital power supply	–0.5	1.8	V
V_{CCA_FPLL}	PLL analog power supply	–0.5	3.4	V

Transceiver Power Supply Requirements

Table 2-7: Transceiver Power Supply Voltage Requirements for Arria V GZ Devices

Conditions	VCCR_GXB and VCCT_GXB (122)	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true: • Data rate > 10.3 Gbps. • DFE is used.	1.05	3.0	1.5	V
If ANY of the following conditions are true (123) : • ATX PLL is used. • Data rate > 6.5Gbps. • DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used.	1.0			
If ALL of the following conditions are true: • ATX PLL is not used. • Data rate ≤ 6.5Gbps. • DFE, AEQ, and EyeQ are not used.	0.85	2.5		

DC Characteristics

Supply Current

Standby current is the current drawn from the respective power rails used for power budgeting.

Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

(122) If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to 0.85 V, they can be shared with the VCC core supply.

(123) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

Symbol	Description	Conditions	Resistance Tolerance		Unit
			C3, I3L	C4, I4	
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8 and 1.5 V	±40	±40	%
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.2 V	±50	±50	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8 and 1.5 V	±40	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±50	±50	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCIO} = 2.5 V	±25	±25	%

Figure 2-1: OCT Variation Without Re-Calibration for Arria V GZ Devices

$$R_{OCT} = R_{SCAL}\left(1 + \left(\frac{dR}{dT} \times \triangle T\right) \pm \left(\frac{dR}{dV} \times \triangle V\right)\right)$$

Notes:
1. The R_{OCT} value shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
2. R_{SCAL} is the OCT resistance value at power-up.
3. ΔT is the variation of temperature with respect to the temperature at power-up.
4. ΔV is the variation of voltage with respect to the V_{CCIO} at power-up.
5. dR/dT is the percentage change of R_{SCAL} with temperature.
6. dR/dV is the percentage change of R_{SCAL} with voltage.

Table 2-12: OCT Variation after Power-Up Calibration for Arria V GZ Devices

Valid for a V_{CCIO} range of ±5% and a temperature range of 0° to 85°C.

Symbol	Description	V_{CCIO} (V)	Typical	Unit
dR/dV	OCT variation with voltage without re-calibration	3.0	0.0297	%/mV
		2.5	0.0344	
		1.8	0.0499	
		1.5	0.0744	
		1.2	0.1241	
dR/dT	OCT variation with temperature without re-calibration	3.0	0.189	%/°C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.2	0.317	

Pin Capacitance

Table 2-13: Pin Capacitance for Arria V GZ Devices

Symbol	Description	Maximum	Unit
C_{IOTB}	Input capacitance on the top and bottom I/O pins	6	pF
C_{IOLR}	Input capacitance on the left and right I/O pins	6	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output and feedback pins	6	pF

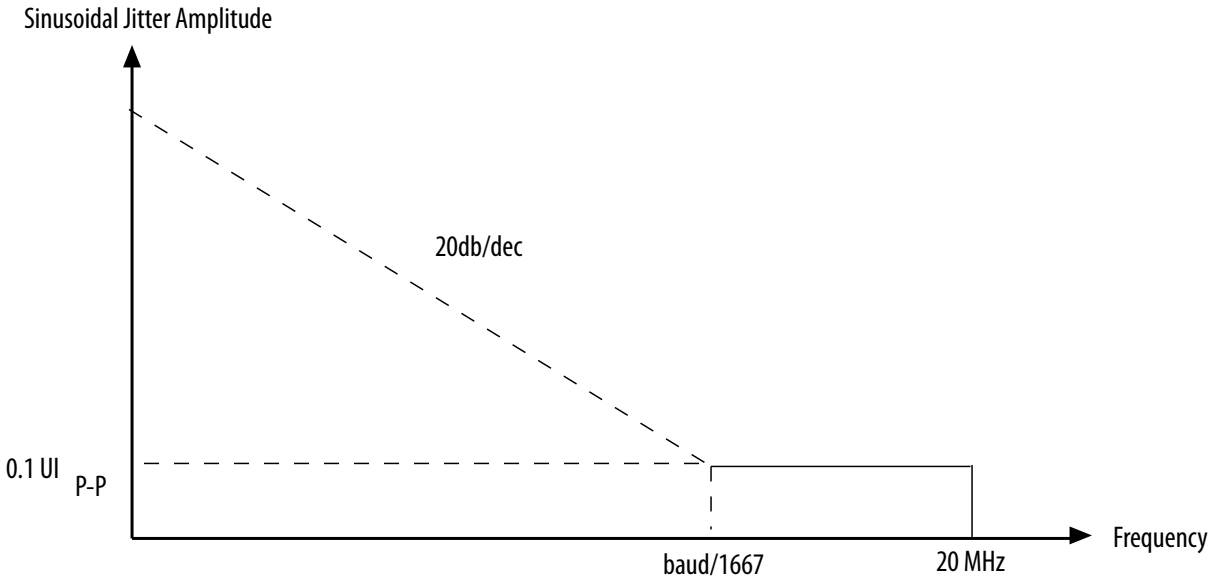
Symbol	Parameter	Min	Typ	Max	Unit
t_{OUTPJ_IO}, (173), (175)	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
t_{FOUTPJ_IO} (173), (175), (176)	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
t_{OUTCCJ_IO} (173), (175)	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{FOUTCCJ\_IO}$ (173), (175), (176)	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{CASC\_OUTPJ\_DC}$ (173), (177)	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period Jitter for a dedicated clock output in cascaded PLLS ($f_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits

(175) The external memory interface clock output jitter specifications use a different measurement method, which is available in the "Memory Output Clock Jitter Specification for Arria V GZ Devices" table.

(176) This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05–0.95 must be ≥ 1000 MHz.

(177) The cascaded PLL specification is only applicable with the following condition:
a. Upstream PLL: 0.59Mhz ≤ Upstream PLL BW < 1 MHz
b. Downstream PLL: Downstream PLL BW > 2 MHz

Figure 2-5: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate < 1.25 Gbps



Non DPA Mode High-Speed I/O Specifications

Table 2-46: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

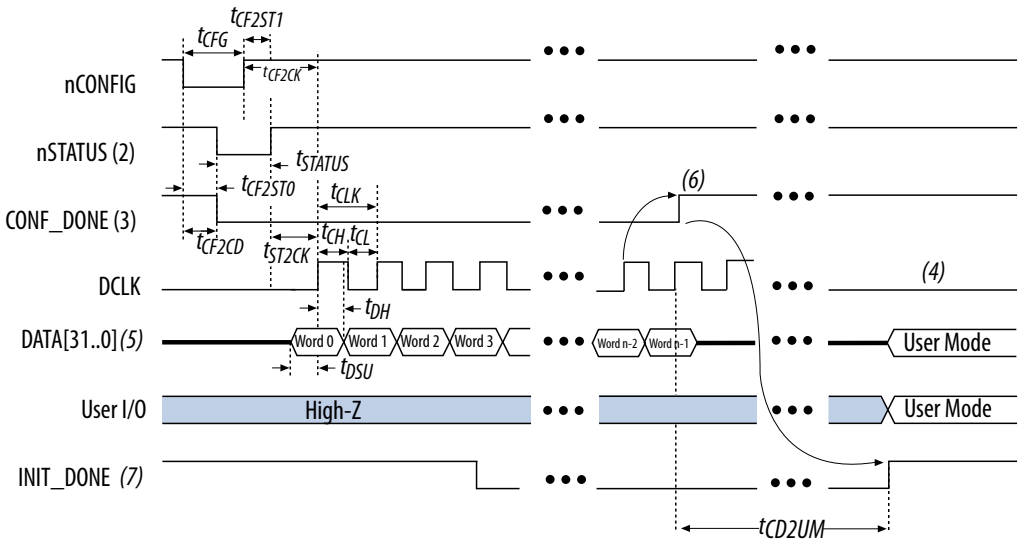
When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Sampling Window	—	—	—	300	—	—	300	ps

FPP Configuration Timing when DCLK to DATA[] = 1

Figure 2-7: FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1

Timing waveform for FPP configuration when using a MAX® II or MAX V device as an external host.

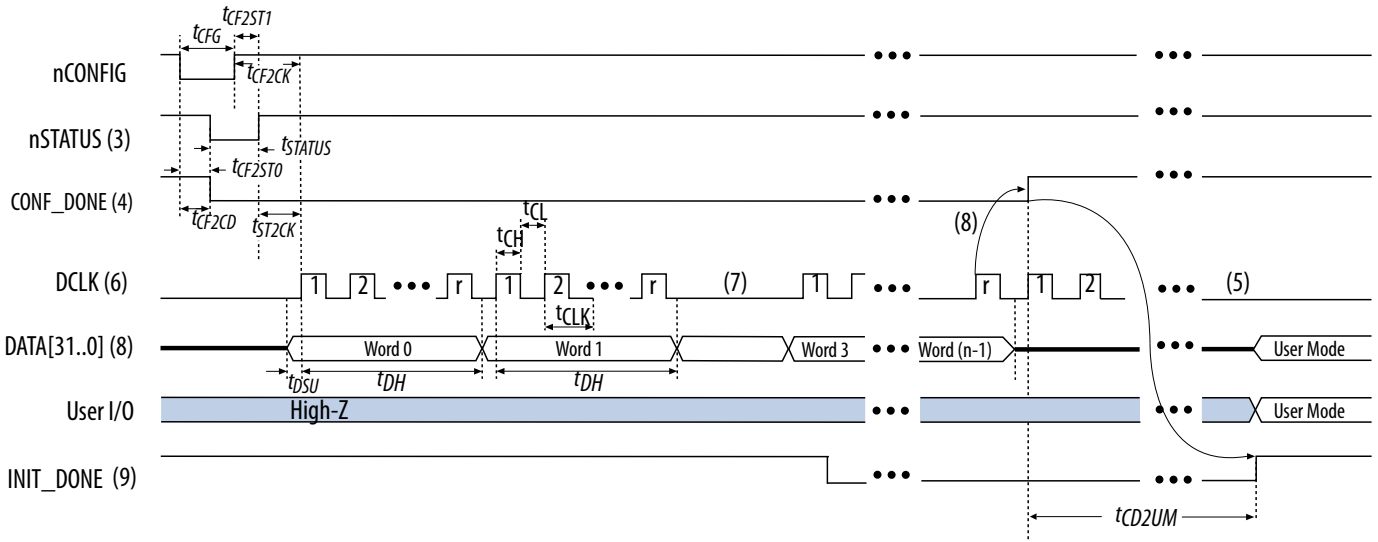


Notes:
1. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
2. After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.
3. After power-up, before and during configuration, CONF_DONE is low.
4. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
5. For FPP ×16, use DATA[15..0]. For FPP ×8, use DATA[7..0]. DATA[31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high when the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
7. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

FPP Configuration Timing when DCLK to DATA[] > 1

Figure 2-8: FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 ,

Timing when using a MAX II device, MAX V device, or microprocessor as an external host.



Notes:

1. To find out the DCLK-to-DATA[] ratio for your system, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
2. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
3. After power-up, the Arria V GZ device holds nSTATUS low for the time as specified by the POR delay.
4. After power-up, before and during configuration, CONF_DONE is low.
5. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
6. "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
7. If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31..0] pins prior to sending the first DCLK rising edge.
8. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
9. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (8576 × CLKUSR period) (215)	—	—

Related Information

- **DCLK-to-DATA[] Ratio (r) for FPP Configuration** on page 2-57
- **Configuration, Design Security, and Remote System Upgrades in Arria V Devices**

(215) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Table 2-60: PS Timing Parameters for Arria V GZ Devices

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1,506 (217)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 (218)	µs
t_{CF2CK} (219)	nCONFIG high to first rising edge on DCLK	1,506	—	µs
t_{ST2CK} (219)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode (220)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (8576 × CLKUSR period) (221)	—	—

(217) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(218) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.
(219) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.
(220) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

Date	Version	Changes

June 2016	2016.06.20	• Changed column heading from "Value" to "Maximum" in the "Pin Capacitance for Arria V GZ Devices" table.
		• Changed the minimum supported data rate range values from "1000" to "2000" in the "ATX PLL Specifications for Arria V GZ Devices" table.
		• Added the supported data rates for the following output standards using true LVDS output buffer types in the "High-Speed Clock Specifications for Arria V GZ Devices" table:
		  • True RSDS output standard: data rates of up to 230 Mbps
		  • True mini-LVDS output standard: data rates of up to 340 Mbps

December 2015	2015.12.16	• Removed the CDR ppm tolerance specification from the "Receiver Specifications for Arria V GZ Devices" table. • Removed transmitter rise and fall time specifications from the "Transmitter Specifications for Arria V GZ Devices" table. • Changed the .rbf sizes in the "Uncompressed .rbf Sizes for Arria V GZ Devices" table. • Added a footnote to the "Transmitter High-Speed I/O Specifications for Arria V GZ Devices" table.
June 2015	2015.06.16	• Changed the conditions for the reference clock rise and fall time and added a note to the condition in the "Reference Clock Specifications for Arria V GZ Devices" table. • Added a note to the "Minimum differential eye opening at receiver serial input pins" specification in the "Receiver Specifications for Arria V GZ Devices" table.
January 2015	2015.01.30	• Added 240-Ω to the "OCT Calibration Accuracy Specifications for Arria V GZ Devices" table. • Changed the CDR PPM tolerance spec in the "Receiver Specifications for Arria V GZ Devices" table. • Added additional max data rate for fPLL in the "Fractional PLL Specifications for Arria V GZ Devices" table.