Intel - 5AGXMA5G4F35I5N Datasheet





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Details

Product Status	Obsolete
Number of LABs/CLBs	8962
Number of Logic Elements/Cells	190000
Total RAM Bits	13284352
Number of I/O	544
Number of Gates	
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxma5g4f35i5n

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Arria V GX, GT, SX, and ST Device Datasheet



This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Arria® V devices.

Arria V devices are offered in commercial and industrial grades. Commercial devices are offered in -C4 (fastest), -C5, and -C6 speed grades. Industrial grade devices are offered in the -I3 and -I5 speed grades.

Related Information

Arria V Device Overview

Provides more information about the densities and packages of devices in the Arria V family.

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Arria V devices.

Operating Conditions

Arria V devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Arria V devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Arria V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms.

The functional operation of the device is not implied for these conditions.

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• Transceiver Specifications for Arria V GT and ST Devices on page 1-29 Provides the specifications for transmitter, receiver, and reference clock I/O pin.

Switching Characteristics

This section provides performance characteristics of Arria V core and periphery blocks.

Transceiver Performance Specifications

Transceiver Specifications for Arria V GX and SX Devices

Table 1-20: Reference Clock Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transc	Unit		
Symbol/Description	Condition	Min	Тур	Max	Min	Тур	Max	Onit
Supported I/O standards	1.2 V PCM	1.2 V PCML, 1.4 V PCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL ⁽²³⁾ , HCSL, and LVDS						
Input frequency from REFCLK input pins	—	27	—	710	27		710	MHz
Rise time	Measure at $\pm 60 \text{ mV of}$ differential signal ⁽²⁴⁾			400			400	ps
Fall time	Measure at $\pm 60 \text{ mV of}$ differential signal ⁽²⁴⁾	_		400	_		400	ps
Duty cycle	_	45	_	55	45	_	55	%
Peak-to-peak differential input voltage	—	200		300 ⁽²⁵⁾ / 2000	200	_	300 ⁽²⁵⁾ / 2000	mV



⁽²³⁾ Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

REFCLK performance requires to meet transmitter REFCLK phase noise specification. (24)

⁽²⁵⁾ The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain

Figure 1-2: Continuous Time-Linear Equalizer (CTLE) Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices



Arria V GX, GT, SX, and ST Device Datasheet

Altera Corporation



Symbol	Parameter	Condition	Min	Тур	Мах	Unit
£		-3 speed grade	5	—	800 ⁽⁶¹⁾	MHz
	Input clock fraguency	-4 speed grade	5		800 ⁽⁶¹⁾	MHz
IIN	input clock nequency	–5 speed grade	5	_	750 ⁽⁶¹⁾	MHz
		-6 speed grade	5		625(61)	MHz
f _{INPFD}	Integer input clock frequency to the phase frequency detector (PFD)	_	5	_	325	MHz
f _{fINPFD}	Fractional input clock frequency to the PFD		50	_	160	MHz
		-3 speed grade	600	—	1600	MHz
f (62)	PLL voltage-controlled oscillator (VCO) operating range	-4 speed grade	600	_	1600	MHz
IVCO		–5 speed grade	600		1600	MHz
		-6 speed grade	600		1300	MHz
t _{EINDUTY}	Input clock or external feedback clock input duty cycle	_	40		60	%
		-3 speed grade	_	_	500 ⁽⁶³⁾	MHz
f	Output frequency for internal global or	-4 speed grade	—	—	500 ⁽⁶³⁾	MHz
LOUT	regional clock	-5 speed grade	_	_	500 ⁽⁶³⁾	MHz
		-6 speed grade	_	_	400 ⁽⁶³⁾	MHz



⁽⁶¹⁾ This specification is limited in the Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

⁽⁶²⁾ The VCO frequency reported by the Quartus Prime software takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

⁽⁶³⁾ This specification is limited by the lower of the two: I/O f_{MAX} or F_{OUT} of the PLL.

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
		-3 speed grade			670 ⁽⁶³⁾	MHz
f	Output frequency for external clock	-4 speed grade	_	_	670 ⁽⁶³⁾	MHz
IOUT_EXT	output	–5 speed grade		_	622 ⁽⁶³⁾	MHz
		–6 speed grade			500(63)	MHz
t _{OUTDUTY}	Duty cycle for external clock output (when set to 50%)	_	45	50	55	%
t _{FCOMP}	External feedback clock compensation time	_	_		10	ns
t _{DYCONFIGCLK}	Dynamic configuration clock for mgmt_ clk and scanclk	_	_		100	MHz
t _{LOCK}	Time required to lock from end-of- device configuration or deassertion of areset	_	_	_	1	ms
t _{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	_			1	ms
		Low	_	0.3	_	MHz
f_{CLBW}	PLL closed-loop bandwidth	Medium	_	1.5	_	MHz
		High ⁽⁶⁴⁾		4		MHz
t _{PLL_PSERR}	Accuracy of PLL phase shift				±50	ps
t _{ARESET}	Minimum pulse width on the areset signal		10		_	ns
t(65)(66)	Input clock cycle_to_cycle iitter	$F_{REF} \ge 100 \text{ MHz}$			0.15	UI (p-p)
'INCCJ		$F_{REF} < 100 \text{ MHz}$			±750	ps (p-p)

⁽⁶⁴⁾ High bandwidth PLL settings are not supported in external feedback mode.



⁽⁶⁵⁾ A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

⁽⁶⁶⁾ F_{REF} is f_{IN}/N , specification applies when N = 1.

High-Speed I/O Specifications

Table 1-40: High-Speed I/O Specifications for Arria V Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block. When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

The Arria V devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 360 Mbps
- True mini-LVDS output standard with data rates of up to 400 Mbps

Symbol		Condition		-I3, -C4			–I5, –C5			-C6		Unit
		Condition	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
f _{HSCLK_in} (inp Differential I	out clock frequency) True /O Standards	Clock boost factor W = 1 to $40^{(72)}$	5		800	5		750	5	_	625	MHz
f _{HSCLK_in} (input clock frequency) Single-Ended I/O Standards ⁽⁷³⁾		Clock boost factor W = 1 to $40^{(72)}$	5		625	5		625	5		500	MHz
f _{HSCLK_in} (inp Single-Ended	out clock frequency) I I/O Standards ⁽⁷⁴⁾	Clock boost factor W = 1 to $40^{(72)}$	5	_	420	5	_	420	5	—	420	MHz
f _{HSCLK_OUT} (output clock frequency)		_	5	_	625(75)	5	_	625(75)	5		500 ⁽⁷⁵⁾	MHz
Transmitter	True Differential I/O Standards - f _{HSDR} (data rate)	SERDES factor J =3 to $10^{(76)}$	(77)		1250	(77)		1250	(77)		1050	Mbps

⁽⁷³⁾ This applies to DPA and soft-CDR modes only.





⁽⁷²⁾ Clock boost factor (W) is the ratio between the input data rate and the input clock rate.

⁽⁷⁴⁾ This applies to non-DPA mode only.

⁽⁷⁵⁾ This is achieved by using the LVDS clock network.

 $^{^{(76)}}$ The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

⁽⁷⁷⁾ The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

Figure 1-7: Timing Diagram for oe and dyn_term_ctrl Signals



Duty Cycle Distortion (DCD) Specifications

Table 1-47: Worst-Case DCD on Arria V I/O Pins

The output DCD cycle only applies to the I/O buffer. It does not cover the system DCD.

Symbol	-I3, -C4		-C5, -I5		-(6	Unit	
Symbol	Min	Max	Min	Max	Min	Max	Ont	
Output Duty Cycle	45	55	45	55	45	55	%	

HPS Specifications

This section provides HPS specifications and timing for Arria V devices.

For HPS reset, the minimum reset pulse widths for the HPS cold and warm reset signals (HPS_nRST and HPS_nPOR) are six clock cycles of HPS_CLK1.



Term	Definition
t _{FALL}	Signal high-to-low transition time (80–20%)
t _{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input
t _{outpj_io}	Period jitter on the GPIO driven by a PLL
t _{outpj_dc}	Period jitter on the dedicated clock output driven by a PLL
t _{RISE}	Signal low-to-high transition time (20–80%)
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = $1/(\text{Receiver Input Clock Frequency Multiplication Factor}) = t_C/w)$
V _{CM(DC)}	DC common mode input voltage.
V _{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.
V _{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
V _{DIF(AC)}	AC differential input voltage—Minimum AC input differential voltage required for switching.
V _{DIF(DC)}	DC differential input voltage— Minimum DC input differential voltage required for switching.
V _{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
V _{IH(AC)}	High-level AC input voltage
V _{IH(DC)}	High-level DC input voltage
V _{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
V _{IL(AC)}	Low-level AC input voltage
V _{IL(DC)}	Low-level DC input voltage
V _{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
V _{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter.
V _{SWING}	Differential input voltage
V _X	Input differential cross point voltage

Arria V GX, GT, SX, and ST Device Datasheet

Altera Corporation

1-100 Document Revision History

Date	Version	Changes
November 2012	3.0	 Updated Table 2, Table 4, Table 9, Table 14, Table 16, Table 17, Table 20, Table 21, Table 25, Table 29, Table 36, Table 56, Table 57, and Table 60. Removed table: Transceiver Block Jitter Specifications for Arria V Devices. Added HPS information: Added "HPS Specifications" section. Added Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, and Table 50. Added Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19. Updated Table 3 and Table 5.
October 2012	2.4	 Updated Arria V GX V_{CCR_GXBL/R}, V_{CCT_GXBL/R}, and V_{CCL_GXBL/R} minimum and maximum values, and data rate in Table 4. Added receiver V_{ICM} (AC coupled) and V_{ICM} (DC coupled) values, and transmitter V_{OCM} (AC coupled) and V_{OCM} (DC coupled) values in Table 20 and Table 21.
August 2012	2.3	Updated the SERDES factor condition in Table 30.
July 2012	2.2	 Updated the maximum voltage for V_I (DC input voltage) in Table 1. Updated Table 20 to include the Arria V GX -I3 speed grade. Updated the minimum value of the fixedclk clock frequency in Table 20 and Table 21. Updated the SERDES factor condition in Table 30. Updated Table 50 to include the IOE programmable delay settings for the Arria V GX -I3 speed grade.
June 2012	2.1	Updated V _{CCR_GXBL/R} , V _{CCT_GXBL/R} , and V _{CCL_GXBL/R} values in Table 4.





This document covers the electrical and switching characteristics for Arria V GZ devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, core, and periphery performance. This document also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

Related Information

Arria V Device Overview

For information regarding the densities and packages of devices in the Arria V GZ family.

Electrical Characteristics

Operating Conditions

When you use Arria V GZ devices, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Arria V GZ devices, you must consider the operating requirements described in this datasheet.

Arria V GZ devices are offered in commercial and industrial temperature grades.

Commercial devices are offered in -3 (fastest) and -4 core speed grades. Industrial devices are offered in -3L and -4 core speed grades. Arria V GZ devices are offered in -2 and -3 transceiver speed grades.

Table 2-1: Commercial and Industrial Speed Grade Offering for Arria V GZ Devices

C = Commercial temperature grade; I = Industrial temperature grade.

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2-28	Transmitter
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Sumbol/Description	Conditions	Trans	ceiver Spee	d Grade 2	Transc	Unit		
Symbol/Description	Conditions	Min	Тур	Мах	Min	Тур	Max	Onit
	85- Ω setting	—	85 ± 20%	_	_	85 ± 20%	—	Ω
Differential on-chip termination	100- Ω setting		100 ± 20%			100 ± 20%	_	Ω
resistors	120- Ω setting	—	120 ± 20%			120 ± 20%	_	Ω
	150-Ω setting	_	150 ± 20%			150 ± 20%	_	Ω
V _{OCM} (AC coupled)	0.65-V setting	—	650			650	_	mV
V _{OCM} (DC coupled)	_	—	650			650	—	mV
Intra-differential pair skew	Tx V _{CM} = 0.5 V and slew rate of 15 ps	_		15	_	_	15	ps
Intra-transceiver block transmitter channel-to-channel skew	x6 PMA bonded mode			120			120	ps
Inter-transceiver block transmitter channel-to-channel skew	xN PMA bonded mode			500			500	ps

Related Information

Arria V Device Overview

For more information about device ordering codes.



2-44 Periphery Performance

Description	Min	Тур	Мах	Unit
Diode ideality factor	1.006	1.008	1.010	—

Periphery Performance

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

Note: The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

High-Speed Clock Specifications

Table 2-39: High-Speed Clock Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

Arria V GZ devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 230 Mbps
- True mini-LVDS output standard with data rates of up to 340 Mbps



2-50 Soft CDR Mode High-Speed I/O Specifications

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽²⁰¹⁾	Maximum
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
	01010101	8	32	640 data transitions

Soft CDR Mode High-Speed I/O Specifications

Table 2-44: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions	C3, I3L			C4, I4			llait
		Min	Тур	Max	Min	Тур	Max	
Soft-CDR ppm tolerance	—	_	_	300			300	± ppm





⁽²⁰¹⁾ This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

FPP Configuration Timing when DCLK to DATA[] > 1

Figure 2-8: FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1,

t_{CF2ST1} tcfg ;↔ nCONFIG ŤĊF2CK nSTATUS (3) 🕳 tstatus tCF2ST0 CONF_DONE (4) TCL tCH tsT2CK ŤĊF2CD (8) DCLK (6) (7) 1 2 ••• r 2 ••• r 1 \mathbf{D} (5) tCLK DATA[31..0] (8) Word 0 Word User Mode Word 3 • • • Word (n-1) tDH tDH tpsy High-Z User I/O User Mode INIT DONE (9) tCD2UM

Timing when using a MAX II device, MAX V device, or microprocessor as an external host.

Notes:

- 1. To find out the DCLK-to-DATA[] ratio for your system, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
- 2. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- 3. After power-up, the Arria V GZ device holds nSTATUS low for the time as specified by the POR delay.
- 4. After power-up, before and during configuration, CONF_DONE is low.
- 5. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- 6. "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
- 7. If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31.0] pins prior to sending the first DCLK rising edge.
- 8. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- 9. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.





2-64 FPP Configuration Timing when DCLK to DATA[] > 1

Symbol	Parameter	Minimum	Maximum	Unit
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK}$ period	_	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (8576 × CLKUSR period) ⁽²¹⁵⁾		_

Related Information

- DCLK-to-DATA[] Ratio (r) for FPP Configuration on page 2-57
- Configuration, Design Security, and Remote System Upgrades in Arria V Devices





⁽²¹⁵⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Table 2-60: PS Timing Parameters for Arria V GZ Devices

Symbol	Parameter	Minimum	Maximum	Unit
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t _{CFG}	nCONFIG low pulse width	2		μs
t _{STATUS}	nSTATUS low pulse width	268	1,506 (217)	μs
t _{CF2ST1}	nCONFIG high to nSTATUS high		1,506 (218)	μs
t _{CF2CK} (219)	nCONFIG high to first rising edge on DCLK	1,506	—	μs
t _{ST2CK} (219)	nSTATUS high to first rising edge of DCLK	2		μs
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t _{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t _{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t _{CL}	DCLK low time	$0.45 imes 1/f_{ m MAX}$	—	S
t _{CLK}	DCLK period	1/f _{MAX}	—	s
f _{MAX}	DCLK frequency	_	125	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽²²⁰⁾	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK}$ period	_	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (8576 × CLKUSR period) (221)	_	_

⁽²¹⁷⁾ This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.



⁽²¹⁸⁾ This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

⁽²¹⁹⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

⁽²²⁰⁾ The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

Glossary

Table 2-68: Glossary





Term	Definition						
R _L	Receiver differential input discrete resistor (external to the Arria V GZ device).						
SW (sampling window)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:						
	Bit Time						
		0.5 x TCCS	RSKM	Sampling Window (SW)	RSKM	0.5 x TCCS	
Single-ended voltage referenced I/O standard	The JEDEC standard for SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing: Single-Ended Voltage Referenced I/O Standard						
	-	V _{0H}		V REF	Viн(DC Vil(DC)	V <u>ccio</u> VIH(AC) VIL(AC) VIL(AC)	



Date	Version	Changes
June 2016	2016.06.20	 Changed column heading from "Value" to "Maximum" in the "Pin Capacitance for Arria V GZ Devices" table. Changed the minimum supported data rate range values from "1000" to "2000" in the "ATX PLL Specifications for Arria V GZ Devices" table. Added the supported data rates for the following output standards using true LVDS output buffer types in the "High-Speed Clock Specifications for Arria V GZ Devices" table: True RSDS output standard: data rates of up to 230 Mbps True mini-LVDS output standard: data rates of up to 340 Mbps
December 2015	2015.12.16	 Removed the CDR ppm tolerance specification from the "Receiver Specifications for Arria V GZ Devices" table. Removed transmitter rise and fall time specifications from the "Transmitter Specifications for Arria V GZ Devices" table. Changed the .rbf sizes in the "Uncompressed .rbf Sizes for Arria V GZ Devices" table. Added a footnote to the "Transmitter High-Speed I/O Specifications for Arria V GZ Devices" table.
June 2015	2015.06.16	 Changed the conditions for the reference clock rise and fall time and added a note to the condition in the "Reference Clock Specifications for Arria V GZ Devices" table. Added a note to the "Minimum differential eye opening at receiver serial input pins" specification in the "Receiver Specifications for Arria V GZ Devices" table.
January 2015	2015.01.30	 Added 240-Ω to the "OCT Calibration Accuracy Specifications for Arria V GZ Devices" table. Changed the CDR PPM tolerance spec in the "Receiver Specifications for Arria V GZ Devices" table. Added additional max data rate for fPLL in the "Fractional PLL Specifications for Arria V GZ Devices" table.



Date	Version	Changes
July 2014	3.8	 Updated Table 21. Updated Table 22 V_{OCM} (DC Coupled) condition. Updated the DCLK note to Figure 6, Figure 7, and Figure 9. Added note to Table 5 and Table 6. Added the DCLK specification to Table 50. Added note to Table 51. Updated the list of parameters in Table 53.
February 2014	3.7	Updated Table 28.
December 2013	3.6	 Updated Table 2, Table 13, Table 18, Table 19, Table 22, Table 30, Table 33, Table 37, Table 38, Table 45, Table 46, Table 47, Table 56, Table 49. Updated "PLL Specifications".
August 2013	3.5	Updated Table 28.
August 2013	3.4	 Removed Preliminary tags for Table 2, Table 4, Table 5, Table 14, Table 27, Table 28, Table 29, Table 31, Table 32, Table 43, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, and Table 54. Updated Table 2 and Table 28.
June 2013	3.3	Updated Table 23, Table 28, Table 51, and Table 55.
May 2013	3.2	 Added Table 23. Updated Table 5, Table 22, Table 26, and Table 57. Updated Figure 6, Figure 7, Figure 8, and Figure 9.
March 2013	3.1	 Updated Table 2, Table 6, Table 7, Table 8, Table 19, Table 22, Table 26, Table 29, Table 52. Updated "Maximum Allowed Overshoot and Undershoot Voltage".
December 2012	3.0	Initial release.

