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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	11460
Number of Logic Elements/Cells	242000
Total RAM Bits	15470592
Number of I/O	336
Number of Gates	-
Voltage - Supply	1.12V ~ 1.18V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	672-BBGA, FCBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/5agxma7d4f27i3n">https://www.e-xfl.com/product-detail/intel/5agxma7d4f27i3n</a>

Symbol	Description	Condition	Minimum <sup>(1)</sup>	Typical	Maximum <sup>(1)</sup>	Unit
$V_{CC}$	Core voltage power supply	–C4, –I5, –C5, –C6	1.07	1.1	1.13	V
		–I3	1.12	1.15	1.18	V
$V_{CCP}$	Periphery circuitry, PCIe hard IP block, and transceiver PCS power supply	–C4, –I5, –C5, –C6	1.07	1.1	1.13	V
		–I3	1.12	1.15	1.18	V
$V_{CCPGM}$	Configuration pins power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
$V_{CC\_AUX}$	Auxiliary supply	—	2.375	2.5	2.625	V
$V_{CCBAT}^{(2)}$	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V
$V_{CCPD}^{(3)}$	I/O pre-driver power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V

<sup>(1)</sup> The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

<sup>(2)</sup> If you do not use the design security feature in Arria V devices, connect  $V_{CCBAT}$  to a 1.5-V, 2.5-V, or 3.0-V power supply. Arria V power-on reset (POR) circuitry monitors  $V_{CCBAT}$ . Arria V devices do not exit POR if  $V_{CCBAT}$  is not powered up.

<sup>(3)</sup>  $V_{CCPD}$  must be 2.5 V when  $V_{CCIO}$  is 2.5, 1.8, 1.5, 1.35, 1.25, or 1.2 V.  $V_{CCPD}$  must be 3.0 V when  $V_{CCIO}$  is 3.0 V.  $V_{CCPD}$  must be 3.3 V when  $V_{CCIO}$  is 3.3 V.

**Figure 1-1: Equation for OCT Variation Without Recalibration**

$$R_{OCT} = R_{SCAL} \left( 1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle \right)$$

The definitions for the equation are as follows:

- The  $R_{OCT}$  value calculated shows the range of OCT resistance with the variation of temperature and  $V_{CCIO}$ .
- $R_{SCAL}$  is the OCT resistance value at power-up.
- $\Delta T$  is the variation of temperature with respect to the temperature at power up.
- $\Delta V$  is the variation of voltage with respect to the  $V_{CCIO}$  at power up.
- $dR/dT$  is the percentage change of  $R_{SCAL}$  with temperature.
- $dR/dV$  is the percentage change of  $R_{SCAL}$  with voltage.

### OCT Variation after Power-Up Calibration

**Table 1-10: OCT Variation after Power-Up Calibration for Arria V Devices**

This table lists OCT variation with temperature and voltage after power-up calibration. The OCT variation is valid for a  $V_{CCIO}$  range of  $\pm 5\%$  and a temperature range of  $0^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

Symbol	Description	$V_{CCIO}$ (V)	Value	Unit
dR/dV	OCT variation with voltage without recalibration	3.0	0.100	%/mV
		2.5	0.100	
		1.8	0.100	
		1.5	0.100	
		1.35	0.150	
		1.25	0.150	
		1.2	0.150	

- [Transceiver Specifications for Arria V GT and ST Devices](#) on page 1-29  
Provides the specifications for transmitter, receiver, and reference clock I/O pin.

## Switching Characteristics

This section provides performance characteristics of Arria V core and periphery blocks.

### Transceiver Performance Specifications

#### Transceiver Specifications for Arria V GX and SX Devices

Table 1-20: Reference Clock Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported I/O standards	1.2 V PCML, 1.4 V PCML,1.5 V PCML, 2.5 V PCML, Differential LVPECL <sup>(23)</sup> , HCSL, and LVDS							
Input frequency from REFCLK input pins	—	27	—	710	27	—	710	MHz
Rise time	Measure at ±60 mV of differential signal <sup>(24)</sup>	—	—	400	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal <sup>(24)</sup>	—	—	400	—	—	400	ps
Duty cycle	—	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	300 <sup>(25)</sup> /2000	200	—	300 <sup>(25)</sup> /2000	mV

<sup>(23)</sup> Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

<sup>(24)</sup> REFCLK performance requires to meet transmitter REFCLK phase noise specification.

<sup>(25)</sup> The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Inter-transceiver block transmitter channel-to-channel skew <sup>(39)</sup>	×N PMA bonded mode	—	—	500	—	—	500	ps

Table 1-24: CMU PLL Specifications for Arria V GX and SX Devices

Symbol/Description	Transceiver Speed Grade 4		Transceiver Speed Grade 6		Unit
	Min	Max	Min	Max	
Supported data range	611	6553.6	611	3125	Mbps
fPLL supported data range	611	3125	611	3125	Mbps

Table 1-25: Transceiver-FPGA Fabric Interface Specifications for Arria V GX and SX Devices

Symbol/Description	Transceiver Speed Grade 4 and 6		Unit
	Min	Max	
Interface speed (single-width mode)	25	187.5	MHz
Interface speed (double-width mode)	25	163.84	MHz

**Related Information**

- [CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain](#) on page 1-35
- [CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain](#) on page 1-36
- [Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines](#)  
Provides more information about the power supply connection for different data rates.

<sup>(39)</sup> This specification is only applicable to channels on one side of the device across two transceiver banks.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Transmitter $\text{REFCLK}$ phase noise <sup>(43)</sup>	10 Hz	—	—	–50	dBc/Hz
	100 Hz	—	—	–80	dBc/Hz
	1 KHz	—	—	–110	dBc/Hz
	10 KHz	—	—	–120	dBc/Hz
	100 KHz	—	—	–120	dBc/Hz
	$\geq 1$ MHz	—	—	–130	dBc/Hz
$R_{\text{REF}}$	—	—	$2000 \pm 1\%$	—	$\Omega$

Table 1-27: Transceiver Clocks Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
$\text{fixedclk}$ clock frequency	PCIe Receiver Detect	—	125	—	MHz
Transceiver Reconfiguration Controller IP ( $\text{mgmt\_clk\_clk}$ ) clock frequency	—	75	—	125	MHz

Table 1-28: Receiver Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS				
Data rate (6-Gbps transceiver) <sup>(44)</sup>	—	611	—	6553.6	Mbps

<sup>(43)</sup> The transmitter  $\text{REFCLK}$  phase jitter is 30 ps p-p (5 ps RMS) with bit error rate (BER)  $10^{-12}$ , equivalent to 14 sigma.<sup>(44)</sup> To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Typical TX  $V_{OD}$  Setting for Arria V Transceiver Channels with termination of 100  $\Omega$ Table 1-32: Typical TX  $V_{OD}$  Setting for Arria V Transceiver Channels with termination of 100  $\Omega$ 

Symbol	$V_{OD}$ Setting <sup>(58)</sup>	$V_{OD}$ Value (mV)	$V_{OD}$ Setting <sup>(58)</sup>	$V_{OD}$ Value (mV)
$V_{OD}$ differential peak-to-peak typical	6 <sup>(59)</sup>	120	34	680
	7 <sup>(59)</sup>	140	35	700
	8 <sup>(59)</sup>	160	36	720
	9	180	37	740
	10	200	38	760
	11	220	39	780
	12	240	40	800
	13	260	41	820
	14	280	42	840
	15	300	43	860
	16	320	44	880
	17	340	45	900
	18	360	46	920
	19	380	47	940
	20	400	48	960
	21	420	49	980
	22	440	50	1000
	23	460	51	1020
	24	480	52	1040

<sup>(58)</sup> Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.<sup>(59)</sup> Only valid for data rates  $\leq 5$  Gbps.

For example, when  $V_{OD} = 800$  mV, the corresponding  $V_{OD}$  value setting is 40. The following conditions show that the 1st post tap pre-emphasis setting = 2 is valid:

- $|B| + |C| \leq 60 \rightarrow 40 + 2 = 42$
- $|B| - |C| > 5 \rightarrow 40 - 2 = 38$
- $(V_{MAX}/V_{MIN} - 1)\% < 600\% \rightarrow (42/38 - 1)\% = 10.52\%$

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Arria V HSSI HSPICE models.

**Table 1-33: Transmitter Pre-Emphasis Levels for Arria V Devices**

Quartus Prime 1st Post Tap Pre-Emphasis Setting	Quartus Prime $V_{OD}$ Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
0	0	0	0	0	0	0	0	dB
1	1.97	0.88	0.43	0.32	0.24	0.19	0.13	dB
2	3.58	1.67	0.95	0.76	0.61	0.5	0.41	dB
3	5.35	2.48	1.49	1.2	1	0.83	0.69	dB
4	7.27	3.31	2	1.63	1.36	1.14	0.96	dB
5	—	4.19	2.55	2.1	1.76	1.49	1.26	dB
6	—	5.08	3.11	2.56	2.17	1.83	1.56	dB
7	—	5.99	3.71	3.06	2.58	2.18	1.87	dB
8	—	6.92	4.22	3.47	2.93	2.48	2.11	dB
9	—	7.92	4.86	4	3.38	2.87	2.46	dB
10	—	9.04	5.46	4.51	3.79	3.23	2.77	dB
11	—	10.2	6.09	5.01	4.23	3.61	—	dB
12	—	11.56	6.74	5.51	4.68	3.97	—	dB
13	—	12.9	7.44	6.1	5.12	4.36	—	dB
14	—	14.44	8.12	6.64	5.57	4.76	—	dB
15	—	—	8.87	7.21	6.06	5.14	—	dB



Protocol	Sub-protocol	Data Rate (Mbps)
Common Public Radio Interface (CPRI)	CPRI E6LV	614.4
	CPRI E6HV	614.4
	CPRI E6LVII	614.4
	CPRI E12LV	1,228.8
	CPRI E12HV	1,228.8
	CPRI E12LVII	1,228.8
	CPRI E24LV	2,457.6
	CPRI E24LVII	2,457.6
	CPRI E30LV	3,072
	CPRI E30LVII	3,072
	CPRI E48LVII	4,915.2
	CPRI E60LVII	6,144
	CPRI E96LVIII <sup>(60)</sup>	9,830.4
Gbps Ethernet (GbE)	GbE 1250	1,250
OBSAI	OBSAI 768	768
	OBSAI 1536	1,536
	OBSAI 3072	3,072
	OBSAI 6144	6,144
Serial digital interface (SDI)	SDI 270 SD	270
	SDI 1485 HD	1,485
	SDI 2970 3G	2,970

<sup>(60)</sup> You can achieve compliance with TX channel restriction of one HSSI channel per six-channel transceiver bank.

## HPS Clock Performance

**Table 1-48: HPS Clock Performance for Arria V Devices**

Symbol/Description	–I3	–C4	–C5, –I5	–C6	Unit
mpu_base_clk (microprocessor unit clock)	1050	925	800	700	MHz
main_base_clk (L3/L4 interconnect clock)	400	400	400	350	MHz
h2f_user0_clk	100	100	100	100	MHz
h2f_user1_clk	100	100	100	100	MHz
h2f_user2_clk	200	200	200	160	MHz

## HPS PLL Specifications

### HPS PLL VCO Frequency Range

**Table 1-49: HPS PLL VCO Frequency Range for Arria V Devices**

Description	Speed Grade	Minimum	Maximum	Unit
VCO range	–C5, –I5, –C6	320	1,600	MHz
	–C4	320	1,850	MHz
	–I3	320	2,100	MHz

### HPS PLL Input Clock Range

The HPS PLL input clock range is 10 – 50 MHz. This clock range applies to both HPS\_CLK1 and HPS\_CLK2 inputs.

#### Related Information

#### [Clock Select, Booting and Configuration chapter](#)

Provides more information about the clock range for different values of clock select (CSEL).

## HPS PLL Input Jitter

Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate. The divide value (N) is the value programmed into the denominator field of the VCO register for each PLL. The PLL input reference clock is divided by this value. The range of the denominator is 1 to 64.

$$\text{Maximum input jitter} = \text{Input clock period} \times \text{Divide value (N)} \times 0.02$$

**Table 1-50: Examples of Maximum Input Jitter**

Input Reference Clock Period	Divide Value (N)	Maximum Jitter	Unit
40 ns	1	0.8	ns
40 ns	2	1.6	ns
40 ns	4	3.2	ns

## Quad SPI Flash Timing Characteristics

**Table 1-51: Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices**

Symbol	Description	Min	Typ	Max	Unit
$F_{\text{clk}}$	SCLK_OUT clock frequency (External clock)	—	—	108	MHz
$T_{\text{qspi\_clk}}$	QSPI_CLK clock period (Internal reference clock)	2.32	—	—	ns
$T_{\text{duty\_cycle}}$	SCLK_OUT duty cycle	45	—	55	%
$T_{\text{dssfrst}}$	Output delay QSPI_SS valid before first clock edge	—	1/2 cycle of SCLK_OUT	—	ns
$T_{\text{dsslst}}$	Output delay QSPI_SS valid after last clock edge	–1	—	1	ns
$T_{\text{dio}}$	I/O data output delay	–1	—	1	ns
$T_{\text{din\_start}}$	Input data valid start	—	—	$(2 + R_{\text{delay}}) \times T_{\text{qspi\_clk}} - 7.52^{(85)}$	ns

Symbol	Description	Min	Max	Unit
$T_h$	SPI MISO hold time	1	—	ns
$T_{\text{duty cycle}}$	SPI_CLK duty cycle	45	55	%
$T_{\text{dssfrst}}$	Output delay SPI_SS valid before first clock edge	8	—	ns
$T_{\text{dsslst}}$	Output delay SPI_SS valid after last clock edge	8	—	ns
$T_{\text{dio}}$	Master-out slave-in (MOSI) output delay	–1	1	ns

<sup>(86)</sup> This value is based on  $\text{rx\_sample\_dly} = 1$  and  $\text{spi\_m\_clk} = 120$  MHz.  $\text{spi\_m\_clk}$  is the internal clock that is used by SPI Master to derive its  $\text{SCLK\_OUT}$ . These timings are based on  $\text{rx\_sample\_dly}$  of 1. This delay can be adjusted as needed to accommodate slower response times from the slave. Note that a delay of 0 is not allowed. The setup time can be used as a reference starting point. It is very crucial to do a calibration to get the correct  $\text{rx\_sample\_dly}$  value because each SPI slave device may have different output delay and each application board may have different path delay. For more information about  $\text{rx\_sample\_delay}$ , refer to the SPI Controller chapter in the Hard Processor System Technical Reference Manual.

## HPS JTAG Timing Specifications

**Table 1-62: HPS JTAG Timing Parameters and Values for Arria V Devices**

Symbol	Description	Min	Max	Unit
$t_{JCP}$	TCK clock period	30	—	ns
$t_{JCH}$	TCK clock high time	14	—	ns
$t_{JCL}$	TCK clock low time	14	—	ns
$t_{JPSU}$ (TDI)	TDI JTAG port setup time	2	—	ns
$t_{JPSU}$ (TMS)	TMS JTAG port setup time	3	—	ns
$t_{JPH}$	JTAG port hold time	5	—	ns
$t_{JPCO}$	JTAG port clock to output	—	12 <sup>(90)</sup>	ns
$t_{JPZX}$	JTAG port high impedance to valid output	—	14 <sup>(90)</sup>	ns
$t_{JPXZ}$	JTAG port valid output to high impedance	—	14 <sup>(90)</sup>	ns

## Configuration Specifications

This section provides configuration specifications and timing for Arria V devices.

### POR Specifications

**Table 1-63: Fast and Standard POR Delay Specification for Arria V Devices**

POR Delay	Minimum	Maximum	Unit
Fast	4	12 <sup>(91)</sup>	ms

<sup>(90)</sup> A 1-ns adder is required for each  $V_{CCIO\_HPS}$  voltage step down from 3.0 V. For example,  $t_{JPCO}$  = 13 ns if  $V_{CCIO\_HPS}$  of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

<sup>(91)</sup> The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

Date	Version	Changes
November 2012	3.0	<ul style="list-style-type: none"> <li>Updated Table 2, Table 4, Table 9, Table 14, Table 16, Table 17, Table 20, Table 21, Table 25, Table 29, Table 36, Table 56, Table 57, and Table 60.</li> <li>Removed table: Transceiver Block Jitter Specifications for Arria V Devices.</li> <li>Added HPS information: <ul style="list-style-type: none"> <li>Added “HPS Specifications” section.</li> <li>Added Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, and Table 50.</li> <li>Added Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19.</li> <li>Updated Table 3 and Table 5.</li> </ul> </li> </ul>
October 2012	2.4	<ul style="list-style-type: none"> <li>Updated Arria V GX <math>V_{CCR\_GXBL/R}</math>, <math>V_{CCT\_GXBL/R}</math>, and <math>V_{CCL\_GXBL/R}</math> minimum and maximum values, and data rate in Table 4.</li> <li>Added receiver <math>V_{ICM}</math> (AC coupled) and <math>V_{ICM}</math> (DC coupled) values, and transmitter <math>V_{OCM}</math> (AC coupled) and <math>V_{OCM}</math> (DC coupled) values in Table 20 and Table 21.</li> </ul>
August 2012	2.3	Updated the SERDES factor condition in Table 30.
July 2012	2.2	<ul style="list-style-type: none"> <li>Updated the maximum voltage for <math>V_I</math> (DC input voltage) in Table 1.</li> <li>Updated Table 20 to include the Arria V GX -I3 speed grade.</li> <li>Updated the minimum value of the fixedclk clock frequency in Table 20 and Table 21.</li> <li>Updated the SERDES factor condition in Table 30.</li> <li>Updated Table 50 to include the IOE programmable delay settings for the Arria V GX -I3 speed grade.</li> </ul>
June 2012	2.1	Updated $V_{CCR\_GXBL/R}$ , $V_{CCT\_GXBL/R}$ , and $V_{CCL\_GXBL/R}$ values in Table 4.

## Transceiver Power Supply Requirements

Table 2-7: Transceiver Power Supply Voltage Requirements for Arria V GZ Devices

Conditions	VCCR_GXB and VCCT_GXB <sup>(122)</sup>	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true: <ul style="list-style-type: none"> <li>Data rate &gt; 10.3 Gbps.</li> <li>DFE is used.</li> </ul>	1.05	3.0	1.5	V
If ANY of the following conditions are true <sup>(123)</sup> : <ul style="list-style-type: none"> <li>ATX PLL is used.</li> <li>Data rate &gt; 6.5Gbps.</li> <li>DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used.</li> </ul>	1.0			
If ALL of the following conditions are true: <ul style="list-style-type: none"> <li>ATX PLL is not used.</li> <li>Data rate ≤ 6.5Gbps.</li> <li>DFE, AEQ, and EyeQ are not used.</li> </ul>	0.85	2.5		

## DC Characteristics

## Supply Current

Standby current is the current drawn from the respective power rails used for power budgeting.

Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

<sup>(122)</sup> If the VCCR\_GXB and VCCT\_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR\_GXB and VCCT\_GXB are set to 0.85 V, they can be shared with the VCC core supply.

<sup>(123)</sup> Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
fixedclk clock frequency	PCIe Receiver Detect	—	100 or 125	—	—	100 or 125	—	MHz
Reconfiguration clock (mgmt_clk_clk) frequency	—	100	—	125	100	—	125	MHz

**Related Information**[Arria V Device Overview](#)

For more information about device ordering codes.

**Receiver****Table 2-24: Receiver Specifications for Arria V GZ Devices**

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported I/O Standards	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS							
Data rate (Standard PCS) <sup>(143)</sup> , <sup>(144)</sup>	—	600	—	9900	600	—	8800	Mbps
Data rate (10G PCS) <sup>(143)</sup> , <sup>(144)</sup>	—	600	—	12500	600	—	10312.5	Mbps
Absolute V <sub>MAX</sub> for a receiver pin <sup>(145)</sup>	—	—	—	1.2	—	—	1.2	V
Absolute V <sub>MIN</sub> for a receiver pin	—	−0.4	—	—	−0.4	—	—	V

<sup>(143)</sup> The line data rate may be limited by PCS-FPGA interface speed grade.

<sup>(144)</sup> To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

<sup>(145)</sup> The device cannot tolerate prolonged operation at this absolute maximum.



## Core Performance Specifications

### Clock Tree Specifications

**Table 2-33: Clock Tree Performance for Arria V GZ Devices**

Symbol	Performance		Unit
	C3, I3L	C4, I4	
Global and Regional Clock	650	580	MHz
Periphery Clock	500	500	MHz

### PLL Specifications

**Table 2-34: PLL Specifications for Arria V GZ Devices**

Symbol	Parameter	Min	Typ	Max	Unit
$f_{IN}^{(167)}$	Input clock frequency (C3, I3L speed grade)	5	—	800	MHz
	Input clock frequency (C4, I4 speed grade)	5	—	650	MHz
$f_{INPFD}$	Input frequency to the PFD	5	—	325	MHz
$f_{FINPFD}$	Fractional Input clock frequency to the PFD	50	—	160	MHz
$f_{VCO}^{(168)}$	PLL VCO operating range (C3, I3L speed grade)	600	—	1600	MHz
	PLL VCO operating range (C4, I4 speed grade)	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%

<sup>(167)</sup> This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

<sup>(168)</sup> The VCO frequency reported by the Quartus II software in the **PLL Usage Summary** section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the  $f_{VCO}$  specification.

## DLL Range Specifications

**Table 2-47: DLL Range Specifications for Arria V GZ Devices**

Arria V GZ devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Parameter	C3, I3L	C4, I4	Unit
DLL operating frequency range	300 – 890	300 – 890	MHz

## DQS Logic Block Specifications

**Table 2-48: DQS Phase Offset Delay Per Setting for Arria V GZ Devices**

The typical value equals the average of the minimum and maximum values.

The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a –3 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is  $[625 \text{ ps} + (10 \times 11 \text{ ps}) \pm 20 \text{ ps}] = 735 \text{ ps} \pm 20 \text{ ps}$ .

Speed Grade	Min	Max	Unit
C3, I3L	8	15	ps
C4, I4	8	16	ps

**Table 2-49: DQS Phase Shift Error Specification for DLL-Delayed Clock ( $t_{\text{DQS\_PSERR}}$ ) for Arria V GZ Devices**

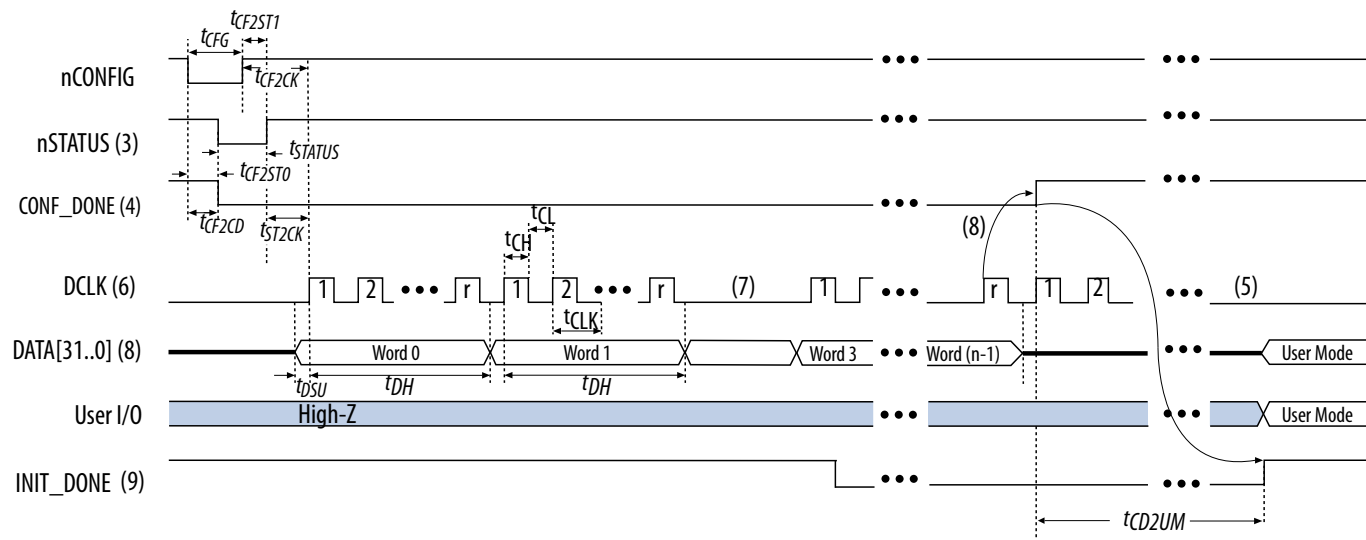
This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a –3 speed grade is  $\pm 84 \text{ ps}$  or  $\pm 42 \text{ ps}$ .

Number of DQS Delay Buffers	C3, I3L	C4, I4	Unit
1	30	32	ps
2	60	64	ps
3	90	96	ps

## FPP Configuration Timing when DCLK to DATA[] &gt; 1

Figure 2-8: FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is &gt;1 ,

Timing when using a MAX II device, MAX V device, or microprocessor as an external host.



## Notes:

1. To find out the DCLK-to-DATA[] ratio for your system, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
2. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF\_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
3. After power-up, the Arria V GZ device holds nSTATUS low for the time as specified by the POR delay.
4. After power-up, before and during configuration, CONF\_DONE is low.
5. Do not leave DCLK floating after configuration is complete. DCLK is ignored after configuration is complete. It can toggle high or low if required.
6. "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
7. If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31..0] pins prior to sending the first DCLK rising edge.
8. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF\_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF\_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
9. After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT\_DONE goes low.

Symbol	Parameter	Minimum	Maximum	Unit
$t_{CD2CU}$	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	—	—
$t_{CD2UMC}$	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (8576 \times \text{CLKUSR period})^{(215)}$	—	—

**Related Information**

- [DCLK-to-DATA\[\] Ratio \(r\) for FPP Configuration](#) on page 2-57
- [Configuration, Design Security, and Remote System Upgrades in Arria V Devices](#)

<sup>(215)</sup> To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the “Initialization” section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Term	Definition
$t_C$	High-speed receiver and transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
$t_{DUTY}$	High-speed I/O block—Duty cycle on the high-speed transmitter output clock.
$t_{FALL}$	Signal high-to-low transition time (80-20%)
$t_{INCCJ}$	Cycle-to-cycle jitter tolerance on the PLL clock input.
$t_{OUTPJ\_IO}$	Period jitter on the general purpose I/O driven by a PLL.
$t_{OUTPJ\_DC}$	Period jitter on the dedicated clock output driven by a PLL.
$t_{RISE}$	Signal low-to-high transition time (20-80%)
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. ( $TUI = 1/(\text{receiver input clock frequency multiplication factor}) = t_C/w$ )
$V_{CM(DC)}$	DC common mode input voltage.
$V_{ICM}$	Input common mode voltage—The common mode of the differential signal at the receiver.
$V_{ID}$	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
$V_{IH}$	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
$V_{IH(AC)}$	High-level AC input voltage
$V_{IH(DC)}$	High-level DC input voltage
$V_{IL}$	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{IL(AC)}$	Low-level AC input voltage
$V_{IL(DC)}$	Low-level DC input voltage