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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	11460
Number of Logic Elements/Cells	242000
Total RAM Bits	15470592
Number of I/O	336
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (Tj)
Package / Case	672-BBGA, FCBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxma7d6f27c6n



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Symbol	Description	Minimum ⁽⁵⁾	Typical	Maximum ⁽⁵⁾	Unit
V_{CCL_GXBL}	GX and SX speed grades—clock network power (left side)	1.08/1.12	1.1/1.15 ⁽⁶⁾	1.14/1.18	V
V_{CCL_GXBR}	GX and SX speed grades—clock network power (right side)				
V_{CCL_GXBL}	GT and ST speed grades—clock network power (left side)	1.17	1.20	1.23	V
V_{CCL_GXBR}	GT and ST speed grades—clock network power (right side)				

Related Information**Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines**

Provides more information about the power supply connection for different data rates.

HPS Power Supply Operating Conditions**Table 1-5: HPS Power Supply Operating Conditions for Arria V SX and ST Devices**

This table lists the steady-state voltage and current values expected from Arria V system-on-a-chip (SoC) devices with ARM®-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to Recommended Operating Conditions for Arria V Devices table for the steady-state voltage values expected from the FPGA portion of the Arria V SoC devices.

Symbol	Description	Condition	Minimum ⁽⁷⁾	Typical	Maximum ⁽⁷⁾	Unit
V_{CC_HPS}	HPS core voltage and periphery circuitry power supply	-C4, -I5, -C5, -C6	1.07	1.1	1.13	V
		-I3	1.12	1.15	1.18	V

⁽⁵⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁷⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

Table 1-16: Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Arria V Devices

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	$I_{OL}^{(14)}$ (mA)	$I_{OH}^{(14)}$ (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCIO} + 0.3$	$V_{REF} - 0.31$	$V_{REF} + 0.31$	$V_{TT} - 0.608$	$V_{TT} + 0.608$	8.1	-8.1
SSTL-2 Class II	-0.3	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$V_{CCIO} + 0.3$	$V_{REF} - 0.31$	$V_{REF} + 0.31$	$V_{TT} - 0.81$	$V_{TT} + 0.81$	16.2	-16.2
SSTL-18 Class I	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCIO} + 0.3$	$V_{REF} - 0.25$	$V_{REF} + 0.25$	$V_{TT} - 0.603$	$V_{TT} + 0.603$	6.7	-6.7
SSTL-18 Class II	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCIO} + 0.3$	$V_{REF} - 0.25$	$V_{REF} + 0.25$	0.28	$V_{CCIO} - 0.28$	13.4	-13.4
SSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	8	-8
SSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	16	-16
SSTL-135	—	$V_{REF} - 0.09$	$V_{REF} + 0.09$	—	$V_{REF} - 0.16$	$V_{REF} + 0.16$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	—	—
SSTL-125	—	$V_{REF} - 0.85$	$V_{REF} + 0.85$	—	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	—	—
HSTL-18 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-18 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8

⁽¹⁴⁾ To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
$t_{LTD_manual}^{(51)}$	—	4	—	—	μs
$t_{LTR_LTD_manual}^{(52)}$	—	15	—	—	μs
Programmable ppm detector ⁽⁵³⁾	—	$\pm 62.5, 100, 125, 200, 250, 300, 500,$ and 1000			ppm
Run length	—	—	—	200	UI
Programmable equalization AC and DC gain	AC gain setting = 0 to 3 ⁽⁵⁴⁾ DC gain setting = 0 to 1	Refer to CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices and CTLE Response at Data Rates \leq 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices diagrams.			

Table 1-29: Transmitter Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O standards	1.5 V PCML				
Data rate (6-Gbps transceiver)	—	611	—	6553.6	Mbps
Data rate (10-Gbps transceiver)	—	0.611	—	10.3125	Gbps
V_{OCM} (AC coupled)	—	—	650	—	mV
V_{OCM} (DC coupled)	≤ 3.2 Gbps ⁽⁴⁸⁾	670	700	730	mV

⁽⁵¹⁾ t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedto data` signal goes high when the CDR is functioning in the manual mode.

⁽⁵²⁾ $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedto ref` signal goes high when the CDR is functioning in the manual mode.

⁽⁵³⁾ The rate match FIFO supports only up to ± 300 ppm.

⁽⁵⁴⁾ The Quartus Prime software allows AC gain setting = 3 for design with data rate between 611 Mbps and 1.25 Gbps only.

DPA Lock Time Specifications

Figure 1-4: Dynamic Phase Alignment (DPA) Lock Time Specifications with DPA PLL Calibration Enabled

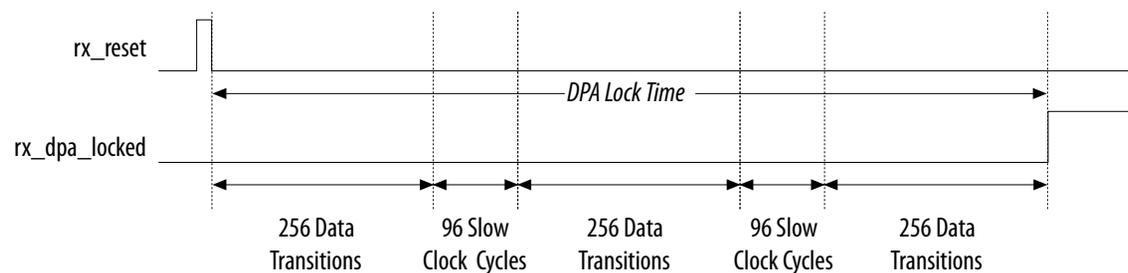


Table 1-41: DPA Lock Time Specifications for Arria V Devices

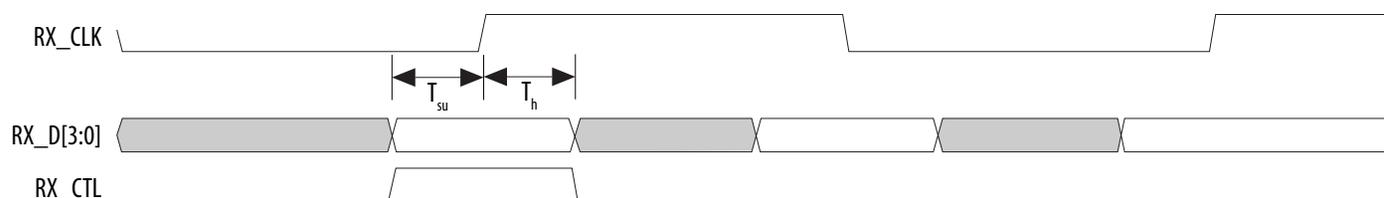
The specifications are applicable to both commercial and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽⁸⁴⁾	Maximum Data Transition
SPI-4	000000000111111111	2	128	640
Parallel Rapid I/O	00001111	2	128	640
	10010000	4	64	640
Miscellaneous	10101010	8	32	640
	01010101	8	32	640

⁽⁸⁴⁾ This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

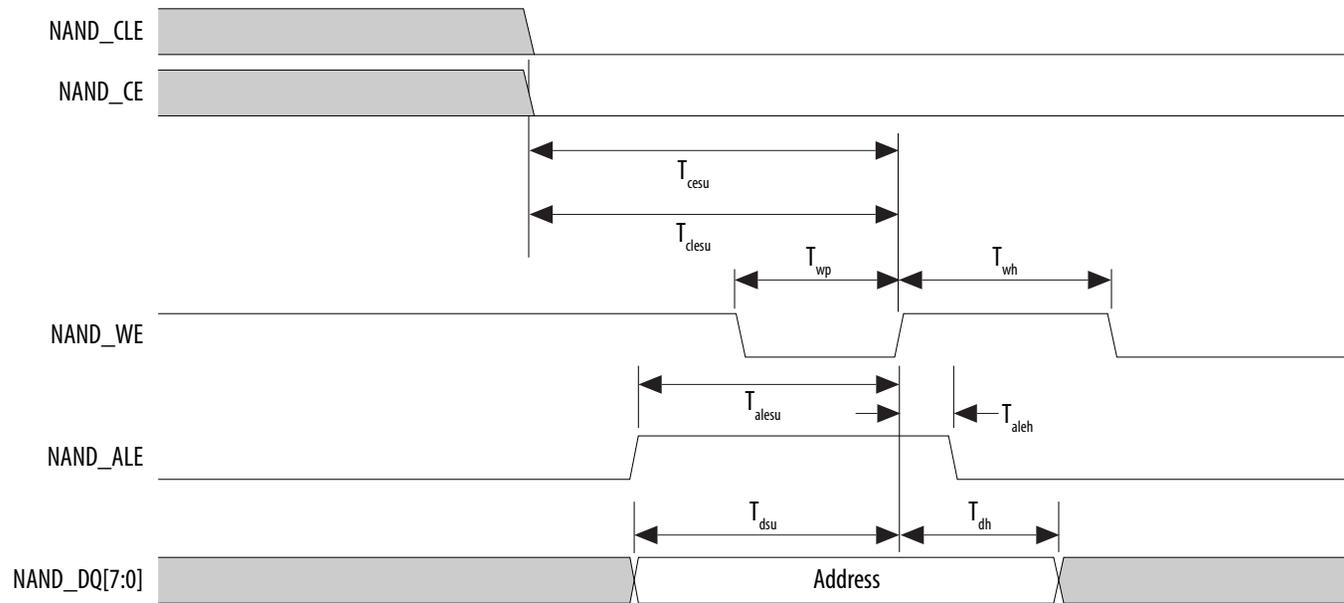
Table 1-57: RGMII RX Timing Requirements for Arria V Devices

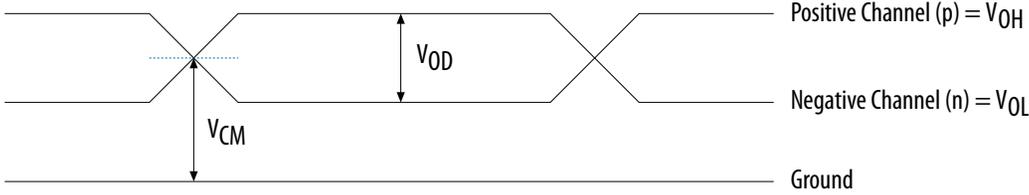
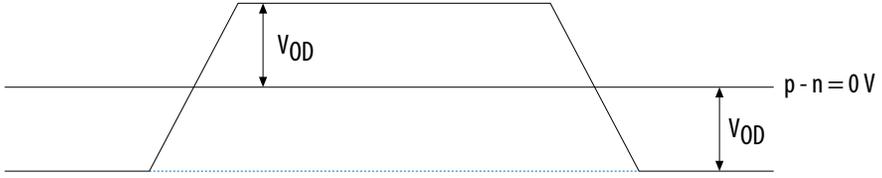
Symbol	Description	Min	Typ	Unit
T_{clk} (1000Base-T)	RX_CLK clock period	—	8	ns
T_{clk} (100Base-T)	RX_CLK clock period	—	40	ns
T_{clk} (10Base-T)	RX_CLK clock period	—	400	ns
T_{su}	RX_D/RX_CTL setup time	1	—	ns
T_h	RX_D/RX_CTL hold time	1	—	ns

Figure 1-14: RGMII RX Timing Diagram**Table 1-58: Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices**

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	MDC clock period	—	400	—	ns
T_d	MDC to MDIO output data delay	10	—	20	ns
T_s	Setup time for MDIO data	10	—	—	ns
T_h	Hold time for MDIO data	0	—	—	ns

Figure 1-18: NAND Address Latch Timing Diagram



Term	Definition
	<p>Transmitter Output Waveforms</p> <p>Single-Ended Waveform</p>  <p>Differential Waveform</p> 
f_{HCLK}	Left/right PLL input clock frequency.
f_{HSDR}	High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{\text{HSDR}} = 1/\text{TUI}$), non-DPA.
f_{HSDRDPA}	High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{\text{HSDRDPA}} = 1/\text{TUI}$), DPA.
J	High-speed I/O block—Deserialization factor (width of parallel data bus).

Date	Version	Changes
July 2014	3.8	<ul style="list-style-type: none"> • Added a note in Table 3, Table 4, and Table 5: The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements. • Updated V_{CC_HPS} specification in Table 5. • Added a note in Table 19: Differential inputs are powered by V_{CCPD} which requires 2.5 V. • Updated "Minimum differential eye opening at the receiver serial input pins" specification in Table 20 and Table 21. • Updated description in "HPS PLL Specifications" section. • Updated VCO range maximum specification in Table 39. • Updated T_d and T_h specifications in Table 45. • Added T_h specification in Table 47 and Figure 13. • Updated a note in Figure 20, Figure 21, and Figure 23 as follows: Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required. • Removed "Remote update only in AS mode" specification in Table 58. • Added DCLK device initialization clock source specification in Table 60. • Added description in "Configuration Files" section: The IOCSR .rbf size is specifically for the Configuration via Protocol (CvP) feature. • Removed $f_{MAX_RU_CLK}$ specification in Table 63.
February 2014	3.7	<ul style="list-style-type: none"> • Updated $V_{CCRSTCLK_HPS}$ maximum specification in Table 1. • Added $V_{CC_AUX_SHARED}$ specification in Table 1.
December 2013	3.6	<ul style="list-style-type: none"> • Added "HPS PLL Specifications". • Added Table 24, Table 39, and Table 40. • Updated Table 1, Table 3, Table 5, Table 19, Table 20, Table 21, Table 38, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, Table 51, Table 55, Table 56, and Table 59. • Updated Figure 7, Figure 13, Figure 15, Figure 16, and Figure 19. • Removed table: GPIO Pulse Width for Arria V Devices.

Symbol	Description	Condition	Minimum ⁽¹¹⁴⁾	Typical	Maximum ⁽¹¹⁴⁾	Unit
V _{CCPT}	Power supply for programmable power technology	—	1.45	1.50	1.55	V
V _{CC_AUX}	Auxiliary supply for the programmable power technology	—	2.375	2.5	2.625	V
V _{CCPD} ⁽¹¹⁶⁾	I/O pre-driver (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O pre-driver (2.5 V) power supply	—	2.375	2.5	2.625	V
V _{CCIO}	I/O buffers (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply	—	1.283	1.35	1.45	V
	I/O buffers (1.25 V) power supply	—	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	—	1.14	1.2	1.26	V
V _{CCPGM}	Configuration pins (3.0 V) power supply	—	2.85	3.0	3.15	V
	Configuration pins (2.5 V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V
V _{CCA_FPLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V _{CCD_FPLL}	PLL digital voltage regulator power supply	—	1.45	1.5	1.55	V
V _{CCBAT} ⁽¹¹⁷⁾	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V

⁽¹¹⁴⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹¹⁶⁾ V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V.

⁽¹¹⁷⁾ If you do not use the design security feature in Arria V GZ devices, connect V_{CCBAT} to a 1.2- to 3.0-V power supply. Arria V GZ power-on-reset (POR) circuitry monitors V_{CCBAT}. Arria V GZ devices do not exit POR if V_{CCBAT} is not powered up.

Symbol	Description	Conditions	Calibration Accuracy		Unit
			C3, I3L	C4, I4	
25-Ω R _S	Internal series termination with calibration (25-Ω setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%
50-Ω R _S	Internal series termination with calibration (50-Ω setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%
34-Ω and 40-Ω R _S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V _{CCIO} = 1.5, 1.35, 1.25, 1.2 V	±15	±15	%
48-Ω, 60-Ω, 80-Ω, and 240-Ω R _S	Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting)	V _{CCIO} = 1.2 V	±15	±15	%
50-Ω R _T	Internal parallel termination with calibration (50-Ω setting)	V _{CCIO} = 2.5, 1.8, 1.5, 1.2 V	-10 to +40	-10 to +40	%
20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω R _T	Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V _{CCIO} = 1.5, 1.35, 1.25 V	-10 to +40	-10 to +40	%
60-Ω and 120-Ω R _T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V _{CCIO} = 1.2	-10 to +40	-10 to +40	%
25-Ω R _{S_left_shift}	Internal left shift series termination with calibration (25-Ω R _{S_left_shift} setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%

Table 2-11: OCT Without Calibration Resistance Tolerance Specifications for Arria V GZ Devices

Symbol	Description	Conditions	Resistance Tolerance		Unit
			C3, I3L	C4, I4	
25-Ω R, 50-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCIO} = 3.0 and 2.5 V	±40	±40	%

CMU PLL

Table 2-26: CMU PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported data range	—	600	—	12500	600	—	10312.5	Mbps
$t_{\text{pll_powerdown}}^{(153)}$	—	1	—	—	1	—	—	μs
$t_{\text{pll_lock}}^{(154)}$	—	—	—	10	—	—	10	μs

Related Information

[Arria V Device Overview](#)

For more information about device ordering codes.

ATX PLL

Table 2-27: ATX PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

⁽¹⁵³⁾ $t_{\text{pll_powerdown}}$ is the PLL powerdown minimum pulse width.

⁽¹⁵⁴⁾ $t_{\text{pll_lock}}$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

Mode ⁽¹⁶⁴⁾	Transceiver Speed Grade	PMA Width	20	20	16	16	10	10	8	8
		PCS/Core Width	40	20	32	16	20	10	16	8
Register	2	C3, I3L core speed grade	9.9	9	7.92	7.2	4.9	4,5	3.92	3.6
	3	C4, I4 core speed grade	8.8	8.2	7.04	6.56	4.4	4.1	3.52	3.28

Related Information

[Operating Conditions](#) on page 2-1

10G PCS Data Rate

Table 2-31: 10G PCS Approximate Maximum Data Rate (Gbps) for Arria V GZ Devices

Mode ⁽¹⁶⁵⁾	Transceiver Speed Grade	PMA Width	64	40	40	40	32	32
		PCS Width	64	66/67	50	40	64/66/67	32
FIFO	2	C3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88
	3	C4, I4 core speed grade	10.3125	10.3125	10.69	10.3125	9.92	9.92
Register	2	C3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88
	3	C4, I4 core speed grade	10.3125	10.3125	10.69	10.3125	9.92	9.92

⁽¹⁶⁴⁾ The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

⁽¹⁶⁵⁾ The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
$t_{x \text{ Jitter}}$ - True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	UI
$t_{x \text{ Jitter}}$ - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	300	—	—	325	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.2	—	—	0.25	UI
t_{DUTY}	Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	%
t_{RISE} & t_{FALL}	True Differential I/O Standards	—	—	200	—	—	200	ps
	Emulated Differential I/O Standards with three external output resistor networks	—	—	250	—	—	300	ps
TCCS	True Differential I/O Standards	—	—	150	—	—	150	ps
	Emulated Differential I/O Standards	—	—	300	—	—	300	ps

Receiver High-Speed I/O Specifications

Table 2-41: Receiver High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Number of DQS Delay Buffers	C3, I3L	C4, I4	Unit
4	120	128	ps

Memory Output Clock Jitter Specifications

Table 2-50: Memory Output Clock Jitter Specification for Arria V GZ Devices

The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

Clock Network	Parameter	Symbol	C3, I3L		C4, I4		Unit
			Min	Max	Min	Max	
Regional	Clock period jitter	$t_{JIT(per)}$	-55	55	-55	55	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	-110	110	-110	110	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-82.5	82.5	-82.5	82.5	ps
Global	Clock period jitter	$t_{JIT(per)}$	-82.5	82.5	-82.5	82.5	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	-165	165	-165	165	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-90	90	-90	90	ps
PHY Clock	Clock period jitter	$t_{JIT(per)}$	-30	30	-35	35	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	-60	60	-70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-45	45	-56	56	ps

Symbol	Parameter	Minimum	Maximum	Unit
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times$ maximum DCLK period	—	—
t_{CD2UM} C	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} +$ ($8576 \times$ CLKUSR period) (209)	—	—

Related Information

- [DCLK-to-DATA\[\] Ratio \(r\) for FPP Configuration](#) on page 2-57
- [Configuration, Design Security, and Remote System Upgrades in Arria V Devices](#)

⁽²⁰⁸⁾ The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

⁽²⁰⁹⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the “Initialization” section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Table 2-57: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	μ s
t_{STATUS}	nSTATUS low pulse width	268	1,506 ⁽²¹⁰⁾	μ s
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽²¹¹⁾	μ s
t_{CF2CK} ⁽²¹²⁾	nCONFIG high to first rising edge on DCLK	1,506	—	μ s
t_{ST2CK} ⁽²¹²⁾	nSTATUS high to first rising edge of DCLK	2	—	μ s
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N-1/f_{DCLK}$ ⁽²¹³⁾	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP $\times 8/\times 16$)	—	125	MHz
	DCLK frequency (FPP $\times 32$)	—	100	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode ⁽²¹⁴⁾	175	437	μ s

⁽²¹⁰⁾ You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

⁽²¹¹⁾ You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

⁽²¹²⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

⁽²¹³⁾ N is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.

⁽²¹⁴⁾ The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

Table 2-60: PS Timing Parameters for Arria V GZ Devices

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	μ s
t_{STATUS}	nSTATUS low pulse width	268	1,506 ⁽²¹⁷⁾	μ s
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽²¹⁸⁾	μ s
t_{CF2CK} ⁽²¹⁹⁾	nCONFIG high to first rising edge on DCLK	1,506	—	μ s
t_{ST2CK} ⁽²¹⁹⁾	nSTATUS high to first rising edge of DCLK	2	—	μ s
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode ⁽²²⁰⁾	175	437	μ s
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (8576 \times \text{CLKUSR period})$ ⁽²²¹⁾	—	—

⁽²¹⁷⁾ This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

⁽²¹⁸⁾ This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

⁽²¹⁹⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

⁽²²⁰⁾ The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

Related Information

- [Configuration, Design Security, and Remote System Upgrades in Arria V Devices](#)
For more information about the reconfiguration input for the ALTREMOTE_UPDATE IP core, refer to the “User Watchdog Timer” section.
- [Configuration, Design Security, and Remote System Upgrades in Arria V Devices](#)
For more information about the `reset_timer` input for the ALTREMOTE_UPDATE IP core, refer to the “Remote System Upgrade State Machine” section.

User Watchdog Internal Oscillator Frequency Specification

Table 2-65: User Watchdog Internal Oscillator Frequency Specifications

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

[Arria V Devices Documentation page](#)

For the Excel-based I/O Timing spreadsheet

⁽²²⁶⁾ This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification. For more information, refer to the “Remote System Upgrade State Machine” section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

⁽²²⁷⁾ This is equivalent to strobing the `reset_timer` input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification. For more information, refer to the “User Watchdog Timer” section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Date	Version	Changes
July 2014	3.8	<ul style="list-style-type: none"> Updated Table 21. Updated Table 22 V_{OCM} (DC Coupled) condition. Updated the DCLK note to Figure 6, Figure 7, and Figure 9. Added note to Table 5 and Table 6. Added the DCLK specification to Table 50. Added note to Table 51. Updated the list of parameters in Table 53.
February 2014	3.7	Updated Table 28.
December 2013	3.6	<ul style="list-style-type: none"> Updated Table 2, Table 13, Table 18, Table 19, Table 22, Table 30, Table 33, Table 37, Table 38, Table 45, Table 46, Table 47, Table 56, Table 49. Updated “PLL Specifications”.
August 2013	3.5	Updated Table 28.
August 2013	3.4	<ul style="list-style-type: none"> Removed Preliminary tags for Table 2, Table 4, Table 5, Table 14, Table 27, Table 28, Table 29, Table 31, Table 32, Table 43, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, and Table 54. Updated Table 2 and Table 28.
June 2013	3.3	Updated Table 23, Table 28, Table 51, and Table 55.
May 2013	3.2	<ul style="list-style-type: none"> Added Table 23. Updated Table 5, Table 22, Table 26, and Table 57. Updated Figure 6, Figure 7, Figure 8, and Figure 9.
March 2013	3.1	<ul style="list-style-type: none"> Updated Table 2, Table 6, Table 7, Table 8, Table 19, Table 22, Table 26, Table 29, Table 52. Updated “Maximum Allowed Overshoot and Undershoot Voltage”.
December 2012	3.0	Initial release.