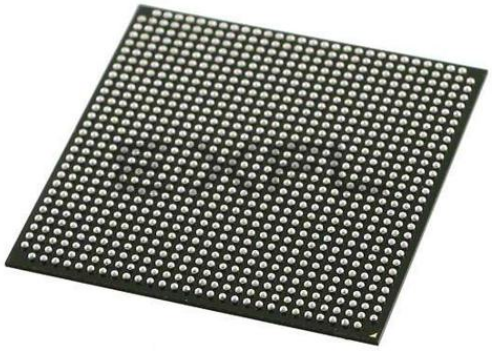

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 11460 |
| Number of Logic Elements/Cells | 242000 |
| Total RAM Bits | 15470592 |
| Number of I/O | 384 |
| Number of Gates | - |
| Voltage - Supply | 1.12V ~ 1.18V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 896-BBGA, FCBGA |
| Supplier Device Package | 896-FBGA (31x31) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5agxma7g4f31i3n |

## I/O Pin Leakage Current

### Table 1-6: I/O Pin Leakage Current for Arria V Devices

| Symbol | Description | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input pin | $V_I$ = 0 V to $V_{CCIOMAX}$ | –30 | — | 30 | µA |
| $I_{OZ}$ | Tri-stated I/O pin | $V_O$ = 0 V to $V_{CCIOMAX}$ | –30 | — | 30 | µA |

## Bus Hold Specifications

### Table 1-7: Bus Hold Parameters for Arria V Devices

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

| Parameter | Symbol | Condition | $V_{CCIO}$ (V) | | | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | 3.3 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus-hold, low, sustaining current | $I_{SUSL}$ | $V_{IN} > V_{IL}$ (max) | 8 | — | 12 | — | 30 | — | 50 | — | 70 | — | 70 | — | µA |
| Bus-hold, high, sustaining current | $I_{SUSH}$ | $V_{IN} < V_{IH}$ (min) | –8 | — | –12 | — | –30 | — | –50 | — | –70 | — | –70 | — | µA |
| Bus-hold, low, overdrive current | $I_{ODL}$ | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | 125 | — | 175 | — | 200 | — | 300 | — | 500 | — | 500 | µA |
| Bus-hold, high, overdrive current | $I_{ODH}$ | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | –125 | — | –175 | — | –200 | — | –300 | — | –500 | — | –500 | µA |

**Table 1-31: Transceiver-FPGA Fabric Interface Specifications for Arria V GT and ST Devices**

| Symbol/Description | Transceiver Speed Grade 3 | | Unit |
|---|---|---|---|
| | Min | Max | |
| Interface speed (PMA direct mode) | 50 | 153.6[56], 161[57] | MHz |
| Interface speed (single-width mode) | 25 | 187.5 | MHz |
| Interface speed (double-width mode) | 25 | 163.84 | MHz |

**Related Information**

- **CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain** on page 1-35
- **CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain** on page 1-36

[56] The maximum frequency when core transceiver local routing is selected.
[57] The maximum frequency when core transceiver network routing (GCLK, RCLK, or PCLK) is selected.

| Symbol | $V_{OD}$ Setting[58] | $V_{OD}$ Value (mV) | $V_{OD}$ Setting[58] | $V_{OD}$ Value (mV) |
|---|---|---|---|---|
| | 25 | 500 | 53 | 1060 |
| | 26 | 520 | 54 | 1080 |
| | 27 | 540 | 55 | 1100 |
| | 28 | 560 | 56 | 1120 |
| | 29 | 580 | 57 | 1140 |
| | 30 | 600 | 58 | 1160 |
| | 31 | 620 | 59 | 1180 |
| | 32 | 640 | 60 | 1200 |
| | 33 | 660 | | |

## Transmitter Pre-Emphasis Levels

The following table lists the simulation data on the transmitter pre-emphasis levels in dB for the first post tap under the following conditions:

- Low-frequency data pattern—five 1s and five 0s
- Data rate—2.5 Gbps

The levels listed are a representation of possible pre-emphasis levels under the specified conditions only and the pre-emphasis levels may change with data pattern and data rate.

Arria V devices only support 1st post tap pre-emphasis with the following conditions:

- The 1st post tap pre-emphasis settings must satisfy $|B| + |C| \leq 60$ where $|B| = V_{OD}$ setting with termination value, $R_{TERM} = 100\ \Omega$ and $|C|$ = 1st post tap pre-emphasis setting.
- $|B| - |C| > 5$ for data rates < 5 Gbps and $|B| - |C| > 8.25$ for data rates > 5 Gbps.
- $(V_{MAX}/V_{MIN} - 1)\% < 600\%$, where $V_{MAX} = |B| + |C|$ and $V_{MIN} = |B| - |C|$.

Exception for PCIe Gen2 design: $V_{OD}$ setting = 43 and pre-emphasis setting = 19 are allowed for PCIe Gen2 design with transmit de-emphasis – 6dB setting (`pipe_txdeemp` = 1'b0) using Altera PCIe Hard IP and PIPE IP cores.

[58] Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

For example, when $V_{OD}$ = 800 mV, the corresponding $V_{OD}$ value setting is 40. The following conditions show that the 1st post tap pre-emphasis setting = 2 is valid:

- $|B| + |C| \leq 60 \rightarrow 40 + 2 = 42$
- $|B| - |C| > 5 \rightarrow 40 - 2 = 38$
- $(V_{MAX}/V_{MIN} - 1)\% < 600\% \rightarrow (42/38 - 1)\% = 10.52\%$

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Arria V HSSI HSPICE models.

**Table 1-33: Transmitter Pre-Emphasis Levels for Arria V Devices**

| Quartus Prime 1st Post Tap Pre-Emphasis Setting | Quartus Prime $V_{OD}$ Setting | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | 10 (200 mV) | 20 (400 mV) | 30 (600 mV) | 35 (700 mV) | 40 (800 mV) | 45 (900 mV) | 50 (1000 mV) | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | dB |
| 1 | 1.97 | 0.88 | 0.43 | 0.32 | 0.24 | 0.19 | 0.13 | dB |
| 2 | 3.58 | 1.67 | 0.95 | 0.76 | 0.61 | 0.5 | 0.41 | dB |
| 3 | 5.35 | 2.48 | 1.49 | 1.2 | 1 | 0.83 | 0.69 | dB |
| 4 | 7.27 | 3.31 | 2 | 1.63 | 1.36 | 1.14 | 0.96 | dB |
| 5 | — | 4.19 | 2.55 | 2.1 | 1.76 | 1.49 | 1.26 | dB |
| 6 | — | 5.08 | 3.11 | 2.56 | 2.17 | 1.83 | 1.56 | dB |
| 7 | — | 5.99 | 3.71 | 3.06 | 2.58 | 2.18 | 1.87 | dB |
| 8 | — | 6.92 | 4.22 | 3.47 | 2.93 | 2.48 | 2.11 | dB |
| 9 | — | 7.92 | 4.86 | 4 | 3.38 | 2.87 | 2.46 | dB |
| 10 | — | 9.04 | 5.46 | 4.51 | 3.79 | 3.23 | 2.77 | dB |
| 11 | — | 10.2 | 6.09 | 5.01 | 4.23 | 3.61 | — | dB |
| 12 | — | 11.56 | 6.74 | 5.51 | 4.68 | 3.97 | — | dB |
| 13 | — | 12.9 | 7.44 | 6.1 | 5.12 | 4.36 | — | dB |
| 14 | — | 14.44 | 8.12 | 6.64 | 5.57 | 4.76 | — | dB |
| 15 | — | — | 8.87 | 7.21 | 6.06 | 5.14 | — | dB |

| Quartus Prime 1st Post Tap Pre-Emphasis Setting | Quartus Prime $V_{OD}$ Setting | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | 10 (200 mV) | 20 (400 mV) | 30 (600 mV) | 35 (700 mV) | 40 (800 mV) | 45 (900 mV) | 50 (1000 mV) | |
| 16 | — | — | 9.56 | 7.73 | 6.49 | — | — | dB |
| 17 | — | — | 10.43 | 8.39 | 7.02 | — | — | dB |
| 18 | — | — | 11.23 | 9.03 | 7.52 | — | — | dB |
| 19 | — | — | 12.18 | 9.7 | 8.02 | — | — | dB |
| 20 | — | — | 13.17 | 10.34 | 8.59 | — | — | dB |
| 21 | — | — | 14.2 | 11.1 | — | — | — | dB |
| 22 | — | — | 15.38 | 11.87 | — | — | — | dB |
| 23 | — | — | — | 12.67 | — | — | — | dB |
| 24 | — | — | — | 13.48 | — | — | — | dB |
| 25 | — | — | — | 14.37 | — | — | — | dB |
| 26 | — | — | — | — | — | — | — | dB |
| 27 | — | — | — | — | — | — | — | dB |
| 28 | — | — | — | — | — | — | — | dB |
| 29 | — | — | — | — | — | — | — | dB |
| 30 | — | — | — | — | — | — | — | dB |
| 31 | — | — | — | — | — | — | — | dB |

**Related Information**

**SPICE Models for Altera Devices**
Provides the Arria V HSSI HSPICE models.

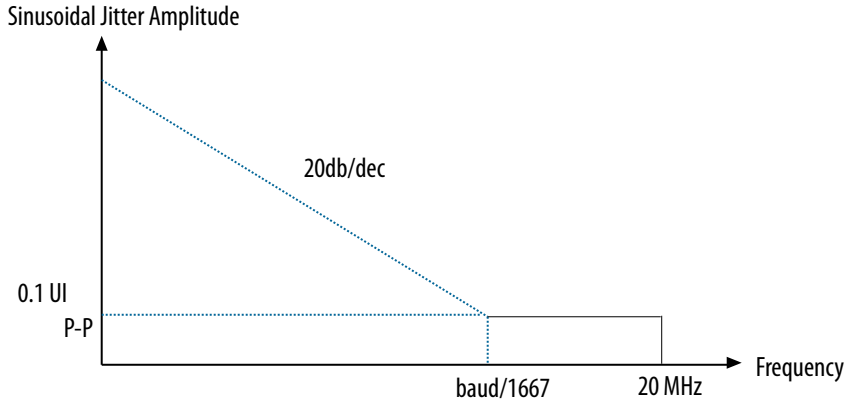
## Transceiver Compliance Specification

The following table lists the physical medium attachment (PMA) specification compliance of all supported protocol for Arria V GX, GT, SX, and ST devices. For more information about the protocol parameter details and compliance specifications, contact your Altera Sales Representative.

**Table 1-34: Transceiver Compliance Specification for All Supported Protocol for Arria V GX, GT, SX, and ST Devices**

| Protocol | Sub-protocol | Data Rate (Mbps) |
|---|---|---|
| PCIe | PCIe Gen1 | 2,500 |
| | PCIe Gen2 | 5,000 |
| | PCIe Cable | 2,500 |
| XAUI | XAUI 2135 | 3,125 |
| Serial RapidIO® (SRIO) | SRIO 1250 SR | 1,250 |
| | SRIO 1250 LR | 1,250 |
| | SRIO 2500 SR | 2,500 |
| | SRIO 2500 LR | 2,500 |
| | SRIO 3125 SR | 3,125 |
| | SRIO 3125 LR | 3,125 |
| | SRIO 5000 SR | 5,000 |
| | SRIO 5000 MR | 5,000 |
| | SRIO 5000 LR | 5,000 |
| | SRIO_6250_SR | 6,250 |
| | SRIO_6250_MR | 6,250 |
| | SRIO_6250_LR | 6,250 |

**Figure 1-6: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Less than 1.25 Gbps**




## DLL Frequency Range Specifications

**Table 1-43: DLL Frequency Range Specifications for Arria V Devices**

| Parameter | –I3, –C4 | –I5, –C5 | –C6 | Unit |
|---|---|---|---|---|
| DLL operating frequency range | 200 – 667 | 200 – 667 | 200 – 667 | MHz |

## DQS Logic Block Specifications

**Table 1-44: DQS Phase Shift Error Specifications for DLL-Delayed Clock ($t_{DQS\_PSERR}$) for Arria V Devices**

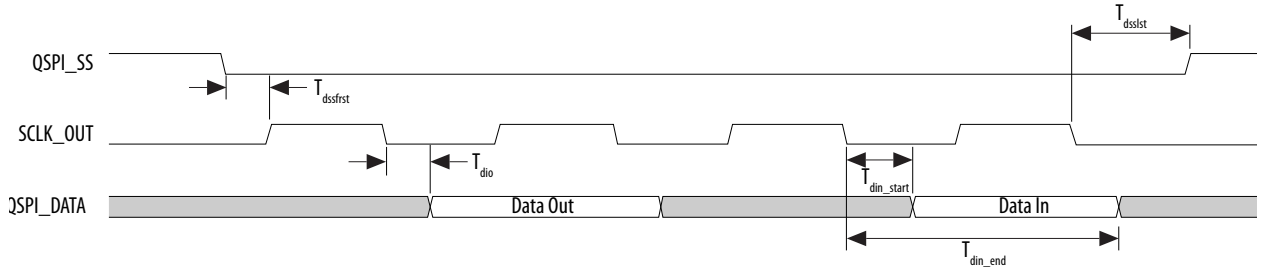
This error specification is the absolute maximum and minimum error.

| Number of DQS Delay Buffer | –I3, –C4 | –I5, –C5 | –C6 | Unit |
|---|---|---|---|---|
| 2 | 40 | 80 | 80 | ps |

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{din\_end}$ | Input data valid end | $(2 + R_{delay}) \times T_{qspi\_clk} - 1.21$ (85) | — | — | ns |

### Figure 1-8: Quad SPI Flash Timing Diagram

This timing diagram illustrates clock polarity mode 0 and clock phase mode 0.




**Related Information**

**Quad SPI Flash Controller Chapter, Arria V Hard Processor System Technical Reference Manual**
Provides more information about Rdelay.

## SPI Timing Characteristics

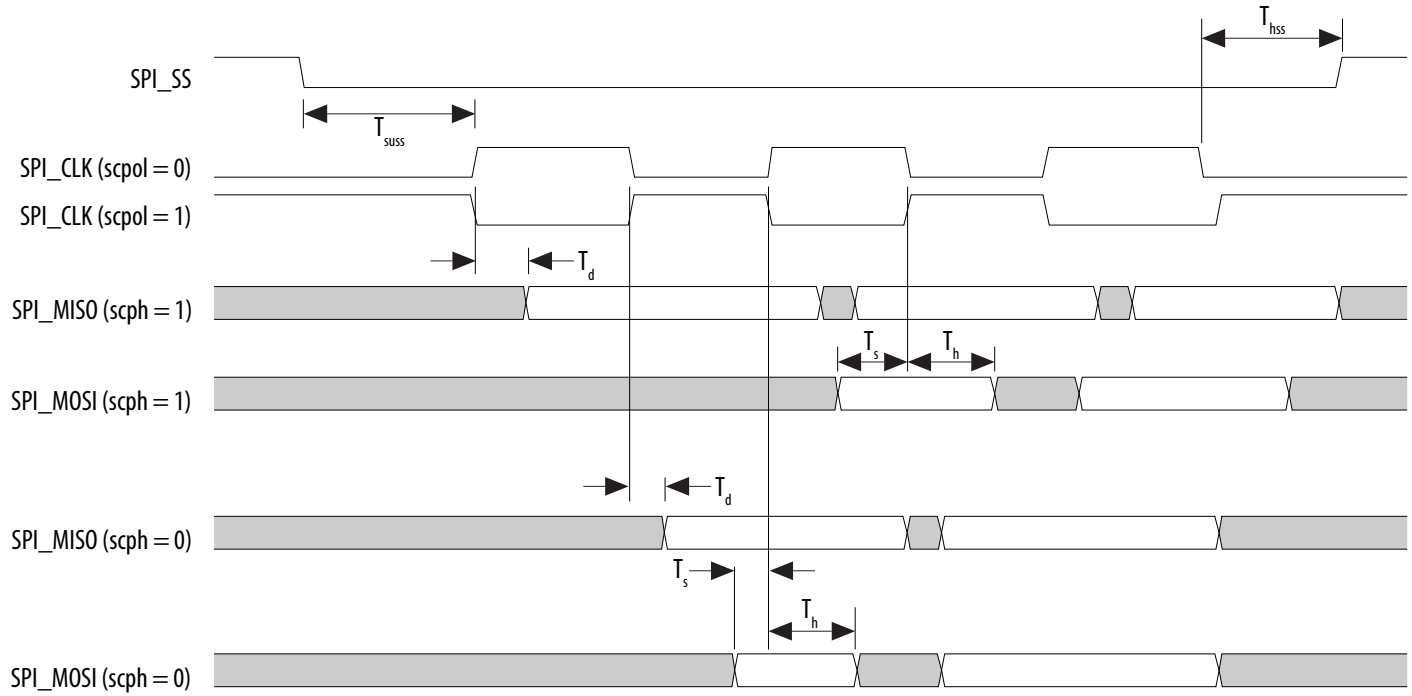
### Table 1-52: SPI Master Timing Requirements for Arria V Devices

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $T_{clk}$ | CLK clock period | 16.67 | — | ns |
| $T_{su}$ | SPI Master-in slave-out (MISO) setup time | 8.35 (86) | — | ns |

(85) $R_{delay}$ is set by programming the register `qspiregs.rddatacap`. For the SoC EDS software version 13.1 and later, Altera provides automatic Quad SPI calibration in the preloader. For more information about $R_{delay}$, refer to the Quad SPI Flash Controller chapter in the Arria V Hard Processor System Technical Reference Manual.

**Figure 1-10: SPI Slave Timing Diagram**




**Related Information**

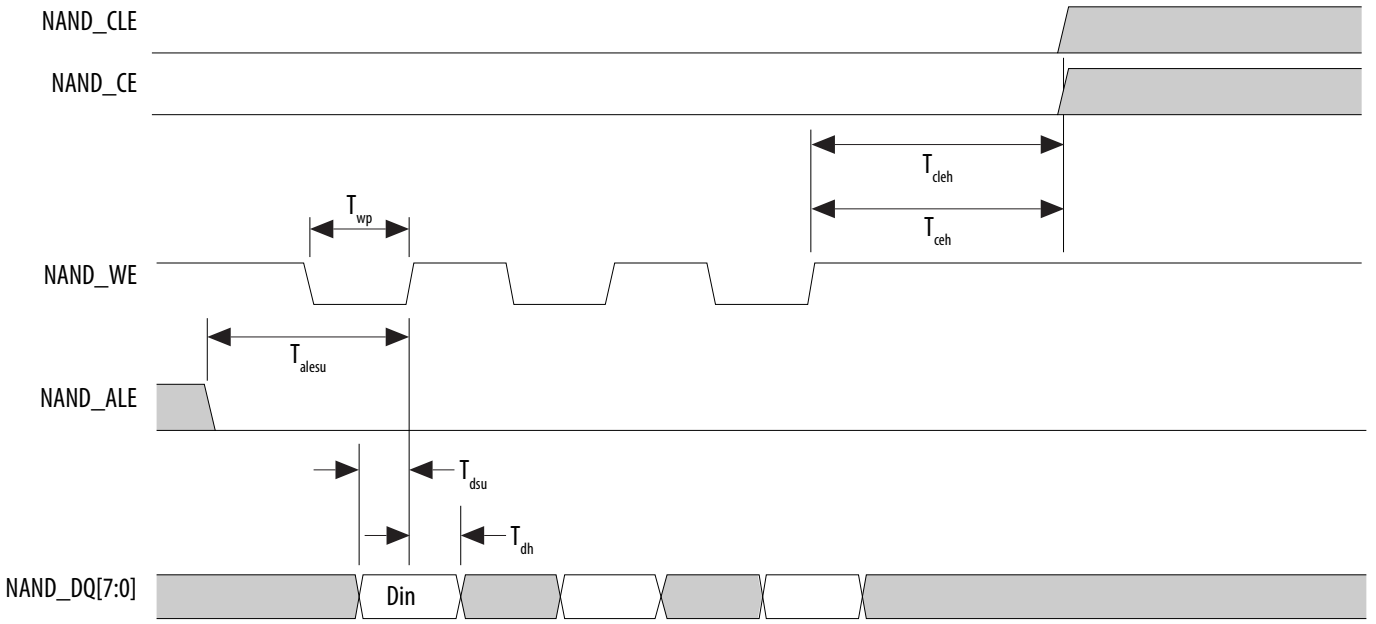
**SPI Controller, Arria V Hard Processor System Technical Reference Manual**
Provides more information about rx_sample_delay.

## SD/MMC Timing Characteristics

**Table 1-54: Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices**

After power up or cold reset, the Boot ROM uses `drvsel` = 3 and `smplsel` = 0 to execute the code. At the same time, the SD/MMC controller enters the Identification Phase followed by the Data Phase. During this time, the value of interface output clock `SDMMC_CLK_OUT` changes from a maximum of 400 kHz (Identification Phase) up to a maximum of 12.5 MHz (Data Phase), depending on the internal reference clock `SDMMC_CLK` and the `CSEL` setting. The value of `SDMMC_CLK` is based on the external oscillator frequency and has a maximum value of 50 MHz.

**Figure 1-19: NAND Data Write Timing Diagram**



| POR Delay | Minimum | Maximum | Unit |
|---|---|---|---|
| Standard | 100 | 300 | ms |

**Related Information**

**MSEL Pin Settings**
Provides more information about POR delay based on MSEL pin settings for each configuration scheme.

## FPGA JTAG Configuration Timing

**Table 1-64: FPGA JTAG Timing Parameters and Values for Arria V Devices**

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 30, 167[92] | — | ns |
| $t_{JCH}$ | TCK clock high time | 14 | — | ns |
| $t_{JCL}$ | TCK clock low time | 14 | — | ns |
| $t_{JPSU\ (TDI)}$ | TDI JTAG port setup time | 2 | — | ns |
| $t_{JPSU\ (TMS)}$ | TMS JTAG port setup time | 3 | — | ns |
| $t_{JPH}$ | JTAG port hold time | 5 | — | ns |
| $t_{JPCO}$ | JTAG port clock to output | — | 12[93] | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | — | 14[93] | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | — | 14[93] | ns |

(92) The minimum TCK clock period is 167 ns if $V_{CCBAT}$ is within the range 1.2 V – 1.5 V when you perform the volatile key programming.
(93) A 1-ns adder is required for each VCCIO voltage step down from 3.0 V. For example, tJPCO= 13 ns if VCCIO of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

## Remote System Upgrades

**Table 1-74: Remote System Upgrade Circuitry Timing Specifications for Arria V Devices**

| Parameter | Minimum | Unit |
|---|---|---|
| $t_{RU\_nCONFIG}$ (110) | 250 | ns |
| $t_{RU\_nRSTIMER}$ (111) | 250 | ns |

**Related Information**

- **Remote System Upgrade State Machine**
  Provides more information about configuration reset (RU_CONFIG) signal.
- **User Watchdog Timer**
  Provides more information about reset_timer (RU_nRSTIMER) signal.

## User Watchdog Internal Oscillator Frequency Specifications

**Table 1-75: User Watchdog Internal Oscillator Frequency Specifications for Arria V Devices**

| Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|
| User watchdog internal oscillator frequency | 5.3 | 7.9 | 12.5 | MHz |

# I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O timing and the Quartus Prime Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

(110) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification.
(111) This is equivalent to strobing the reset timer input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification.

**Related Information**

- **PowerPlay Early Power Estimator User Guide**
  For more information about the EPE tool.
- **PowerPlay Power Analysis**
  For more information about PowerPlay power analysis.

## Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus II PowerPlay Power Analyzer feature.

**Note:** You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

**Related Information**

- **PowerPlay Early Power Estimator User Guide**
  For more information about the EPE tool.
- **PowerPlay Power Analysis**
  For more information about PowerPlay power analysis.

## I/O Pin Leakage Current

**Table 2-8: I/O Pin Leakage Current for Arria V GZ Devices**

If $V_O = V_{CCIO}$ to $V_{CCIOMax}$, 100 µA of leakage current per I/O is expected.

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input pin | $V_I = 0$ V to $V_{CCIOMAX}$ | –30 | — | 30 | µA |
| $I_{OZ}$ | Tri-stated I/O pin | $V_O = 0$ V to $V_{CCIOMAX}$ | –30 | — | 30 | µA |

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Differential on-chip termination resistors | 85-Ω setting | — | 85 ± 20% | — | — | 85 ± 20% | — | Ω |
| | 100-Ω setting | — | 100 ± 20% | — | — | 100 ± 20% | — | Ω |
| | 120-Ω setting | — | 120 ± 20% | — | — | 120 ± 20% | — | Ω |
| | 150-Ω setting | — | 150 ± 20% | — | — | 150 ± 20% | — | Ω |
| $V_{OCM}$ (AC coupled) | 0.65-V setting | — | 650 | — | — | 650 | — | mV |
| $V_{OCM}$ (DC coupled) | — | — | 650 | — | — | 650 | — | mV |
| Intra-differential pair skew | Tx $V_{CM}$ = 0.5 V and slew rate of 15 ps | — | — | 15 | — | — | 15 | ps |
| Intra-transceiver block transmitter channel-to-channel skew | x6 PMA bonded mode | — | — | 120 | — | — | 120 | ps |
| Inter-transceiver block transmitter channel-to-channel skew | xN PMA bonded mode | — | — | 500 | — | — | 500 | ps |

**Related Information**

**Arria V Device Overview**

For more information about device ordering codes.

| Mode | Performance | | | Unit |
|---|---|---|---|---|
| | C3, I3L | C4 | I4 | |
| One sum of two 27 × 27 | 380 | 300 | 290 | MHz |
| One sum of two 36 × 18 | 380 | 300 | | MHz |
| One complex 18 × 18 | 400 | 350 | | MHz |
| One 36 × 36 | 380 | 300 | | MHz |
| **Modes using Three DSP Blocks** | | | | |
| One complex 18 × 25 | 340 | 275 | 265 | MHz |
| **Modes using Four DSP Blocks** | | | | |
| One complex 27 × 27 | 350 | 310 | | MHz |

## Memory Block Specifications

### Table 2-36: Memory Block Performance Specifications for Arria V GZ Devices

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in $F_{MAX}$.

| Memory | Mode | Resources Used | | Performance | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | ALUTs | Memory | C3 | C4 | I3L | I4 | |
| MLAB | Single port, all supported widths | 0 | 1 | 400 | 315 | 400 | 315 | MHz |
| | Simple dual-port, x32/x64 depth | 0 | 1 | 400 | 315 | 400 | 315 | MHz |
| | Simple dual-port, x16 depth (178) | 0 | 1 | 533 | 400 | 533 | 400 | MHz |
| | ROM, all supported widths | 0 | 1 | 500 | 450 | 500 | 450 | MHz |

(178) The $F_{MAX}$ specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{x\ Jitter}$ - True Differential I/O Standards | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 160 | — | — | 160 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.1 | — | — | 0.1 | UI |
| $t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 300 | — | — | 325 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.2 | — | — | 0.25 | UI |
| $t_{DUTY}$ | Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards | 45 | 50 | 55 | 45 | 50 | 55 | % |
| $t_{RISE}$ & $t_{FALL}$ | True Differential I/O Standards | — | — | 200 | — | — | 200 | ps |
| | Emulated Differential I/O Standards with three external output resistor networks | — | — | 250 | — | — | 300 | ps |
| TCCS | True Differential I/O Standards | — | — | 150 | — | — | 150 | ps |
| | Emulated Differential I/O Standards | — | — | 300 | — | — | 300 | ps |

## Receiver High-Speed I/O Specifications

### Table 2-41: Receiver High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

| Number of DQS Delay Buffers | C3, I3L | C4, I4 | Unit |
|---|---|---|---|
| 4 | 120 | 128 | ps |

## Memory Output Clock Jitter Specifications

### Table 2-50: Memory Output Clock Jitter Specification for Arria V GZ Devices

The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

| Clock Network | Parameter | Symbol | C3, I3L | | C4, I4 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| Regional | Clock period jitter | $t_{JIT(per)}$ | –55 | 55 | –55 | 55 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | –110 | 110 | –110 | 110 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | –82.5 | 82.5 | –82.5 | 82.5 | ps |
| Global | Clock period jitter | $t_{JIT(per)}$ | –82.5 | 82.5 | –82.5 | 82.5 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | –165 | 165 | –165 | 165 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | –90 | 90 | –90 | 90 | ps |
| PHY Clock | Clock period jitter | $t_{JIT(per)}$ | –30 | 30 | –35 | 35 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | –60 | 60 | –70 | 70 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | –45 | 45 | –56 | 56 | ps |

**Note:** When you enable the decompression or design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8, FPP ×16, and FPP ×32. For the respective DCLK-to-DATA[] ratio, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.

### Table 2-56: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1

Use these timing parameters when the decompression and design security features are disabled.

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 600 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 600 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 1,506 (205) | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 1,506 (206) | µs |
| $t_{CF2CK}$ (207) | nCONFIG high to first rising edge on DCLK | 1,506 | — | µs |
| $t_{ST2CK}$ (207) | nSTATUS high to first rising edge of DCLK | 2 | — | µs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | 0 | — | ns |
| $t_{CH}$ | DCLK high time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | $1/f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency (FPP ×8/×16) | — | 125 | MHz |
| | DCLK frequency (FPP ×32) | — | 100 | MHz |
| $t_{CD2UM}$ | CONF_DONE high to user mode (208) | 175 | 437 | µs |

(205) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(206) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.
(207) If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + (8576 × CLKUSR period) (209) | — | — |

**Related Information**

- **DCLK-to-DATA[] Ratio (r) for FPP Configuration** on page 2-57
- **Configuration, Design Security, and Remote System Upgrades in Arria V Devices**

(208) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

(209) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

**Table 2-60: PS Timing Parameters for Arria V GZ Devices**

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 600 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 600 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 1,506 (217) | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 1,506 (218) | µs |
| $t_{CF2CK}$ (219) | nCONFIG high to first rising edge on DCLK | 1,506 | — | µs |
| $t_{ST2CK}$ (219) | nSTATUS high to first rising edge of DCLK | 2 | — | µs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | 0 | — | ns |
| $t_{CH}$ | DCLK high time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | $1/f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency | — | 125 | MHz |
| $t_{CD2UM}$ | CONF_DONE high to user mode (220) | 175 | 437 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + (8576 × CLKUSR period) (221) | — | — |

(217) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(218) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.
(219) If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.
(220) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.