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Intel - 5AGXMA7G6F35C6N Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Details	
Product Status	Obsolete
Number of LABs/CLBs	11460
Number of Logic Elements/Cells	242000
Total RAM Bits	15470592
Number of I/O	544
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxma7g6f35c6n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1/O Standard	V _{IL(DC)} (V)		V _{IH(DC)} (V)		V _{IL(AC)} (V)	V _{IH(AC)} (V)	V _{OL} (V)	V _{OH} (V)	I _{OL} ⁽¹⁴⁾	I_{a} (mA)
	Min	Max	Min	Мах	Max	Min	Мах	Min	(mA)	
HSTL-15 Class II	—	V _{REF} – 0.1	$V_{REF} + 0.1$	_	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	V _{CCIO} – 0.4	16	-16
HSTL-12 Class I	-0.15	V _{REF} – 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	V _{REF} – 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	16	-16
HSUL-12	_	V _{REF} – 0.13	$V_{REF} + 0.13$	_	V _{REF} - 0.22	V _{REF} + 0.22	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	_	_

Differential SSTL I/O Standards

Table 1-17: Differential SSTL I/O Standards for Arria V Devices

I/O Standard		V _{CCIO} (V)		V _{SWI}	_{NG(DC)} (V)	V _{X(AC)} (V)			V _{SWING(AC)} (V)		
	Min	Тур	Max	Min	Мах	Min	Тур	Max	Min	Max	
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V _{CCIO} + 0.6	V _{CCIO} /2 – 0.2	—	V _{CCIO} /2 + 0.2	0.62	$V_{CCIO} + 0.6$	
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V _{CCIO} + 0.6	V _{CCIO} /2 – 0.175	—	V _{CCIO} /2 + 0.175	0.5	$V_{CCIO} + 0.6$	
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(15)	V _{CCIO} /2 – 0.15	—	V _{CCIO} /2 + 0.15	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$	
SSTL-135	1.283	1.35	1.45	0.18	(15)	V _{CCIO} /2 – 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} – V _{REF})	$2(V_{IL(AC)} - V_{REF})$	

⁽¹⁴⁾ To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.



 $^{^{(15)}}$ The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

1/O Standard		V _{CCIO} (V)		V _{SWI}	$V_{X(AC)}(V)$ $V_{X(AC)}(V)$ $V_{SWING(AC)}(V)$				_{WING(AC)} (V)	
	Min	Тур	Max	Min	Мах	Min	Тур	Max	Min	Max
SSTL-125	1.19	1.25	1.31	0.18	(15)	V _{CCIO} /2 – 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} – V _{REF})	$2(V_{IL(AC)} - V_{REF})$

Differential HSTL and HSUL I/O Standards

Table 1-18: Differential HSTL and HSUL I/O Standards for Arria V Devices

I/O Standard	,	V _{CCIO} (V))	V _{DI}	_{F(DC)} (V)		V _{X(AC)} (V)			$V_{CM(DC)}(V)$	V _{DIF(AC)} (V)		
	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Мах
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	_	0.78	_	1.12	0.78	_	1.12	0.4	_
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V _{CCIO} + 0.3	_	$0.5 imes V_{ m CCIO}$		$0.4 \times V_{ m CCIO}$	$0.5 imes V_{ m CCIO}$	$0.6 \times V_{ m CCIO}$	0.3	V _{CCIO} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	$\begin{array}{c} 0.5 \times \\ \mathrm{V}_{\mathrm{CCIO}} - \\ 0.12 \end{array}$	0.5 × V _{CCIO}	$\begin{array}{c} 0.5 \times \\ \mathrm{V}_{\mathrm{CCIO}} \\ + \ 0.12 \end{array}$	$0.4 \times V_{\rm CCIO}$	0.5 × V _{CCIO}	0.6 × V _{CCIO}	0.44	0.44

Differential I/O Standard Specifications

Table 1-19: Differential I/O Standard Specifications for Arria V Devices

Differential inputs are powered by V_{CCPD} which requires 2.5 V.



Symbol/Description	Condition	Tran	sceiver Speed Gra	de 3	Unit
Symbol/Description	Condition	Min	Тур	Max	Ont
	85- Ω setting	—	85	—	Ω
Differential on-chip termination	100- Ω setting	—	100	—	Ω
resistors	120-Ω setting	—	120	—	Ω
	150-Ω setting		150	_	Ω
Intra-differential pair skew	TX V_{CM} = 0.65 V (AC coupled) and slew rate of 15 ps			15	ps
Intra-transceiver block transmitter channel-to-channel skew	×6 PMA bonded mode			180	ps
Inter-transceiver block transmitter channel-to-channel skew ⁽⁵⁵⁾	× <i>N</i> PMA bonded mode			500	ps

Table 1-30: CMU PLL Specifications for Arria V GT and ST Devices

Symbol/Description	Transceiver S	peed Grade 3	Unit
Symbol Description	Min	Max	onit
Supported data range	0.611	10.3125	Gbps
fPLL supported data range	611	3125	Mbps

⁽⁵⁵⁾ This specification is only applicable to channels on one side of the device across two transceiver banks.



Protocol	Sub-protocol	Data Rate (Mbps)
	CPRI E6LV	614.4
	CPRI E6HV	614.4
	CPRI E6LVII	614.4
	CPRI E12LV	1,228.8
	CPRI E12HV	1,228.8
	CPRI E12LVII	1,228.8
Common Public Radio Interface (CPRI)	CPRI E24LV	2,457.6
	CPRI E24LVII	2,457.6
	CPRI E30LV	3,072
	CPRI E30LVII	3,072
	CPRI E48LVII	4,915.2
	CPRI E60LVII	6,144
	CPRI E96LVIII ⁽⁶⁰⁾	9,830.4
Gbps Ethernet (GbE)	GbE 1250	1,250
	OBSAI 768	768
ODSAL	OBSAI 1536	1,536
ODSAI	OBSAI 3072	3,072
	OBSAI 6144	6,144
	SDI 270 SD	270
Serial digital interface (SDI)	SDI 1485 HD	1,485
	SDI 2970 3G	2,970



⁽⁶⁰⁾ You can achieve compliance with TX channel restriction of one HSSI channel per six-channel transceiver bank.

	Symbol			-I3, -C4			-l5, -C5		-C6			Unit
			Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
	TCCS	True Differential I/O Standards		_	150		-	150	_	_	150	ps
		Emulated Differential I/O Standards			300		_	300		_	300	ps
	True Differential I/O Standards - freepopp	SERDES factor J =3 to $10^{(76)}$	150		1250	150		1250	150		1050	Mbps
	(data rate)	SERDES factor $J \ge 8$ with DPA ⁽⁷⁶⁾⁽⁷⁸⁾	150	_	1600	150	_	1500	150	_	1250	Mbps
Receiver		SERDES factor J = 3 to 10	(77)	_	(83)	(77)	_	(83)	(77)	_	(83)	Mbps
	f _{HSDR} (data rate)	SERDES factor J = 1 to 2, uses DDR registers	(77)		(79)	(77)	_	(79)	(77)	_	(79)	Mbps
DPA Mode	DPA run length		_	_	10000	_	_	10000	_	_	10000	UI
Soft-CDR Mode	Soft-CDR ppm tolerance			_	300		_	300		_	300	±ppm
Non-DPA Mode	Sampling Window				300		_	300		_	300	ps

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⁽⁸³⁾ You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

Memory Output Clock Jitter Specifications

Table 1-45: Memory Output Clock Jitter Specifications for Arria V Devices

The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard. The memory output clock jitter is applicable when an input jitter of 30 ps (p-p) is applied with bit error rate (BER) 10^{-12} , equivalent to 14 sigma. Altera recommends using the UniPHY intellectual property (IP) with PHYCLK connections for better jitter performance.

Daramotor	Clock Notwork	Symbol	-I3,	-C4	–15,	-C5	_(6	Unit
Falameter	CIOCK NETWORK	Symbol	Min	Max	Min	Max	Min	Max	Onit
Clock period jitter	PHYCLK	t _{JIT(per)}	-41	41	-50	50	-55	55	ps
Cycle-to-cycle period jitter	PHYCLK	t _{JIT(cc)}	6	3	9	0	9	94	ps

OCT Calibration Block Specifications

Table 1-46: OCT Calibration Block Specifications for Arria V Devices

Symbol	Description	Min	Тур	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	_		20	MHz
T _{OCTCAL}	Number of octus RCLK clock cycles required for $R_{\rm S}$ OCT/R_T OCT calibration		1000		Cycles
T _{OCTSHIFT}	Number of OCTUSRCLK clock cycles required for OCT code to shift out		32	_	Cycles
T _{RS_RT}	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	_	2.5		ns



Figure 1-20: NAND Data Read Timing Diagram



ARM Trace Timing Characteristics

Table 1-61: ARM Trace Timing Requirements for Arria V Devices

Most debugging tools have a mechanism to adjust the capture point of trace data.

Description	Min	Мах	Unit
CLK clock period	12.5	_	ns
CLK maximum duty cycle	45	55	%
CLK to D0 –D7 output data delay	-1	1	ns

UART Interface

The maximum UART baud rate is 6.25 megasymbols per second.

GPIO Interface

The minimum detectable general-purpose I/O (GPIO) pulse width is 2 µs. The pulse width is based on a debounce clock frequency of 1 MHz.



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	Symbol	Parameter	Typical	Unit			
			0 (default)	ps			
Л	·	Dising and/or falling adap dalay	50	ps			
D	OUTBUF	Kising and/or failing edge delay	100	ps			
			150	ps			

Glossary

Table 1-78: Glossary

Term	Definition	
Differential I/O standards	Receiver Input Waveforms	
	Single-Ended Waveform	Positive Channel (p) = V_{IH} Negative Channel (n) = V_{IL}
		Ground
	Differential Waveform	
		p - n = 0 V



AV-51002

1-96 Document Revision History

Date	Version	Changes
June 2015	2015.06.16	 Added the supported data rates for the following output standards using true LVDS output buffer types in the High-Speed I/O Specifications for Arria V Devices table:
		True RSDS output standard: data rates of up to 360 Mbps
		 True mini-LVDS output standard: data rates of up to 400 Mbps
		 Added note in the condition for Transmitter—Emulated Differential I/O Standards f_{HSDR} data rate parameter in the High-Speed I/O Specifications for Arria V Devices table. Note: When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.
		Changed Queued Serial Peripheral Interface (QSPI) to Quad Serial Peripheral Interface (SPI) Flash.
		 Updated T_h location in I²C Timing Diagram.
		 Updared T_{wp} location in NAND Address Latch Timing Diagram.
		 Corrected the unit for t_{DH} from ns to s in FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices table.
		• Updated the maximum value for t _{CO} from 4 ns to 2 ns in AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices table.
		• Moved the following timing diagrams to the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.
		FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is 1
		 FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is >1
		AS Configuration Timing Waveform
		PS Configuration Timing Waveform



1-98 Document Revision History

Date	Version	Changes
July 2014	3.8	 Added a note in Table 3, Table 4, and Table 5: The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements. Updated V_{CC_HPS} specification in Table 5. Added a note in Table 19: Differential inputs are powered by V_{CCPD} which requires 2.5 V. Updated "Minimum differential eye opening at the receiver serial input pins" specification in Table 20 and Table 21. Updated description in "HPS PLL Specifications" section. Updated VCO range maximum specification in Table 39. Updated T_d and T_h specifications in Table 45. Added T_h specification in Table 47 and Figure 13. Updated a note in Figure 20, Figure 21, and Figure 23 as follows: Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required. Removed "Remote update only in AS mode" specification in Table 58. Added DCLK device initialization clock source specification in Table 60. Added description in "Configuration Files" section: The IOCSR .rbf size is specifically for the Configuration via Protocol (CvP) feature. Removed f_{MAX_RU_CLK} specification in Table 63.
February 2014	3.7	 Updated V_{CCRSTCLK_HPS} maximum specification in Table 1. Added V_{CC_AUX_SHARED} specification in Table 1.
December 2013	3.6	 Added "HPS PLL Specifications". Added Table 24, Table 39, and Table 40. Updated Table 1, Table 3, Table 5, Table 19, Table 20, Table 21, Table 38, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, Table 51, Table 55, Table 56, and Table 59. Updated Figure 7, Figure 13, Figure 15, Figure 16, and Figure 19. Removed table: GPIO Pulse Width for Arria V Devices.



2-2 Absolute Maximum Ratings

Lower number refers to faster speed grade.

L = Low power devices.

Transceiver Speed Grade	Core Speed Grade					
	C3	C4	I3L	14		
2	Yes	_	Yes	_		
3		Yes		Yes		

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Arria V GZ devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions other than those listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 2-2: Absolute Maximum Ratings for Arria V GZ Devices

Symbol	Description	Minimum	Maximum	Unit
V _{CC}	Power supply for core voltage and periphery circuitry	-0.5	1.35	V
V _{CCPT}	Power supply for programmable power technology	-0.5	1.8	V
V _{CCPGM}	Power supply for configuration pins	-0.5	3.9	V
V _{CC_AUX}	Auxiliary supply for the programmable power technology	-0.5	3.4	V
V _{CCBAT}	Battery back-up power supply for design security volatile key register		3.9	V
V _{CCPD}	I/O pre-driver power supply		3.9	V
V _{CCIO}	I/O power supply		3.9	V
V _{CCD_FPLL}	PLL digital power supply	-0.5	1.8	V
V _{CCA_FPLL}	PLL analog power supply	-0.5	3.4	V



2-4 Recommended Operating Conditions

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle.

For example, a signal that overshoots to 3.95 V can be at 3.95 V for only $\sim 21\%$ over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~ 2 years.

Table 2-4: Maximum Allowed Overshoot During Transitions for Arria V GZ Devices
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Symbol	Description	Condition (V)	Overshoot Duration as % @ T」= 100°C	Unit
	AC input voltage	3.8	100	%
		3.85	64	%
		3.9	36	%
		3.95	21	%
Vi (AC)		4	12	%
		4.05	7	%
		4.1	4	%
		4.15	2	%
		4.2	1	%

Recommended Operating Conditions

Table 2-5: Recommended Operating Conditions for Arria V GZ Devices

Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum ⁽¹¹⁴⁾	Typical	Maximum ⁽¹¹⁴⁾	Unit
V _{CC}	Core voltage and periphery circuitry power supply ⁽¹¹⁵⁾	—	0.82	0.85	0.88	V

⁽¹¹⁴⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.





⁽¹¹⁵⁾ The V_{CC} core supply must be set to 0.9 V if the Partial Reconfiguration (PR) feature is used.

Symbol	Description	Minimum ⁽¹¹⁸⁾	Typical	Maximum ⁽¹¹⁸⁾	Unit
		0.82	0.85	0.88	
V _{CCR_GXBL} ⁽¹²¹⁾	Receiver analog power supply (left side)	0.97	1.0	1.03	V
		1.03	1.05	1.07	
		0.82	0.85	0.88	
V _{CCR_GXBR} ⁽¹²¹⁾	Receiver analog power supply (right side)	0.97	1.0	1.03	V
		1.03	1.05	1.07	
	Transmitter analog power supply (left side)	0.82	0.85	0.88	V
V _{CCT_GXBL} ⁽¹²¹⁾		0.97	1.0	1.03	
		1.03	1.05	1.07	
	Transmitter analog power supply (right side)	0.82	0.85	0.88	
V _{CCT_GXBR} ⁽¹²¹⁾		0.97	1.0	1.03	V
		1.03	1.05	1.07	
V _{CCH_GXBL}	Transmitter output buffer power supply (left side)	1.425	1.5	1.575	V
V _{CCH_GXBR}	Transmitter output buffer power supply (right side)	1.425	1.5	1.575	V



⁽¹¹⁸⁾ This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹²¹⁾ This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rate up to 6.5 Gbps, you can connect this supply to 0.85 V.

Hot Socketing

Table 2-14: Hot Socketing Specifications for Arria V GZ Devices

Symbol	Description	Maximum
I _{IOPIN (DC)}	DC current per I/O pin	300 µA
I _{IOPIN (AC)}	AC current per I/O pin	8 mA ⁽¹²⁴⁾
I _{XCVR-TX (DC)}	DC current per transceiver transmitter pin	100 mA
I _{XCVR-RX (DC)}	DC current per transceiver receiver pin	50 mA

Internal Weak Pull-Up Resistor

Table 2-15: Internal Weak Pull-Up Resistor for Arria V GZ Devices

All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins. The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 k Ω .

Symbol	Description	V _{CCIO} Conditions (V) ⁽¹²⁵⁾	Value ⁽¹²⁶⁾	Unit
	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option.	3.0 ±5%	25	kΩ
		2.5 ±5%	25	kΩ
		1.8 ±5%	25	kΩ
R _{PU}		1.5 ±5%	25	kΩ
		1.35 ±5%	25	kΩ
		1.25 ±5%	25	kΩ
		1.2 ±5%	25	kΩ

⁽¹²⁴⁾ The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.





 $^{^{(125)}}$ The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO} .

 $^{^{(126)}}$ These specifications are valid with a ±10% tolerance to cover changes over PVT.

Table 2-19: Differential SSTL I/O Standards for Arria V GZ Devices

I/O Standard	V _{ccio} (V)			V _{SWING(DC)} (V)		V _{X(AC)} (V)			V _{SWING(AC)} (V)		
	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Мах	
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V _{CCIO} + 0.6	V _{CCIO} /2 - 0.2		V _{CCIO} /2 + 0.2	0.62	$V_{CCIO} + 0.6$	
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V _{CCIO} + 0.6	V _{CCIO} /2 - 0.175	_	V _{CCIO} /2 + 0.175	0.5	$V_{CCIO} + 0.6$	
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(127)	V _{CCIO} /2 - 0.15		V _{CCIO} /2 + 0.15	0.35	—	
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	(127)	V _{CCIO} /2 - 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	$2(V_{IL(AC)} - V_{REF})$	
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(127)	V _{CCIO} /2 - 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	_	
SSTL-12 Class I, II	1.14	1.2	1.26	0.18		V _{REF} -0.15	V _{CCIO} /2	V _{REF} + 0.15	-0.30	0.30	

Table 2-20: Differential HSTL and HSUL I/O Standards for Arria V GZ Devices

I/O Standard	V _{CCIO} (V)		V _{DIF(DC)} (V)		$V_{X(AC)}(V)$			V _{CM(DC)} (V)			V _{DIF(AC)} (V)		
	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Мах
HSTL-18 Class I, II	1.71	1.8	1.89	0.2		0.78		1.12	0.78	_	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68		0.9	0.4	—



 $^{^{(127)}}$ The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Switching Characteristics

Transceiver Performance Specifications

Reference Clock

Table 2-22: Reference Clock Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transce	eiver Speed (Grade 2	Transce	eiver Speed	Unit			
Symbol/Description	Conditions	Min	Тур	Max	Min	Тур	Max	Onit		
Reference Clock										
Supported I/O Standards	Dedicated reference clock and HCSL 1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL,									
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS								
Input Reference Clock Frequency (CMU PLL) ⁽¹³⁷⁾	_	40		710	40		710	MHz		
Input Reference Clock Frequency (ATX PLL) ⁽¹³⁷⁾	-	100		710	100		710	MHz		

⁽¹³⁷⁾ The input reference clock frequency options depend on the data rate and the device speed grade.



Sumbol	Conditions	C3, I3L				Unit			
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Onic	
	SERDES factor J = 3 to 10 (182), (183)	(184)	—	1250	(184)	—	1050	Mbps	
True Differential I/O Standards - f _{HSDR} (data rate)	SERDES factor $J \ge 4$ LVDS TX with DPA (185), (186), (187), (188)	(184)		1600	(184)	_	1250	Mbps	
	SERDES factor J = 2, uses DDR Registers	(184)	—	(189)	(184)	_	(189)	Mbps	
	SERDES factor J = 1, uses SDR Register	(184)	—	(189)	(184)		(189)	Mbps	
Emulated Differential I/O Standards with Three External Output Resistor Networks - f _{HSDR} (data rate) (190)	SERDES factor J = 4 to 10 ⁽¹⁹¹⁾	(184)		840	(184)		840	Mbps	

⁽¹⁸²⁾ If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

- ⁽¹⁸⁵⁾ Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.
- Requires package skew compensation with PCB trace length. (186)
- (187)Do not mix single-ended I/O buffer within LVDS I/O bank.
- Chip-to-chip communication only with a maximum load of 5 pF. (188)
- ⁽¹⁸⁹⁾ The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.
- ⁽¹⁹⁰⁾ You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.
- ⁽¹⁹¹⁾ When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.



⁽¹⁸³⁾ The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

⁽¹⁸⁴⁾ The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.



Non DPA Mode High-Speed I/O Specifications

Table 2-46: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions		C3, I3L			Unit		
Symbol		Min	Тур	Max	Min	Тур	Max	
Sampling Window	—	_		300	_		300	ps



Passive Serial Configuration Timing

Figure 2-10: PS Configuration Timing Waveform

Timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.



Notes:

- 1. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- 2. After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.
- 3. After power-up, before and during configuration, CONF_DONE is low.
- 4. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- 5. DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the Device and Pins Option.
- 6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- 7. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.



Programmable IOE Delay

Fast Model Slow Model Available Parameter (228) Min Offset (229) Unit Settings Industrial Commercial C3 C4 I3L 14 D1 64 0 0.464 0.493 0.924 1.011 0.921 1.006 ns 0 D2 32 0.230 0.244 0.459 0.503 0.456 0.500 ns D3 8 0 1.699 2.992 3.192 1.587 3.047 3.257 ns 0 D4 64 0.464 0.492 0.924 1.011 0.920 1.006 ns D5 64 0 0.464 0.493 0.924 1.011 0.921 1.006 ns 0.499 D6 32 0 0.244 0.503 0.229 0.458 0.456 ns

Table 2-66: IOE Programmable Delay for Arria V GZ Devices

Programmable Output Buffer Delay

Table 2-67: Programmable Output Buffer Delay for Arria V GZ Devices

You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

Symbol	Parameter	Typical	Unit
		0 (default)	ps
D	Dising and/or falling adge delay	50	ps
DOUTBUF	Rising and/or failing edge delay	100	ps
		150	ps

⁽²²⁸⁾ You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D4**, **D5**, and **D6** in the **Assignment Name** column of **Assignment Editor**.





⁽²²⁹⁾ Minimum offset does not include the intrinsic delay.