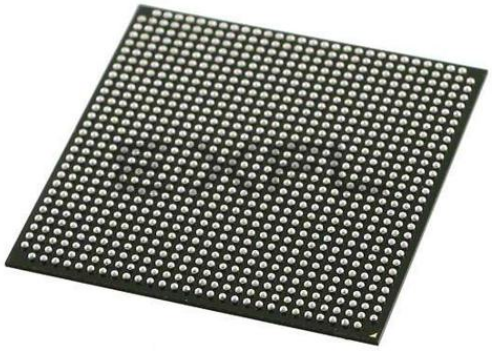

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 14151 |
| Number of Logic Elements/Cells | 300000 |
| Total RAM Bits | 17358848 |
| Number of I/O | 384 |
| Number of Gates | - |
| Voltage - Supply | 1.07V ~ 1.13V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 896-BBGA, FCBGA |
| Supplier Device Package | 896-FBGA (31x31) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5agxmb1g4f31c4n |

## Transceiver Power Supply Operating Conditions

**Table 1-4: Transceiver Power Supply Operating Conditions for Arria V Devices**

| Symbol | Description | Minimum[5] | Typical | Maximum[5] | Unit |
|---|---|---|---|---|---|
| $V_{CCA\_GXBL}$ | Transceiver high voltage power (left side) | 2.375 | 2.500 | 2.625 | V |
| $V_{CCA\_GXBR}$ | Transceiver high voltage power (right side) | | | | |
| $V_{CCR\_GXBL}$ | GX and SX speed grades—receiver power (left side) | 1.08/1.12 | 1.1/1.15[6] | 1.14/1.18 | V |
| $V_{CCR\_GXBR}$ | GX and SX speed grades—receiver power (right side) | | | | |
| $V_{CCR\_GXBL}$ | GT and ST speed grades—receiver power (left side) | 1.17 | 1.20 | 1.23 | V |
| $V_{CCR\_GXBR}$ | GT and ST speed grades—receiver power (right side) | | | | |
| $V_{CCT\_GXBL}$ | GX and SX speed grades—transmitter power (left side) | 1.08/1.12 | 1.1/1.15[6] | 1.14/1.18 | V |
| $V_{CCT\_GXBR}$ | GX and SX speed grades—transmitter power (right side) | | | | |
| $V_{CCT\_GXBL}$ | GT and ST speed grades—transmitter power (left side) | 1.17 | 1.20 | 1.23 | V |
| $V_{CCT\_GXBR}$ | GT and ST speed grades—transmitter power (right side) | | | | |
| $V_{CCH\_GXBL}$ | Transmitter output buffer power (left side) | 1.425 | 1.500 | 1.575 | V |
| $V_{CCH\_GXBR}$ | Transmitter output buffer power (right side) | | | | |

(5) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(6) For data rate <=3.2 Gbps, connect $V_{CCR\_GXBL/R}$, $V_{CCT\_GXBL/R}$, or $V_{CCL\_GXBL/R}$ to either 1.1-V or 1.15-V power supply. For data rate >3.2 Gbps, connect $V_{CCR\_GXBL/R}$, $V_{CCT\_GXBL/R}$, or $V_{CCL\_GXBL/R}$ to a 1.15-V power supply. For details, refer to the Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines.

## Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

**Table 1-15: Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.418 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ |
| SSTL-125 Class I, II | 1.19 | 1.25 | 1.26 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | — | $V_{CCIO}$/2 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 | — | $V_{CCIO}$/2 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.47 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.53 × $V_{CCIO}$ | — | $V_{CCIO}$/2 | — |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | — | — | — |

- **Transceiver Specifications for Arria V GT and ST Devices** on page 1-29
  Provides the specifications for transmitter, receiver, and reference clock I/O pin.

# Switching Characteristics

This section provides performance characteristics of Arria V core and periphery blocks.

## Transceiver Performance Specifications

### Transceiver Specifications for Arria V GX and SX Devices

**Table 1-20: Reference Clock Specifications for Arria V GX and SX Devices**

| Symbol/Description | Condition | Transceiver Speed Grade 4 | | | Transceiver Speed Grade 6 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supported I/O standards | 1.2 V PCML, 1.4 V PCML,1.5 V PCML, 2.5 V PCML, Differential LVPECL[23], HCSL, and LVDS | | | | | | | |
| Input frequency from REFCLK input pins | — | 27 | — | 710 | 27 | — | 710 | MHz |
| Rise time | Measure at ±60 mV of differential signal[24] | — | — | 400 | — | — | 400 | ps |
| Fall time | Measure at ±60 mV of differential signal[24] | — | — | 400 | — | — | 400 | ps |
| Duty cycle | — | 45 | — | 55 | 45 | — | 55 | % |
| Peak-to-peak differential input voltage | — | 200 | — | 300[25]/ 2000 | 200 | — | 300[25]/ 2000 | mV |

(23) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.
(24) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
(25) The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

## Transceiver Specifications for Arria V GT and ST Devices

### Table 1-26: Reference Clock Specifications for Arria V GT and ST Devices

| Symbol/Description | Condition | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Supported I/O standards | 1.2 V PCML, 1.4 VPCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL(40), HCSL, and LVDS | | | | |
| Input frequency from REFCLK input pins | — | 27 | — | 710 | MHz |
| Rise time | Measure at ±60 mV of differential signal(41) | — | — | 400 | ps |
| Fall time | Measure at ±60 mV of differential signal(41) | — | — | 400 | ps |
| Duty cycle | — | 45 | — | 55 | % |
| Peak-to-peak differential input voltage | — | 200 | — | 300(42)/2000 | mV |
| Spread-spectrum modulating clock frequency | PCI Express (PCIe) | 30 | — | 33 | kHz |
| Spread-spectrum downspread | PCIe | — | 0 to –0.5% | — | — |
| On-chip termination resistors | — | — | 100 | — | Ω |
| $V_{ICM}$ (AC coupled) | — | — | 1.2 | — | V |
| $V_{ICM}$ (DC coupled) | HCSL I/O standard for the PCIe reference clock | 250 | — | 550 | mV |

(40) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.
(41) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
(42) The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

| Symbol | $V_{OD}$ Setting[58] | $V_{OD}$ Value (mV) | $V_{OD}$ Setting[58] | $V_{OD}$ Value (mV) |
|---|---|---|---|---|
| | 25 | 500 | 53 | 1060 |
| | 26 | 520 | 54 | 1080 |
| | 27 | 540 | 55 | 1100 |
| | 28 | 560 | 56 | 1120 |
| | 29 | 580 | 57 | 1140 |
| | 30 | 600 | 58 | 1160 |
| | 31 | 620 | 59 | 1180 |
| | 32 | 640 | 60 | 1200 |
| | 33 | 660 | | |

## Transmitter Pre-Emphasis Levels

The following table lists the simulation data on the transmitter pre-emphasis levels in dB for the first post tap under the following conditions:

- Low-frequency data pattern—five 1s and five 0s
- Data rate—2.5 Gbps

The levels listed are a representation of possible pre-emphasis levels under the specified conditions only and the pre-emphasis levels may change with data pattern and data rate.

Arria V devices only support 1st post tap pre-emphasis with the following conditions:

- The 1st post tap pre-emphasis settings must satisfy $|B| + |C| \leq 60$ where $|B| = V_{OD}$ setting with termination value, $R_{TERM} = 100\ \Omega$ and $|C|$ = 1st post tap pre-emphasis setting.
- $|B| - |C| > 5$ for data rates < 5 Gbps and $|B| - |C| > 8.25$ for data rates > 5 Gbps.
- $(V_{MAX}/V_{MIN} - 1)\% < 600\%$, where $V_{MAX} = |B| + |C|$ and $V_{MIN} = |B| - |C|$.

Exception for PCIe Gen2 design: $V_{OD}$ setting = 43 and pre-emphasis setting = 19 are allowed for PCIe Gen2 design with transmit de-emphasis – 6dB setting (`pipe_txdeemp` = 1'b0) using Altera PCIe Hard IP and PIPE IP cores.

[58] Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

| Symbol | | Condition | –I3, –C4 | | | –I5, –C5 | | | –C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | TCCS | True Differential I/O Standards | — | — | 150 | — | — | 150 | — | — | 150 | ps |
| | | Emulated Differential I/O Standards | — | — | 300 | — | — | 300 | — | — | 300 | ps |
| Receiver | True Differential I/O Standards - $f_{HSDRDPA}$ (data rate) | SERDES factor J =3 to 10(76) | 150 | — | 1250 | 150 | — | 1250 | 150 | — | 1050 | Mbps |
| | | SERDES factor J ≥ 8 with DPA(76)(78) | 150 | — | 1600 | 150 | — | 1500 | 150 | — | 1250 | Mbps |
| | $f_{HSDR}$ (data rate) | SERDES factor J = 3 to 10 | (77) | — | (83) | (77) | — | (83) | (77) | — | (83) | Mbps |
| | | SERDES factor J = 1 to 2, uses DDR registers | (77) | — | (79) | (77) | — | (79) | (77) | — | (79) | Mbps |
| DPA Mode | DPA run length | — | — | — | 10000 | — | — | 10000 | — | — | 10000 | UI |
| Soft-CDR Mode | Soft-CDR ppm tolerance | — | — | — | 300 | — | — | 300 | — | — | 300 | ±ppm |
| Non-DPA Mode | Sampling Window | — | — | — | 300 | — | — | 300 | — | — | 300 | ps |

(83) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

## HPS Clock Performance

### Table 1-48: HPS Clock Performance for Arria V Devices

| Symbol/Description | –I3 | –C4 | –C5, –I5 | –C6 | Unit |
|---|---|---|---|---|---|
| mpu_base_clk (microprocessor unit clock) | 1050 | 925 | 800 | 700 | MHz |
| main_base_clk (L3/L4 interconnect clock) | 400 | 400 | 400 | 350 | MHz |
| h2f_user0_clk | 100 | 100 | 100 | 100 | MHz |
| h2f_user1_clk | 100 | 100 | 100 | 100 | MHz |
| h2f_user2_clk | 200 | 200 | 200 | 160 | MHz |

## HPS PLL Specifications

### HPS PLL VCO Frequency Range

### Table 1-49: HPS PLL VCO Frequency Range for Arria V Devices

| Description | Speed Grade | Minimum | Maximum | Unit |
|---|---|---|---|---|
| VCO range | –C5, –I5, –C6 | 320 | 1,600 | MHz |
| | –C4 | 320 | 1,850 | MHz |
| | –I3 | 320 | 2,100 | MHz |

### HPS PLL Input Clock Range

The HPS PLL input clock range is 10 – 50 MHz. This clock range applies to both HPS_CLK1 and HPS_CLK2 inputs.

**Related Information**

**Clock Select, Booting and Configuration chapter**
Provides more information about the clock range for different values of clock select (CSEL).

**Figure 1-9: SPI Master Timing Diagram**

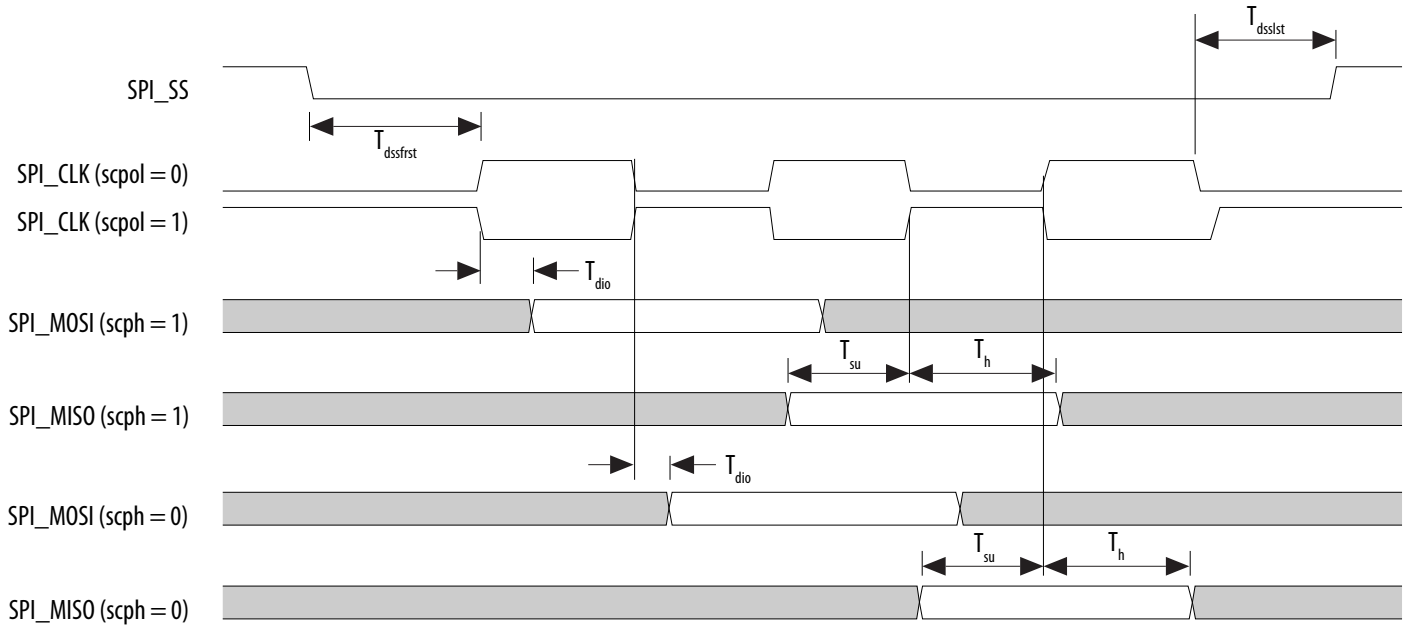


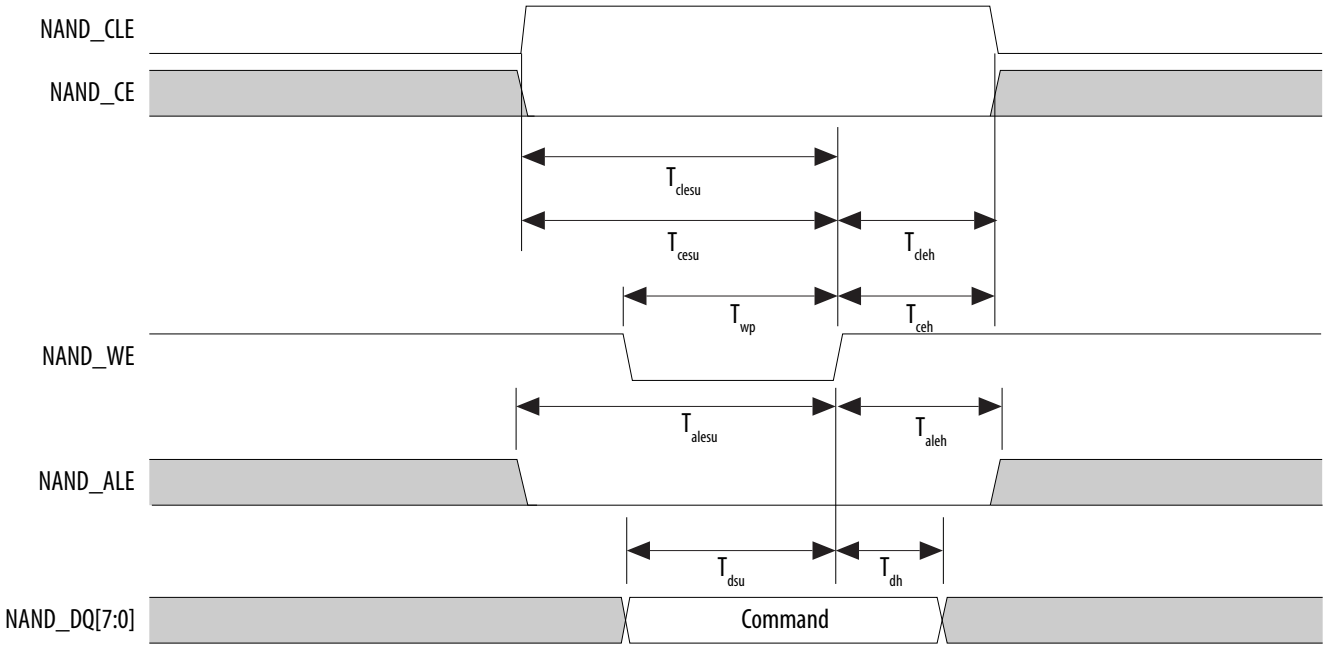

**Table 1-53: SPI Slave Timing Requirements for Arria V Devices**

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $T_{clk}$ | CLK clock period | 20 | — | ns |
| $T_s$ | MOSI Setup time | 5 | — | ns |
| $T_h$ | MOSI Hold time | 5 | — | ns |
| $T_{suss}$ | Setup time SPI_SS valid before first clock edge | 8 | — | ns |
| $T_{hss}$ | Hold time SPI_SS valid after last clock edge | 8 | — | ns |
| $T_d$ | MISO output delay | — | 6 | ns |

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $T_{dh}$ (89) | Data to write enable hold time | 5 | — | ns |
| $T_{cea}$ | Chip enable to data access time | — | 25 | ns |
| $T_{rea}$ | Read enable to data access time | — | 16 | ns |
| $T_{rhz}$ | Read enable to data high impedance | — | 100 | ns |
| $T_{rr}$ | Ready to read enable low | 20 | — | ns |

**Figure 1-17: NAND Command Latch Timing Diagram**



## I/O Standard Specifications

The $V_{OL}$ and $V_{OH}$ values are valid at the corresponding $I_{OH}$ and $I_{OL}$, respectively.

**Table 2-16: Single-Ended I/O Standards for Arria V GZ Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{IL}$ (V) | | $V_{IH}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| LVTTL | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.6 | 0.4 | 2.4 | 2 | –2 |
| LVCMOS | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| 2.5 V | 2.375 | 2.5 | 2.625 | –0.3 | 0.7 | 1.7 | 3.6 | 0.4 | 2 | 1 | –1 |
| 1.8 V | 1.71 | 1.8 | 1.89 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.45 | $V_{CCIO}$ – 0.45 | 2 | –2 |
| 1.5 V | 1.425 | 1.5 | 1.575 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 2 | –2 |
| 1.2 V | 1.14 | 1.2 | 1.26 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 2 | –2 |

**Table 2-17: Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V GZ Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × VCCIO | 0.51 × $V_{CCIO}$ |

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{ol}$ (mA) | $I_{oh}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-18 Class II | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | 0.28 | $V_{CCIO}$ – 0.28 | 13.4 | –13.4 |
| SSTL-15 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.175 | $V_{REF}$ + 0.175 | 0.2 × $V_{CCIO}$ | 0.8 × $V_{CCIO}$ | 8 | –8 |
| SSTL-15 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.175 | $V_{REF}$ + 0.175 | 0.2 × $V_{CCIO}$ | 0.8 × $V_{CCIO}$ | 16 | –16 |
| SSTL-135 Class I, II | — | $V_{REF}$ – 0.09 | $V_{REF}$ + 0.09 | — | $V_{REF}$ – 0.16 | $V_{REF}$ + 0.16 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |
| SSTL-125 Class I, II | — | $V_{REF}$ – 0.85 | $V_{REF}$ + 0.85 | — | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |
| SSTL-12 Class I, II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |
| HSTL-18 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-18 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 16 | –16 |
| HSTL-15 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-15 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 16 | –16 |
| HSTL-12 Class I | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 8 | –8 |
| HSTL-12 Class II | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 16 | –16 |
| HSUL-12 | — | $V_{REF}$ – 0.13 | $V_{REF}$ + 0.13 | — | $V_{REF}$ – 0.22 | $V_{REF}$ + 0.22 | 0.1 × $V_{CCIO}$ | 0.9 × $V_{CCIO}$ | — | — |

| I/O Standard | $V_{CCIO}$ (V) [128] | | | $V_{ID}$ (mV) [129] | | | $V_{ICM(DC)}$ (V) | | | $V_{OD}$ (V) [130] | | | $V_{OCM}$ (V) [130] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Condition | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| RSDS (HIO) [133] | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.3 | — | 1.4 | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.4 |
| Mini-LVDS (HIO) [134] | 2.375 | 2.5 | 2.625 | 200 | — | 600 | 0.4 | — | 1.325 | 0.25 | — | 0.6 | 1 | 1.2 | 1.4 |
| LVPECL [135], [136] | — | — | — | 300 | — | — | 0.6 | $D_{MAX} \leq$ 700 Mbps | 1.8 | — | — | — | — | — | — |
| | — | — | — | 300 | — | — | 1 | $D_{MAX} >$ 700 Mbps | 1.6 | — | — | — | — | — | — |

**Related Information**

**Glossary** on page 2-73

[128] Differential inputs are powered by VCCPD which requires 2.5 V.
[129] The minimum VID value is applicable over the entire common mode range, VCM.
[130] RL range: 90 ≤ RL ≤ 110 Ω.
[133] For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.
[134] For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.
[135] LVPECL is only supported on dedicated clock input pins.
[136] For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{OUT}$ (169) | Output frequency for an internal global or regional clock (C3, I3L speed grade) | — | — | 650 | MHz |
| | Output frequency for an internal global or regional clock (C4, I4 speed grade) | — | — | 580 | MHz |
| $f_{OUT\_EXT}$ (169) | Output frequency for an external clock output (C3, I3L speed grade) | — | — | 667 | MHz |
| | Output frequency for an external clock output (C4, I4 speed grade) | — | — | 533 | MHz |
| $t_{OUTDUTY}$ | Duty cycle for a dedicated external clock output (when set to 50%) | 45 | 50 | 55 | % |
| $t_{FCOMP}$ | External feedback clock compensation time | — | — | 10 | ns |
| $f_{DYCONFIGCLK}$ | Dynamic configuration clock for `mgmt_clk` and `scanclk` | — | — | 100 | MHz |
| $t_{LOCK}$ | Time required to lock from the end-of-device configuration or deassertion of `areset` | — | — | 1 | ms |
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/ delays) | — | — | 1 | ms |
| $f_{CLBW}$ | PLL closed-loop low bandwidth | — | 0.3 | — | MHz |
| | PLL closed-loop medium bandwidth | — | 1.5 | — | MHz |
| | PLL closed-loop high bandwidth (170) | — | 4 | — | MHz |
| $t_{PLL\_PSERR}$ | Accuracy of PLL phase shift | — | — | ±50 | ps |
| $t_{ARESET}$ | Minimum pulse width on the `areset` signal | 10 | — | — | ns |

(169) This specification is limited by the lower of the two: I/O $f_{MAX}$ or $f_{OUT}$ of the PLL.
(170) High bandwidth PLL settings are not supported in external feedback mode.

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $k_{VALUE}$ | Numerator of Fraction | 128 | 8388608 | 2147483648 | — |
| $f_{RES}$ | Resolution of VCO frequency ($f_{INPFD}$ = 100 MHz) | 390625 | 5.96 | 0.023 | Hz |

**Related Information**

- **Duty Cycle Distortion (DCD) Specifications** on page 2-56
- **DLL Range Specifications** on page 2-53

## DSP Block Specifications

**Table 2-35: DSP Block Performance Specifications for Arria V GZ Devices**

| Mode | Performance | | | Unit |
|---|---|---|---|---|
| | C3, I3L | C4 | I4 | |
| **Modes using One DSP Block** | | | | |
| Three 9 × 9 | 480 | 420 | | MHz |
| One 18 × 18 | 480 | 420 | 400 | MHz |
| Two partial 18 × 18 (or 16 × 16) | 480 | 420 | 400 | MHz |
| One 27 × 27 | 400 | 350 | | MHz |
| One 36 × 18 | 400 | 350 | | MHz |
| One sum of two 18 × 18 (One sum of two 16 × 16) | 400 | 350 | | MHz |
| One sum of square | 400 | 350 | | MHz |
| One 18 × 18 plus 36 (a × b) + c | 400 | 350 | | MHz |
| **Modes using Two DSP Blocks** | | | | |
| Three 18 × 18 | 400 | 350 | | MHz |
| One sum of four 18 × 18 | 380 | 300 | | MHz |

| Description | Min | Typ | Max | Unit |
|---|---|---|---|---|
| Diode ideality factor | 1.006 | 1.008 | 1.010 | — |

# Periphery Performance

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

**Note:** The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

## High-Speed I/O Specification

### High-Speed Clock Specifications

**Table 2-39: High-Speed Clock Specifications for Arria V GZ Devices**

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

Arria V GZ devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 230 Mbps
- True mini-LVDS output standard with data rates of up to 340 Mbps

| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{x\ Jitter}$ - True Differential I/O Standards | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 160 | — | — | 160 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.1 | — | — | 0.1 | UI |
| $t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 300 | — | — | 325 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.2 | — | — | 0.25 | UI |
| $t_{DUTY}$ | Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards | 45 | 50 | 55 | 45 | 50 | 55 | % |
| $t_{RISE}$ & $t_{FALL}$ | True Differential I/O Standards | — | — | 200 | — | — | 200 | ps |
| | Emulated Differential I/O Standards with three external output resistor networks | — | — | 250 | — | — | 300 | ps |
| TCCS | True Differential I/O Standards | — | — | 150 | — | — | 150 | ps |
| | Emulated Differential I/O Standards | — | — | 300 | — | — | 300 | ps |

## Receiver High-Speed I/O Specifications

### Table 2-41: Receiver High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

**Figure 2-4: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate ≥ 1.25 Gbps**

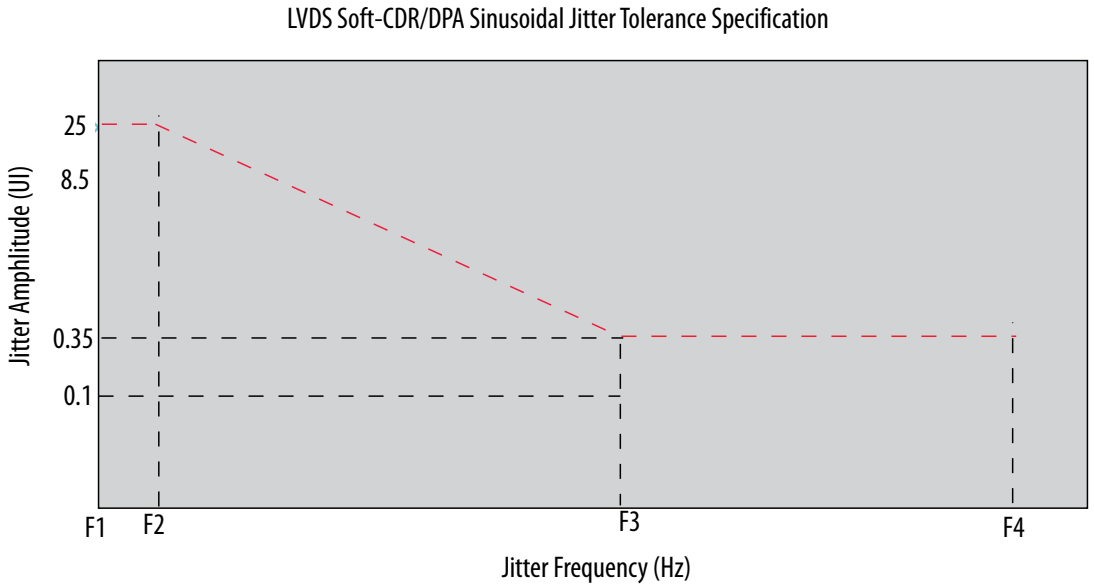



**Table 2-45: LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate ≥ 1.25 Gbps**

| Jitter Frequency (Hz) | | Sinusoidal Jitter (UI) |
|---|---|---|
| F1 | 10,000 | 25.000 |
| F2 | 17,565 | 25.000 |
| F3 | 1,493,000 | 0.350 |
| F4 | 50,000,000 | 0.350 |

## DLL Range Specifications

### Table 2-47: DLL Range Specifications for Arria V GZ Devices

Arria V GZ devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

| Parameter | C3, I3L | C4, I4 | Unit |
|---|---|---|---|
| DLL operating frequency range | 300 – 890 | 300 – 890 | MHz |

## DQS Logic Block Specifications

### Table 2-48: DQS Phase Offset Delay Per Setting for Arria V GZ Devices

The typical value equals the average of the minimum and maximum values.

The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a –3 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 11 ps) ± 20 ps] = 735 ps ± 20 ps.

| Speed Grade | Min | Max | Unit |
|---|---|---|---|
| C3, I3L | 8 | 15 | ps |
| C4, I4 | 8 | 16 | ps |

### Table 2-49: DQS Phase Shift Error Specification for DLL-Delayed Clock ($t_{DQS\_PSERR}$) for Arria V GZ Devices

This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a –3 speed grade is ±84 ps or ±42 ps.

| Number of DQS Delay Buffers | C3, I3L | C4, I4 | Unit |
|---|---|---|---|
| 1 | 30 | 32 | ps |
| 2 | 60 | 64 | ps |
| 3 | 90 | 96 | ps |

**Related Information**

**Configuration, Design Security, and Remote System Upgrades in Arria V Devices**

## Initialization

**Table 2-61: Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices**

| Initialization Clock Source | Configuration Schemes | Maximum Frequency (MHz) | Minimum Number of Clock Cycles |
|---|---|---|---|
| Internal Oscillator | AS, PS, FPP | 12.5 | 8576 |
| CLKUSR (222) | PS, FPP | 125 | |
| | AS | 100 | |
| DCLK | PS, FPP | 125 | |

## Configuration Files

Use the following table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (`.hex`) or tabular text file (`.ttf`) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size.

(221) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

(222) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** panel of the **Device and Pin Options** dialog box.

| Date | Version | Changes |
|---|---|---|
| July 2014 | 3.8 | • Updated Table 21.<br>• Updated Table 22 $V_{OCM}$ (DC Coupled) condition.<br>• Updated the DCLK note to Figure 6, Figure 7, and Figure 9.<br>• Added note to Table 5 and Table 6.<br>• Added the DCLK specification to Table 50.<br>• Added note to Table 51.<br>• Updated the list of parameters in Table 53. |
| February 2014 | 3.7 | Updated Table 28. |
| December 2013 | 3.6 | • Updated Table 2, Table 13, Table 18, Table 19, Table 22, Table 30, Table 33, Table 37, Table 38, Table 45, Table 46, Table 47, Table 56, Table 49.<br>• Updated "PLL Specifications". |
| August 2013 | 3.5 | Updated Table 28. |
| August 2013 | 3.4 | • Removed Preliminary tags for Table 2, Table 4, Table 5, Table 14, Table 27, Table 28, Table 29, Table 31, Table 32, Table 43, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, and Table 54.<br>• Updated Table 2 and Table 28. |
| June 2013 | 3.3 | Updated Table 23, Table 28, Table 51, and Table 55. |
| May 2013 | 3.2 | • Added Table 23.<br>• Updated Table 5, Table 22, Table 26, and Table 57.<br>• Updated Figure 6, Figure 7, Figure 8, and Figure 9. |
| March 2013 | 3.1 | • Updated Table 2, Table 6, Table 7, Table 8, Table 19, Table 22, Table 26, Table 29, Table 52.<br>• Updated "Maximum Allowed Overshoot and Undershoot Voltage". |
| December 2012 | 3.0 | Initial release. |