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Intel - 5AGXMB1G4F31C5N Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	14151
Number of Logic Elements/Cells	300000
Total RAM Bits	17358848
Number of I/O	384
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxmb1g4f31c5n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Symbol	Description	Condition	Minimum ⁽¹⁾	Typical	Maximum ⁽¹⁾	Unit
	-	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
V	1/O buffers newer supply	1.8 V	1.71	1.8	1.89	V
V CCIO	1/O bullets power supply	1.5 V	1.425	1.5	1.575	V
		1.35 V	1.283	1.35	1.418	V
		1.25 V	1.19	1.25	1.31	V
		1.2 V	1.14	1.2	1.26	V
V _{CCD_FPLL}	PLL digital voltage regulator power supply	_	1.425	1.5	1.575	V
V _{CCA_FPLL}	PLL analog voltage regulator power supply	_	2.375	2.5	2.625	V
V _I	DC input voltage	_	-0.5	_	3.6	V
V _O	Output voltage	_	0	_	V _{CCIO}	V
T	Operating junction temperature	Commercial	0	_	85	°C
1 j	Operating junction temperature	Industrial	-40	_	100	°C
+ (4)	Power supply ramp time	Standard POR	200 µs	_	100 ms	_
t _{RAMP} ^(*)	Power supply ramp time	Fast POR	200 µs	_	4 ms	_



⁽¹⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁴⁾ This is also applicable to HPS power supply. For HPS power supply, refer to t_{RAMP} specifications for standard POR when HPS_PORSEL = 0 and t_{RAMP} specifications for fast POR when HPS_PORSEL = 1.

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Symbol	Description	Condition	Minimum ⁽⁷⁾	Typical	Maximum ⁽⁷⁾	Unit
	HPS I/O	3.3 V	3.135	3.3	3.465	V
V _{CCPD_HPS} ⁽⁸⁾	pre-driver	3.0 V	2.85	3.0	3.15	V
	supply	2.5 V	2.375	2.5	2.625	V
V _{CCIO_HPS}		3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
	HPS I/O	2.5 V	2.375	2.5	2.625	V
	buffers power	1.8 V	1.71	1.8	1.89	V
	supply	1.5 V	1.425	1.5	1.575	V
		1.35 V ⁽⁹⁾	1.283	1.35	1.418	V
		1.2 V	1.14	1.2	1.26	V
	HPS reset	3.3 V	3.135	3.3	3.465	V
V	and clock	3.0 V	2.85	3.0	3.15	V
V CCRSTCLK_HPS	power	2.5 V	2.375	2.5	2.625	V
	supply	1.8 V	1.71	1.8	1.89	V
V _{CCPLL_HPS}	HPS PLL analog voltage regulator power supply	_	2.375	2.5	2.625	V



⁽⁷⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁸⁾ V_{CCPD_HPS} must be 2.5 V when V_{CCIO_HPS} is 2.5, 1.8, 1.5, or 1.2 V. V_{CCPD_HPS} must be 3.0 V when V_{CCIO_HPS} is 3.0 V. V_{CCPD_HPS} must be 3.3 V when V_{CCIO_HPS} is 3.3 V.

 $^{^{(9)}\,}$ V_{CCIO_HPS} 1.35 V is supported for HPS row I/O bank only.

Table 1-21: Transceiver Clocks Specifications for Arria V GX and SX Devices

Sumbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit	
Symbol/Description	Condition	Min	Тур	Max	Min	Тур	Max	Onit	
fixedclk clock frequency	PCIe Receiver Detect	_	125	_	_	125	_	MHz	
Transceiver Reconfigura- tion Controller IP (mgmt_ clk_clk) clock frequency	_	75	_	125	75	_	125	MHz	

Table 1-22: Receiver Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			11
symbol/Description	Condition	Min	Тур	Мах	Min	Тур	Max	Onit
Supported I/O standards		1	.5 V PCML,	2.5 V PCML,	LVPECL, an	d LVDS		
Data rate ⁽²⁸⁾		611	—	6553.6	611	—	3125	Mbps
Absolute V_{MAX} for a receiver pin ⁽²⁹⁾	_		_	1.2		—	1.2	V
Absolute V _{MIN} for a receiver pin	_	-0.4	_		-0.4	—	—	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) before device configuration	_	_		1.6		_	1.6	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) after device configuration	_	_	_	2.2		_	2.2	V



 ⁽²⁸⁾ To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.
 ⁽²⁹⁾ The device cannot tolerate prolonged operation at this absolute maximum.

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
Symbol/Description	Condition	Min	Тур	Max	Min	Тур	Max	Onic
Minimum differential eye opening at the receiver serial input pins ⁽³⁰⁾	_	100	_	_	100	_	_	mV
V _{ICM} (AC coupled)	—	_	0.7/0.75/ 0.8 ⁽³¹⁾			0.7/0.75/ 0.8 ⁽³¹⁾	—	mV
V _{ICM} (DC coupled)	\leq 3.2Gbps ⁽³²⁾	670	700	730	670	700	730	mV
	85- Ω setting		85			85	—	Ω
Differential on-chip	100- Ω setting		100			100		Ω
termination resistors	120-Ω setting		120			120	—	Ω
	150-Ω setting		150			150	—	Ω
$t_{LTR}^{(33)}$	_			10		—	10	μs
$t_{LTD}^{(34)}$		4	_		4	_	—	μs
t _{LTD_manual} ⁽³⁵⁾		4			4	—		μs
$t_{LTR_LTD_manual}^{(36)}$		15			15	—	_	μs
Programmable ppm detector ⁽³⁷⁾	_	±62.5, 100, 125, 200, 250, 300, 500, and 1000					ppm	

⁽³⁰⁾ The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(31) The AC coupled $V_{ICM} = 700 \text{ mV}$ for Arria V GX and SX in PCIe mode only. The AC coupled $V_{ICM} = 750 \text{ mV}$ for Arria V GT and ST in PCIe mode only.

⁽³²⁾ For standard protocol compliance, use AC coupling.

 $^{(33)}$ t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

 $^{(34)}$ t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.

 $^{(35)}$ t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.

 $t_{\text{LTR_LTD_manual}}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.



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Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
Symbol/Description	Condition	Min	Тур	Max	Min	Тур	Max	Onit
Run length	—	—	_	200	—		200	UI
Programmable equaliza- tion AC and DC gain	AC gain setting = 0 to $3^{(38)}$ DC gain setting = 0 to 1	Refer to C Gain and Response G	TLE Respons DC Gain for at Data Rates ain for Arria	e at Data Rat Arria V GX, s ≤ 3.25 Gbps V GX, GT, S2	es > 3.25 Gbj GT, SX, and across Supp K, and ST De	ps across Sup ST Devices a orted AC Gai vices diagram	ported AC nd CTLE n and DC ns.	dB

Table 1-23: Transmitter Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
Symbol/Description	condition	Min	Тур	Max	Min	Тур	Max	Onit
Supported I/O standards				1.5 V PC	ML			
Data rate	_	611		6553.6	611	_	3125	Mbps
V _{OCM} (AC coupled)	_	_	650	_		650	_	mV
V _{OCM} (DC coupled)	\leq 3.2Gbps ⁽³²⁾	670	700	730	670	700	730	mV
	85- Ω setting	_	85	_		85	_	Ω
Differential on-chip	100- Ω setting	—	100	—	_	100	_	Ω
termination resistors	120- Ω setting		120			120		Ω
	150-Ω setting	_	150	—		150	_	Ω
Intra-differential pair skew	TX V_{CM} = 0.65 V (AC coupled) and slew rate of 15 ps	—	_	15	_	_	15	ps
Intra-transceiver block transmitter channel-to- channel skew	×6 PMA bonded mode	_	_	180	_	—	180	ps

⁽³⁷⁾ The rate match FIFO supports only up to ±300 parts per million (ppm).
 ⁽³⁸⁾ The Quartus Prime software allows AC gain setting = 3 for design with data rate between 611 Mbps and 1.25 Gbps only.



Sumbol/Decertistics	Condition	Т	Unit		
Symbol/Description	Condition	Min	Тур	Мах	Unit
Data rate (10-Gbps transceiver) ⁽⁴⁴⁾	—	0.611	_	10.3125	Gbps
Absolute $\mathrm{V}_{\mathrm{MAX}}$ for a receiver $\mathrm{pin}^{\scriptscriptstyle{(45)}}$	—	_		1.2	V
Absolute $\mathrm{V}_{\mathrm{MIN}}$ for a receiver pin	—	-0.4		—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	_	_	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	_	_	_	2.2	V
Minimum differential eye opening at the receiver serial input pins ⁽⁴⁶⁾	—	100		_	mV
V _{ICM} (AC coupled)	—	_	750 ⁽⁴⁷⁾ /800	—	mV
V _{ICM} (DC coupled)	\leq 3.2Gbps ⁽⁴⁸⁾	670	700	730	mV
	85- Ω setting		85		Ω
Differential on-chip termination	100- Ω setting		100		Ω
resistors	120- Ω setting		120		Ω
	150-Ω setting		Ω		
$t_{LTR}^{(49)}$	_	_		10	μs
$t_{LTD}^{(50)}$	—	4	—	—	μs

⁽⁴⁵⁾ The device cannot tolerate prolonged operation at this absolute maximum.



⁽⁴⁶⁾ The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

 $^{^{(47)}}$ The AC coupled $V_{\rm ICM}$ is 750 mV for PCIe mode only.

⁽⁴⁸⁾ For standard protocol compliance, use AC coupling.

 $^{^{(49)}}$ t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

⁽⁵⁰⁾ t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.

Symbol/Description	Condition	Tran	sceiver Speed Gra	Unit	
Symbol/Description	Condition	Min	Тур	Max	Ont
	85- Ω setting	—	85	—	Ω
Differential on-chip termination resistors	100- Ω setting		100	—	Ω
	120-Ω setting	—	120	—	Ω
	150-Ω setting		150	_	Ω
Intra-differential pair skew	TX V_{CM} = 0.65 V (AC coupled) and slew rate of 15 ps			15	ps
Intra-transceiver block transmitter channel-to-channel skew	×6 PMA bonded mode			180	ps
Inter-transceiver block transmitter channel-to-channel skew ⁽⁵⁵⁾	× <i>N</i> PMA bonded mode			500	ps

Table 1-30: CMU PLL Specifications for Arria V GT and ST Devices

Symbol/Description	Transceiver S	peed Grade 3	linit	
Symbol Description	Min	Max	onit	
Supported data range	0.611	10.3125	Gbps	
fPLL supported data range	611	3125	Mbps	

⁽⁵⁵⁾ This specification is only applicable to channels on one side of the device across two transceiver banks.



Typical TX V_{OD} Setting for Arria V Transceiver Channels with termination of 100 Ω

Table 1-32: Typical TX Vor	Setting for Arria V Tran	sceiver Channels with	termination of 100 Ω

Symbol	V _{OD} Setting ⁽⁵⁸⁾	V _{OD} Value (mV)	V _{OD} Setting ⁽⁵⁸⁾	V _{OD} Value (mV)
	6 ⁽⁵⁹⁾	120	34	680
	7 ⁽⁵⁹⁾	140	35	700
	8(59)	160	36	720
	9	180	37	740
	10	200	38	760
	11	220	39	780
	12	240	40	800
	13	260	41	820
	14	280	42	840
V _{OD} differential peak-to-peak typical	15	300	43	860
71	16	320	44	880
	17	340	45	900
	18	360	46	920
	19	380	47	940
	20	400	48	960
	21	420	49	980
	22	440	50	1000
	23	460	51	1020
	24	480	52	1040

⁽⁵⁸⁾ Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

⁽⁵⁹⁾ Only valid for data rates \leq 5 Gbps.



For example, when V_{OD} = 800 mV, the corresponding V_{OD} value setting is 40. The following conditions show that the 1st post tap pre-emphasis setting = 2 is valid:

- $|B| + |C| \le 60 \Rightarrow 40 + 2 = 42$ ٠
- $|B| |C| > 5 \rightarrow 40 2 = 38$
- $(V_{MAX}/V_{MIN} 1)\% < 600\% \Rightarrow (42/38 1)\% = 10.52\%$

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Arria V HSSI HSPICE models.

Table 1-33: Transmitter Pre-Emphasis Levels for Arria V Devices

Quartus Prime 1st	Quartus Prime V _{OD} Setting							
Post Tap Pre- Emphasis Setting	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	Unit
0	0	0	0	0	0	0	0	dB
1	1.97	0.88	0.43	0.32	0.24	0.19	0.13	dB
2	3.58	1.67	0.95	0.76	0.61	0.5	0.41	dB
3	5.35	2.48	1.49	1.2	1	0.83	0.69	dB
4	7.27	3.31	2	1.63	1.36	1.14	0.96	dB
5	_	4.19	2.55	2.1	1.76	1.49	1.26	dB
6	_	5.08	3.11	2.56	2.17	1.83	1.56	dB
7	_	5.99	3.71	3.06	2.58	2.18	1.87	dB
8	_	6.92	4.22	3.47	2.93	2.48	2.11	dB
9	_	7.92	4.86	4	3.38	2.87	2.46	dB
10	_	9.04	5.46	4.51	3.79	3.23	2.77	dB
11	_	10.2	6.09	5.01	4.23	3.61	_	dB
12	_	11.56	6.74	5.51	4.68	3.97	_	dB
13	_	12.9	7.44	6.1	5.12	4.36	_	dB
14	_	14.44	8.12	6.64	5.57	4.76	_	dB
15	_	_	8.87	7.21	6.06	5.14	_	dB

Arria V GX, GT, SX, and ST Device Datasheet

Altera Corporation



DPA Lock Time Specifications

Figure 1-4: Dynamic Phase Alignment (DPA) Lock Time Specifications with DPA PLL Calibration Enabled



Table 1-41: DPA Lock Time Specifications for Arria V Devices

The specifications are applicable to both commercial and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽⁸⁴⁾	Maximum Data Transition
SPI-4	00000000001111111111	2	128	640
Darallel Papid I/O	00001111	2	128	640
Parallel Rapid I/O	10010000	4	64	640
Miscellaneous	10101010	8	32	640
witscenaricous	01010101	8	32	640

⁽⁸⁴⁾ This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.





DLL Frequency Range Specifications

Table 1-43: DLL Frequency Range Specifications for Arria V Devices

Parameter	-I3, -C4	-I5, -C5	-C6	Unit
DLL operating frequency range	200 - 667	200 - 667	200 - 667	MHz

DQS Logic Block Specifications

Table 1-44: DQS Phase Shift Error Specifications for DLL-Delayed Clock (t_{DOS PSERR}) for Arria V Devices

This error specification is the absolute maximum and minimum error.

Number of DQS Delay Buffer	–I3, –C4	–I5, –C5	-C6	Unit
2	40	80	80	ps



HPS PLL Input Jitter

Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate. The divide value (N) is the value programmed into the denominator field of the VCO register for each PLL. The PLL input reference clock is divided by this value. The range of the denominator is 1 to 64.

Maximum input jitter = Input clock period × Divide value (N) × 0.02

Table 1-50: Examples of Maximum Input Jitter

Input Reference Clock Period	Divide Value (N)	Maximum Jitter	Unit
40 ns	1	0.8	ns
40 ns	2	1.6	ns
40 ns	4	3.2	ns

Quad SPI Flash Timing Characteristics

Table 1-51: Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices

Symbol	Description	Min	Тур	Max	Unit
F _{clk}	SCLK_OUT clock frequency (External clock)	_	_	108	MHz
T _{qspi_clk}	QSPI_CLK clock period (Internal reference clock)	2.32			ns
T _{dutycycle}	SCLK_OUT duty cycle	45		55	%
T _{dssfrst}	Output delay QSPI_SS valid before first clock edge		1/2 cycle of SCLK_OUT		ns
T _{dsslst}	Output delay QSPI_SS valid after last clock edge	-1		1	ns
T _{dio}	I/O data output delay	-1		1	ns
T _{din_start}	Input data valid start			$(2 + R_{delay}) \times T_{qspi_clk} - 7.52^{(85)}$	ns



Table 1-57: RGMII RX Timing Requirements for Arria V Devices

Symbol	Description	Min	Тур	Unit
T _{clk} (1000Base-T)	RX_CLK clock period		8	ns
T _{clk} (100Base-T)	RX_CLK clock period		40	ns
T _{clk} (10Base-T)	RX_CLK clock period		400	ns
T _{su}	RX_D/RX_CTL setup time	1	_	ns
T _h	RX_D/RX_CTL hold time	1		ns

Figure 1-14: RGMII RX Timing Diagram



Table 1-58: Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices

Symbol	Description	Min	Тур	Max	Unit
T _{clk}	MDC clock period	—	400	—	ns
T _d	MDC to MDIO output data delay	10		20	ns
T _s	Setup time for MDIO data	10	_	—	ns
T _h	Hold time for MDIO data	0			ns



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The Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

Arria V I/O Timing Spreadsheet

Provides the Arria V Excel-based I/O timing spreadsheet.

Programmable IOE Delay

Parameter ⁽¹¹²	Available	ble Minimum Fast Model		Slow Model				llait		
)	Settings	Offset ⁽¹¹³⁾	Industrial	Commercial	-C4	-C5	-C6	-l3	-15	
D1	32	0	0.508	0.517	0.870	1.063	1.063	0.872	1.057	ns
D3	8	0	1.763	1.795	2.999	3.496	3.571	3.031	3.643	ns
D4	32	0	0.508	0.518	0.869	1.063	1.063	1.063	1.057	ns
D5	32	0	0.508	0.517	0.870	1.063	1.063	0.872	1.057	ns

Table 1-76: I/O element (IOE) Programmable Delay for Arria V Devices

Programmable Output Buffer Delay

Table 1-77: Programmable Output Buffer Delay for Arria V Devices

This table lists the delay chain settings that control the rising and falling edge delays of the output buffer.

You can set the programmable output buffer delay in the Quartus Prime software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.



⁽¹¹²⁾ You can set this value in the Quartus Prime software by selecting **D1**, **D3**, **D4**, and **D5** in the **Assignment Name** column of **Assignment Editor**.

⁽¹¹³⁾ Minimum offset does not include the intrinsic delay.

1-96 Document Revision History

Date	Version	Changes
June 2015	2015.06.16	• Added the supported data rates for the following output standards using true LVDS output buffer types in the High-Speed I/O Specifications for Arria V Devices table:
		True RSDS output standard: data rates of up to 360 Mbps
		True mini-LVDS output standard: data rates of up to 400 Mbps
		• Added note in the condition for Transmitter—Emulated Differential I/O Standards f _{HSDR} data rate parameter in the High-Speed I/O Specifications for Arria V Devices table. Note: When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.
		Changed Queued Serial Peripheral Interface (QSPI) to Quad Serial Peripheral Interface (SPI) Flash.
		• Updated T _h location in I ² C Timing Diagram.
		 Updared T_{wp} location in NAND Address Latch Timing Diagram.
		 Corrected the unit for t_{DH} from ns to s in FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices table.
		• Updated the maximum value for t_{CO} from 4 ns to 2 ns in AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices table.
		• Moved the following timing diagrams to the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.
		FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is 1
		 FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is >1
		AS Configuration Timing Waveform
		PS Configuration Timing Waveform



1-100 Document Revision History

Date	Version	Changes
November 2012	3.0	 Updated Table 2, Table 4, Table 9, Table 14, Table 16, Table 17, Table 20, Table 21, Table 25, Table 29, Table 36, Table 56, Table 57, and Table 60. Removed table: Transceiver Block Jitter Specifications for Arria V Devices. Added HPS information: Added "HPS Specifications" section. Added Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, and Table 50. Added Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19. Updated Table 3 and Table 5.
October 2012	2.4	 Updated Arria V GX V_{CCR_GXBL/R}, V_{CCT_GXBL/R}, and V_{CCL_GXBL/R} minimum and maximum values, and data rate in Table 4. Added receiver V_{ICM} (AC coupled) and V_{ICM} (DC coupled) values, and transmitter V_{OCM} (AC coupled) and V_{OCM} (DC coupled) values in Table 20 and Table 21.
August 2012	2.3	Updated the SERDES factor condition in Table 30.
July 2012	2.2	 Updated the maximum voltage for V_I (DC input voltage) in Table 1. Updated Table 20 to include the Arria V GX -I3 speed grade. Updated the minimum value of the fixedclk clock frequency in Table 20 and Table 21. Updated the SERDES factor condition in Table 30. Updated Table 50 to include the IOE programmable delay settings for the Arria V GX -I3 speed grade.
June 2012	2.1	Updated V _{CCR_GXBL/R} , V _{CCT_GXBL/R} , and V _{CCL_GXBL/R} values in Table 4.



Symbol	Description	V _{CCIO} (V)	Typical	Unit
dR/dV		3.0	0.0297	
		2.5 0.0344 1.8 0.0499	0.0344	
	OCT variation with voltage without re-calibration		%/mV	
		1.5	0.0744	
		1.2	0.1241	
dR/dT		3.0	0.189	
		2.5 0.208	0.208	
	OCT variation with temperature without re-calibration	1.8	0.266	%/°C
		1.5	0.273	
		1.2	0.317	

Pin Capacitance

Table 2-13: Pin Capacitance for Arria V GZ Devices

Symbol	Description	Maximum	Unit
C _{IOTB}	Input capacitance on the top and bottom I/O pins	6	pF
C _{IOLR}	Input capacitance on the left and right I/O pins	6	pF
C _{OUTFB}	Input capacitance on dual-purpose clock output and feedback pins	6	pF



Table 2-19: Differential SSTL I/O Standards for Arria V GZ Devices

I/O Standard		$V_{CCIO}(V)$		V _{SWING}	_{G(DC)} (V)		V _{X(AC)} (V)		V _{SWING(AC)} (V)		
	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Мах	
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V _{CCIO} + 0.6	V _{CCIO} /2 - 0.2		V _{CCIO} /2 + 0.2	0.62	$V_{CCIO} + 0.6$	
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V _{CCIO} + 0.6	V _{CCIO} /2 - 0.175	_	V _{CCIO} /2 + 0.175	0.5	$V_{CCIO} + 0.6$	
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(127)	V _{CCIO} /2 - 0.15		V _{CCIO} /2 + 0.15	0.35	—	
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	(127)	V _{CCIO} /2 - 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	$2(V_{IL(AC)} - V_{REF})$	
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(127)	V _{CCIO} /2 - 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} - V _{REF})	_	
SSTL-12 Class I, II	1.14	1.2	1.26	0.18		V _{REF} -0.15	V _{CCIO} /2	V _{REF} + 0.15	-0.30	0.30	

Table 2-20: Differential HSTL and HSUL I/O Standards for Arria V GZ Devices

I/O Standard		۷ _{ccio} (۱	/)	V _{DIF}	_(DC) (V)		$V_{X(AC)}(V)$		V _{CM(DC)} (V)			V _{DIF(AC)} (V)	
	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Мах
HSTL-18 Class I, II	1.71	1.8	1.89	0.2		0.78		1.12	0.78	_	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68		0.9	0.4	—



 $^{^{(127)}}$ The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Switching Characteristics

Transceiver Performance Specifications

Reference Clock

Table 2-22: Reference Clock Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transce	eiver Speed	Unit				
Symbol/Description	Conditions	Min	Тур	Max	Min	Тур	Max	Onit			
Reference Clock											
Supported I/O Standards	Dedicated reference clock and HCSL 1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS,										
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS									
Input Reference Clock Frequency (CMU PLL) ⁽¹³⁷⁾	_	40		710	40		710	MHz			
Input Reference Clock Frequency (ATX PLL) ⁽¹³⁷⁾	-	100		710	100		710	MHz			

⁽¹³⁷⁾ The input reference clock frequency options depend on the data rate and the device speed grade.



Term	Definition
t _C	High-speed receiver and transmitter input and output clock period.
TCCS (channel-to- channel-skew)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t _{DUTY}	High-speed I/O block—Duty cycle on the high-speed transmitter output clock.
t _{FALL}	Signal high-to-low transition time (80-20%)
t _{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.
t _{OUTPJ_IO}	Period jitter on the general purpose I/O driven by a PLL.
t _{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL.
t _{RISE}	Signal low-to-high transition time (20-80%)
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = $1/(\text{receiver input clock frequency multiplication factor}) = t_C/w)$
V _{CM(DC)}	DC common mode input voltage.
V _{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.
V _{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
V _{DIF(AC)}	AC differential input voltage—Minimum AC input differential voltage required for switching.
V _{DIF(DC)}	DC differential input voltage— Minimum DC input differential voltage required for switching.
V _{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
V _{IH(AC)}	High-level AC input voltage
V _{IH(DC)}	High-level DC input voltage
V _{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
V _{IL(AC)}	Low-level AC input voltage
V _{IL(DC)}	Low-level DC input voltage

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