Intel - 5AGXMB1G4F31I5 Datasheet





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The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	14151
Number of Logic Elements/Cells	300000
Total RAM Bits	17358848
Number of I/O	384
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxmb1g4f31i5

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Arria V GX, GT, SX, and ST Device Datasheet



This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Arria® V devices.

Arria V devices are offered in commercial and industrial grades. Commercial devices are offered in -C4 (fastest), -C5, and -C6 speed grades. Industrial grade devices are offered in the -I3 and -I5 speed grades.

Related Information

Arria V Device Overview

Provides more information about the densities and packages of devices in the Arria V family.

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Arria V devices.

Operating Conditions

Arria V devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Arria V devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Arria V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms.

The functional operation of the device is not implied for these conditions.

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Symbol	Description	Condition	Minimum ⁽⁷⁾	Typical	Maximum ⁽⁷⁾	Unit
	HPS I/O	3.3 V	3.135	3.3	3.465	V
V _{CCPD_HPS} ⁽⁸⁾	pre-driver	3.0 V	2.85	3.0	3.15	V
	supply	2.5 V	2.375	2.5	2.625	V
		3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
	HPS I/O	2.5 V	2.375	2.5	2.625	V
V _{CCIO_HPS}	buffers power	1.8 V	1.71	1.8	1.89	V
	supply	1.5 V	1.425	1.5	1.575	V
		1.35 V ⁽⁹⁾	1.283	1.35	1.418	V
		1.2 V	1.14	1.2	1.26	V
	HPS reset	3.3 V	3.135	3.3	3.465	V
V	and clock	3.0 V	2.85	3.0	3.15	V
V CCRSTCLK_HPS	power	2.5 V	2.375	2.5	2.625	V
	supply	1.8 V	1.71	1.8	1.89	V
V _{CCPLL_HPS}	HPS PLL analog voltage regulator power supply	_	2.375	2.5	2.625	V



⁽⁷⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁸⁾ V_{CCPD_HPS} must be 2.5 V when V_{CCIO_HPS} is 2.5, 1.8, 1.5, or 1.2 V. V_{CCPD_HPS} must be 3.0 V when V_{CCIO_HPS} is 3.0 V. V_{CCPD_HPS} must be 3.3 V when V_{CCIO_HPS} is 3.3 V.

 $^{^{(9)}\,}$ V_{CCIO_HPS} 1.35 V is supported for HPS row I/O bank only.

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

I/O Standard		V _{CCIO} (V)			V _{REF} (V) V _{TT} (V)				
i/O Stanuaru	Min	Тур	Max	Min	Тур	Мах	Min	Тур	Max
SSTL-2 Class I, II	2.375	2.5	2.625	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	V _{REF} - 0.04	V _{REF}	$V_{REF} + 0.04$
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V _{REF} - 0.04	V _{REF}	$V_{REF} + 0.04$
SSTL-15 Class I, II	1.425	1.5	1.575	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
SSTL-135 Class I, II	1.283	1.35	1.418	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
SSTL-125 Class I, II	1.19	1.25	1.26	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95		V _{CCIO} /2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9		V _{CCIO} /2	_
HSTL-12 Class I, II	1.14	1.2	1.26	$0.47 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.53 \times V_{CCIO}$		V _{CCIO} /2	_
HSUL-12	1.14	1.2	1.3	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	_		

Tuble 1 15, Single Ended SSTE, 15TE, and 15OE / O hererence voltage Specifications for Anna v Devices



Symbol/Description	Condition	Transceiver Speed Grade 4			Transc	Unit		
Symbol/Description	Condition	Min	Тур	Max	Min	Тур	Max	Onit
Spread-spectrum modulating clock frequency	PCI Express [®] (PCIe)	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to -0.5%			0 to -0.5%	—	—
On-chip termination resistors	—	—	100			100	—	Ω
V _{ICM} (AC coupled)	—	_	1.1/1.15 ⁽²⁶⁾			1.1/1.15 ⁽²⁶⁾	_	V
V_{ICM} (DC coupled)	HCSL I/O standard for the PCIe reference clock	250	_	550	250		550	mV
	10 Hz	_	_	-50		_	-50	dBc/Hz
	100 Hz	_	_	-80		_	-80	dBc/Hz
Transmitter REFCLK phase	1 KHz	_	—	-110		_	-110	dBc/Hz
noise ⁽²⁷⁾	10 KHz	—	—	-120		—	-120	dBc/Hz
	100 KHz	_	_	-120		_	-120	dBc/Hz
	≥1 MHz	_	_	-130	_	_	-130	dBc/Hz
R _{REF}	_	_	2000 ±1%	_		2000 ±1%	_	Ω



⁽²⁶⁾ For data rate \leq 3.2 Gbps, connect V_{CCR_GXBL/R} to either 1.1-V or 1.15-V power supply. For data rate > 3.2 Gbps, connect V_{CCR_GXBL/R} to a 1.15-V power supply. For details, refer to the Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines.

⁽²⁷⁾ The transmitter REFCLK phase jitter is 30 ps p-p at bit error rate (BER) 10^{-12} .

Table 1-21: Transceiver Clocks Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
Symbol/Description	Condition	Min	Тур	Max	Min	Тур	Max	Onit
fixedclk clock frequency	PCIe Receiver Detect	_	125	_	_	125	_	MHz
Transceiver Reconfigura- tion Controller IP (mgmt_ clk_clk) clock frequency	_	75	_	125	75	_	125	MHz

Table 1-22: Receiver Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transc	llnit		
symbol/Description	Condition	Min	Тур	Мах	Min	Тур	Max	Onit
Supported I/O standards		1	.5 V PCML,	2.5 V PCML,	LVPECL, an	d LVDS		
Data rate ⁽²⁸⁾		611	—	6553.6	611	—	3125	Mbps
Absolute V_{MAX} for a receiver pin ⁽²⁹⁾	_		_	1.2		—	1.2	V
Absolute V _{MIN} for a receiver pin	_	-0.4	_		-0.4	—	—	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) before device configuration	_	_		1.6		_	1.6	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) after device configuration	_	_	_	2.2		_	2.2	V



 ⁽²⁸⁾ To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.
 ⁽²⁹⁾ The device cannot tolerate prolonged operation at this absolute maximum.

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
		-3 speed grade	5	—	800 ⁽⁶¹⁾	MHz
f	Input clock fraguency	-4 speed grade	5		800 ⁽⁶¹⁾	MHz
IIN	input clock nequency	–5 speed grade	5	_	750 ⁽⁶¹⁾	MHz
		-6 speed grade	5		625(61)	MHz
f _{INPFD}	Integer input clock frequency to the phase frequency detector (PFD)	_	5	_	325	MHz
f _{fINPFD}	Fractional input clock frequency to the PFD		50	_	160	MHz
		-3 speed grade	600	—	1600	MHz
f (62)	PLL voltage-controlled oscillator (VCO) operating range	-4 speed grade	600	_	1600	MHz
IVCO		–5 speed grade	600		1600	MHz
		-6 speed grade	600		1300	MHz
t _{EINDUTY}	Input clock or external feedback clock input duty cycle	_	40		60	%
		-3 speed grade	_	_	500 ⁽⁶³⁾	MHz
f	Output frequency for internal global or	-4 speed grade	—	—	500 ⁽⁶³⁾	MHz
LOUT	regional clock	-5 speed grade	_	_	500 ⁽⁶³⁾	MHz
		-6 speed grade	_	_	400 ⁽⁶³⁾	MHz



⁽⁶¹⁾ This specification is limited in the Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

⁽⁶²⁾ The VCO frequency reported by the Quartus Prime software takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

⁽⁶³⁾ This specification is limited by the lower of the two: I/O f_{MAX} or F_{OUT} of the PLL.

Memory Output Clock Jitter Specifications

Table 1-45: Memory Output Clock Jitter Specifications for Arria V Devices

The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard. The memory output clock jitter is applicable when an input jitter of 30 ps (p-p) is applied with bit error rate (BER) 10^{-12} , equivalent to 14 sigma. Altera recommends using the UniPHY intellectual property (IP) with PHYCLK connections for better jitter performance.

Daramotor	Clock Notwork	Symbol	-I3,	-C4	–15,	-C5	_(6	Unit
Falameter		Symbol	Min	Max	Min	Max	Min	Max	onit
Clock period jitter	PHYCLK	t _{JIT(per)}	-41	41	-50	50	-55	55	ps
Cycle-to-cycle period jitter	PHYCLK	t _{JIT(cc)}	6	3	9	0	9	94	ps

OCT Calibration Block Specifications

Table 1-46: OCT Calibration Block Specifications for Arria V Devices

Symbol	Description	Min	Тур	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	_		20	MHz
T _{OCTCAL}	Number of octus RCLK clock cycles required for $R_{\rm S}$ OCT/R_T OCT calibration		1000		Cycles
T _{OCTSHIFT}	Number of OCTUSRCLK clock cycles required for OCT code to shift out		32	_	Cycles
T _{RS_RT}	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	_	2.5		ns



Symbol	Description	Min	Тур	Max	Unit
T _{din_end}	Input data valid end	$(2 + R_{delay}) \times T_{qspi_clk} - 1.21^{(85)}$			ns

Figure 1-8: Quad SPI Flash Timing Diagram

This timing diagram illustrates clock polarity mode 0 and clock phase mode 0.



Related Information

Quad SPI Flash Controller Chapter, Arria V Hard Processor System Technical Reference Manual

Provides more information about Rdelay.

SPI Timing Characteristics

Table 1-52: SPI Master Timing Requirements for Arria V Devices

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

Symbol	Description	Min	Max	Unit
T _{clk}	CLK clock period	16.67	—	ns
T _{su}	SPI Master-in slave-out (MISO) setup time	8.35 (86)	—	ns

 $^{^{(85)}}$ R_{delay} is set by programming the register <code>qspiregs.rddatacap</code>. For the SoC EDS software version 13.1 and later, Altera provides automatic Quad SPI calibration in the preloader. For more information about R_{delay}, refer to the Quad SPI Flash Controller chapter in the Arria V Hard Processor System Technical Reference Manual.



1-62 SPI Timing Characteristics

Symbol	Description	Min	Max	Unit
T _h	SPI MISO hold time	1	_	ns
T _{dutycycle}	SPI_CLK duty cycle	45	55	%
T _{dssfrst}	Output delay SPI_SS valid before first clock edge	8		ns
T _{dsslst}	Output delay SPI_SS valid after last clock edge	8		ns
T _{dio}	Master-out slave-in (MOSI) output delay	-1	1	ns

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⁽⁸⁶⁾ This value is based on rx_sample_dly = 1 and spi_m_clk = 120 MHz. spi_m_clk is the internal clock that is used by SPI Master to derive it's SCLK_OUT. These timings are based on rx_sample_dly of 1. This delay can be adjusted as needed to accommodate slower response times from the slave. Note that a delay of 0 is not allowed. The setup time can be used as a reference starting point. It is very crucial to do a calibration to get the correct rx_sample_dly value because each SPI slave device may have different output delay and each application board may have different path delay. For more information about rx_sample_delay, refer to the SPI Controller chapter in the Hard Processor System Technical Reference Manual.

1-76 FPGA JTAG Configuration Timing

POR Delay	Minimum	Maximum	Unit
Standard	100	300	ms

Related Information

MSEL Pin Settings

Provides more information about POR delay based on MSEL pin settings for each configuration scheme.

FPGA JTAG Configuration Timing

Table 1-64: FPGA JTAG Timing Parameters and Values for Arria V Devices

Symbol	Description	Min	Max	Unit
t _{JCP}	TCK clock period	30, 167 ⁽⁹²⁾		ns
t _{JCH}	TCK clock high time	14		ns
t _{JCL}	TCK clock low time	14		ns
t _{JPSU (TDI)}	TDI JTAG port setup time	2		ns
t _{JPSU (TMS)}	TMS JTAG port setup time	3		ns
t _{JPH}	JTAG port hold time	5		ns
t _{JPCO}	JTAG port clock to output		12 ⁽⁹³⁾	ns
t _{JPZX}	JTAG port high impedance to valid output		14 ⁽⁹³⁾	ns
t _{JPXZ}	JTAG port valid output to high impedance		14 ⁽⁹³⁾	ns



⁽⁹²⁾ The minimum TCK clock period is 167 ns if V_{CCBAT} is within the range 1.2 V – 1.5 V when you perform the volatile key programming.

⁽⁹³⁾ A 1-ns adder is required for each VCCIO voltage step down from 3.0 V. For example, tJPCO= 13 ns if VCCIO of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

			Active Seria	 (108)	Fast Passive Parallel ⁽¹⁰⁹⁾			
Variant	Member Code	Width	DCLK (MHz)	Minimum Configura- tion Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)	
	A1	4	100	178	16	125	36	
	A3	4	100	178	16	125	36	
	A5	4	100	255	16	125	51	
Arria V CV	A7	4	100	255	16	125	51	
Arria V GX	B1	4	100	344	16	125	69	
	В3	4	100	344	16	125	69	
	B5	4	100	465	16	125	93	
	B7	4	100	465	16	125	93	
	C3	4	100	178	16	125	36	
Amia V CT	C7	4	100	255	16	125	51	
Allia v GI	D3	4	100	344	16	125	69	
	D7	4	100	465	16	125	93	
Arria V SV	В3	4	100	465	16	125	93	
AIIIa V SA	B5	4	100	465	16	125	93	
Arria V ST	D3	4	100	465	16	125	93	
AIIIa v SI	D5	4	100	465	16	125	93	

Related Information Configuration Files on page 1-83

(108) DCLK frequency of 100 MHz using external CLKUSR.
 (109) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

I/O Standard Specifications

The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL} , respectively.

Table 2-16: Single-Ended I/O Standards for Arria V GZ Devices

1/O Standard		V _{CCIO} (V)		V _{IL} (V)		V _{IH} (V)		V _{OL} (V)	V _{OH} (V)	Ι (mΔ)	Ι (m Λ)
i/O Stanuaru	Min	Тур	Max	Min	Max	Min	Max	Мах	Min	10L (1114)	10H (111A)
LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVCMOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	V _{CCIO} – 0.2	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	$0.35 \times V_{ m CCIO}$	0.65 × V _{CCIO}	V _{CCIO} + 0.3	0.45	V _{CCIO} – 0.45	2	-2
1.5 V	1.425	1.5	1.575	-0.3	$0.35 \times V_{ m CCIO}$	0.65 × V _{CCIO}	V _{CCIO} + 0.3	$0.25 imes V_{ m CCIO}$	$0.75 \times V_{CCIO}$	2	-2
1.2 V	1.14	1.2	1.26	-0.3	$0.35 \times V_{\rm CCIO}$	0.65 × V _{CCIO}	V _{CCIO} + 0.3	$0.25 \times V_{ m CCIO}$	$0.75 \times V_{CCIO}$	2	-2

Table 2-17: Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V GZ Devices

I/O Standard	V _{CCIO} (V)			V _{REF} (V)			V _{TT} (V)			
	Min	Тур	Max	Min	Тур	Max	Min	Тур	Мах	
SSTL-2 Class I, II	2.375	2.5	2.625	$0.49 \times V_{CCIO}$	$0.5 imes V_{ m CCIO}$	$0.51 imes V_{ m CCIO}$	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04	
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04	
SSTL-15 Class I, II	1.425	1.5	1.575	$0.49 \times V_{CCIO}$	$0.5 imes V_{ m CCIO}$	0.51 × V _{CCIO}	$0.49 \times V_{CCIO}$	0.5 × VCCIO	$0.51 \times V_{CCIO}$	



$V_{CCIO}(V)^{(128)}$		(128)	V _{ID} (mV) ⁽¹²⁹⁾			V _{ICM(DC)} (V)		V _{OD} (V) ⁽¹³⁰⁾		0)	V _{OCM} (V) ⁽¹³⁰⁾				
	Min	Тур	Max	Min	Condition	Max	Min	Condition	Max	Min	Тур	Max	Min	Тур	Мах
RSDS (HIO) (133)	2.375	2.5	2.625	100	V _{CM} = 1.25 V		0.3		1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini- LVDS (HIO) (134)	2.375	2.5	2.625	200	_	600	0.4	_	1.325	0.25		0.6	1	1.2	1.4
LVPECL		_	_	300		_	0.6	D _{MAX} ≤ 700 Mbps	1.8	_	_		_		
(135), (136)	_	_	_	300			1	D _{MAX} > 700 Mbps	1.6	_	_		_		

Related Information

Glossary on page 2-73



⁽¹²⁸⁾ Differential inputs are powered by VCCPD which requires 2.5 V.

⁽¹²⁹⁾ The minimum VID value is applicable over the entire common mode range, VCM.

RL range: $90 \le RL \le 110 \Omega$. (130)

⁽¹³³⁾ For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.

⁽¹³⁴⁾ For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.

⁽¹³⁵⁾ LVPECL is only supported on dedicated clock input pins.

⁽¹³⁶⁾ For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

Core Performance Specifications

Clock Tree Specifications

Table 2-33: Clock Tree Performance for Arria V GZ Devices

Symbol	Perfo	Unit	
зульог	C3, I3L	C4, I4	
Global and Regional Clock	650	580	MHz
Periphery Clock	500	500	MHz

PLL Specifications

Table 2-34: PLL Specifications for Arria V GZ Devices

Symbol	Parameter	Min	Тур	Мах	Unit
f (167)	Input clock frequency (C3, I3L speed grade)	5	—	800	MHz
IN	Input clock frequency (C4, I4 speed grade)	5	—	650	MHz
f _{INPFD}	Input frequency to the PFD	5	_	325	MHz
f _{FINPFD}	Fractional Input clock frequency to the PFD	50	_	160	MHz
f	PLL VCO operating range (C3, I3L speed grade)	600	_	1600	MHz
IVCO	PLL VCO operating range (C4, I4 speed grade)	600	—	1300	MHz
t _{EINDUTY}	Input clock or external feedback clock input duty cycle	40	_	60	%

⁽¹⁶⁷⁾ This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

⁽¹⁶⁸⁾ The VCO frequency reported by the Quartus II software in the **PLL Usage Summary** section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

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DPA Mode High-Speed I/O Specifications

Table 2-42: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Тур	Мах	Min	Тур	Мах	
DPA run length	—	_	_	10000	_		10000	UI

Figure 2-3: DPA Lock Time Specification with DPA PLL Calibration Enabled



Table 2-43: DPA Lock Time Specifications for Arria V GZ Devices

The DPA lock time is for one channel.

One data transition is defined as a 0-to-1 or 1-to-0 transition.

The DPA lock time stated in this table applies to both commercial and industrial grade.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽²⁰¹⁾	Maximum
SPI-4	0000000001111111111	2	128	640 data transitions



⁽²⁰¹⁾ This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Table 2-57: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t _{CFG}	nCONFIG low pulse width	2	_	μs
t _{STATUS}	nSTATUS low pulse width	268	1,506 (210)	μs
t _{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 (211)	μs
t _{CF2CK} ⁽²¹²⁾	nCONFIG high to first rising edge on DCLK	1,506	_	μs
t _{ST2CK} ⁽²¹²⁾	nSTATUS high to first rising edge of DCLK	2	_	μs
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5	_	ns
t _{DH}	DATA[] hold time after rising edge on DCLK	N-1/f _{DCLK} ⁽²¹³⁾		S
t _{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	_	S
t _{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$		S
t _{CLK}	DCLK period	1/f _{MAX}	_	S
f _{MAX}	DCLK frequency (FPP ×8/×16)	—	125	MHz
	DCLK frequency (FPP ×32)	—	100	MHz
t _R	Input rise time	—	40	ns
t _F	Input fall time	—	40	ns
t _{CD2UM}	CONF_DONE high to user mode ⁽²¹⁴⁾	175	437	μs

⁽²¹⁰⁾ You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

⁽²¹¹⁾ You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

 $^{(212)}$ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

 $^{(213)}$ N is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.

⁽²¹⁴⁾ The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

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Symbol	Parameter	Minimum	Maximum	Unit
t _{CO}	DCLK falling edge to AS_DATA0/ASDO output	-	4	ns
t _{SU}	Data setup time before falling edge on DCLK	1.5		ns
t _H	Data hold time after falling edge on DCLK	0	—	ns
t _{CD2UM}	CONF_DONE high to user mode ⁽²¹⁶⁾	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK}$ period	—	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (8576 × clkusr period)	_	_

Table 2-59: DCLK Frequency Specification in the AS Configuration Scheme

This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

The AS multi-device configuration scheme does not support ${\tt DCLK}$ frequency of 100 MHz.

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

Related Information

- Passive Serial Configuration Timing on page 2-67
- Configuration, Design Security, and Remote System Upgrades in Arria V Devices





⁽²¹⁶⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Passive Serial Configuration Timing

Figure 2-10: PS Configuration Timing Waveform

Timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.



Notes:

- 1. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- 2. After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.
- 3. After power-up, before and during configuration, CONF_DONE is low.
- 4. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- 5. DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the Device and Pins Option.
- 6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- 7. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.



Table 2-60: PS Timing Parameters for Arria V GZ Devices

Symbol	Parameter	Minimum	Maximum	Unit
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	_	600	ns
t _{CFG}	nCONFIG low pulse width	2		μs
t _{STATUS}	nSTATUS low pulse width	268	1,506 (217)	μs
t _{CF2ST1}	nCONFIG high to nSTATUS high		1,506 (218)	μs
t _{CF2CK} (219)	nCONFIG high to first rising edge on DCLK	1,506	—	μs
t _{ST2CK} (219)	nSTATUS high to first rising edge of DCLK	2		μs
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5		ns
t _{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t _{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t _{CL}	DCLK low time	$0.45 imes 1/f_{ m MAX}$	—	S
t _{CLK}	DCLK period	1/f _{MAX}	—	s
f _{MAX}	DCLK frequency	_	125	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽²²⁰⁾	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK}$ period	_	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (8576 × CLKUSR period) (221)	_	_

⁽²¹⁷⁾ This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.



⁽²¹⁸⁾ This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

⁽²¹⁹⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

⁽²²⁰⁾ The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

Term	Definition
t _C	High-speed receiver and transmitter input and output clock period.
TCCS (channel-to- channel-skew)	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t _{DUTY}	High-speed I/O block—Duty cycle on the high-speed transmitter output clock.
t _{FALL}	Signal high-to-low transition time (80-20%)
t _{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.
t _{OUTPJ_IO}	Period jitter on the general purpose I/O driven by a PLL.
t _{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL.
t _{RISE}	Signal low-to-high transition time (20-80%)
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = $1/(\text{receiver input clock frequency multiplication factor}) = t_C/w)$
V _{CM(DC)}	DC common mode input voltage.
V _{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.
V _{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
V _{DIF(AC)}	AC differential input voltage—Minimum AC input differential voltage required for switching.
V _{DIF(DC)}	DC differential input voltage— Minimum DC input differential voltage required for switching.
V _{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
V _{IH(AC)}	High-level AC input voltage
V _{IH(DC)}	High-level DC input voltage
V _{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
V _{IL(AC)}	Low-level AC input voltage
V _{IL(DC)}	Low-level DC input voltage

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