### Intel - 5AGXMB1G4F35I5N Datasheet





Welcome to <u>E-XFL.COM</u>

#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	14151
Number of Logic Elements/Cells	300000
Total RAM Bits	17358848
Number of I/O	544
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxmb1g4f35i5n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# Arria V GX, GT, SX, and ST Device Datasheet



This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Arria® V devices.

Arria V devices are offered in commercial and industrial grades. Commercial devices are offered in -C4 (fastest), -C5, and -C6 speed grades. Industrial grade devices are offered in the -I3 and -I5 speed grades.

#### **Related Information**

#### Arria V Device Overview

Provides more information about the densities and packages of devices in the Arria V family.

## **Electrical Characteristics**

The following sections describe the operating conditions and power consumption of Arria V devices.

## **Operating Conditions**

Arria V devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Arria V devices, you must consider the operating requirements described in this section.

### **Absolute Maximum Ratings**

This section defines the maximum operating conditions for Arria V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms.

The functional operation of the device is not implied for these conditions.

<sup>©</sup> 2017 Intel Corporation. All rights reserved. Intel, the Intel logo, Altera, Arria, Cyclone, Enpirion, MAX, NIOS, Quartus and Stratix words and logos are trademarks of Intel Corporation in the US and/or other countries. Other marks and brands may be claimed as the property of others. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.





Symbol	Description	Minimum <sup>(5)</sup>	Typical	Maximum <sup>(5)</sup>	Unit
V <sub>CCL_GXBL</sub>	GX and SX speed grades—clock network power (left side)	1 08/1 12	1 1/1 15(6)	1 14/1 18	V
V <sub>CCL_GXBR</sub>	GX and SX speed grades—clock network power (right side)	c network power		1.14/1.10	v
V <sub>CCL_GXBL</sub>	GT and ST speed grades—clock network power (left side)	117	1 20	1 22	V
V <sub>CCL_GXBR</sub>	GT and ST speed grades—clock network power (right side)	1.17	1.20	1.23	v

#### Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines

Provides more information about the power supply connection for different data rates.

#### **HPS Power Supply Operating Conditions**

#### Table 1-5: HPS Power Supply Operating Conditions for Arria V SX and ST Devices

This table lists the steady-state voltage and current values expected from Arria V system-on-a-chip (SoC) devices with ARM®-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to Recommended Operating Conditions for Arria V Devices table for the steady-state voltage values expected from the FPGA portion of the Arria V SoC devices.

Symbol	Description	Condition	Minimum <sup>(7)</sup>	Typical	Maximum <sup>(7)</sup>	Unit
	HPS core	-C4, -I5, -C5, -C6	1.07	1.1	1.13	V
V <sub>CC_HPS</sub>	voltage and periphery circuitry power supply	-I3	1.12	1.15	1.18	V

<sup>&</sup>lt;sup>(5)</sup> The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.



<sup>&</sup>lt;sup>(7)</sup> The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

		V <sub>CCIO</sub> (V)													
Parameter	Symbol	Condition	1	.2	1	.5	1	.8	2	.5	3	.0	3	.3	Unit
			Min	Мах	Min	Max	Min	Max	Min	Мах	Min	Max	Min	Max	
Bus-hold trip point	V <sub>TRIP</sub>	_	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

#### **OCT Calibration Accuracy Specifications**

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

#### Table 1-8: OCT Calibration Accuracy Specifications for Arria V Devices

Calibration accuracy for the calibrated on-chip series termination ( $R_S$  OCT) and on-chip parallel termination ( $R_T$  OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (V)		alibration Accura	су	Unit
Symbol	Description		–I3, –C4	–I5, –C5	-C6	Ont
25-Ω R <sub>S</sub>	Internal series termination with calibration (25- $\Omega$ setting)	V <sub>CCIO</sub> = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
50-Ω R <sub>S</sub>	Internal series termination with calibration (50- $\Omega$ setting)	V <sub>CCIO</sub> = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
34- $\Omega$ and 40- $\Omega$ $R_S$	Internal series termination with calibration (34- $\Omega$ and 40- $\Omega$ setting)	V <sub>CCIO</sub> = 1.5, 1.35, 1.25, 1.2	±15	±15	±15	%
48-Ω, 60-Ω, and 80- Ω R <sub>S</sub>	Internal series termination with calibration (48- $\Omega$ , 60- $\Omega$ , and 80- $\Omega$ setting)	$V_{CCIO} = 1.2$	±15	±15	±15	%
50-Ω $R_T$	Internal parallel termination with calibration (50- $\Omega$ setting)	V <sub>CCIO</sub> = 2.5, 1.8, 1.5, 1.2	-10 to +40	-10 to +40	-10 to +40	%
20- $\Omega$ , 30- $\Omega$ , 40- $\Omega$ ,60- $\Omega$ , and 120- $\Omega$ R <sub>T</sub>	Internal parallel termination with calibration (20- $\Omega$ , 30- $\Omega$ , 40- $\Omega$ , 60- $\Omega$ , and 120- $\Omega$ setting)	V <sub>CCIO</sub> = 1.5, 1.35, 1.25	-10 to +40	-10 to +40	-10 to +40	%



Symbol	Description	V <sub>CCIO</sub> (V)	Value	Unit
		3.0	0.189	
		2.5	0.208	
	OCT variation with temperature without recalibration	1.8	0.266	
dR/dT		1.5	0.273	%/°C
		1.35	0.200	
		1.25	0.200	
		1.2	0.317	

### **Pin Capacitance**

## Table 1-11: Pin Capacitance for Arria V Devices

Symbol	Description	Maximum	Unit
C <sub>IOTB</sub>	Input capacitance on top/bottom I/O pins	6	pF
C <sub>IOLR</sub>	Input capacitance on left/right I/O pins	6	pF
C <sub>OUTFB</sub>	Input capacitance on dual-purpose clock output/feedback pins	6	pF
C <sub>IOVREF</sub>	Input capacitance on V <sub>REF</sub> pins	48	pF

## **Hot Socketing**

### Table 1-12: Hot Socketing Specifications for Arria V Devices

Symbol	Description	Maximum	Unit
I <sub>IOPIN (DC)</sub>	DC current per I/O pin	300	μΑ
I <sub>IOPIN (AC)</sub>	AC current per I/O pin	8(10)	mA
I <sub>XCVR-TX (DC)</sub>	DC current per transceiver transmitter (TX) pin	100	mA

#### Arria V GX, GT, SX, and ST Device Datasheet

**Altera Corporation** 



• Transceiver Specifications for Arria V GT and ST Devices on page 1-29 Provides the specifications for transmitter, receiver, and reference clock I/O pin.

## Switching Characteristics

This section provides performance characteristics of Arria V core and periphery blocks.

## **Transceiver Performance Specifications**

## Transceiver Specifications for Arria V GX and SX Devices

#### Table 1-20: Reference Clock Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
Symbol/Description	Condition	Min	Тур	Max	Min	Тур	Max	Onit
Supported I/O standards	1.2 V PCM	L, 1.4 V PCM	IL,1.5 V PCML	, 2.5 V PCMI	., Differentia	LVPECL <sup>(23)</sup>	HCSL, and	LVDS
Input frequency from REFCLK input pins	—	27	—	710	27		710	MHz
Rise time	Measure at $\pm 60 \text{ mV of}$ differential signal <sup>(24)</sup>			400			400	ps
Fall time	Measure at $\pm 60 \text{ mV of}$ differential signal <sup>(24)</sup>	_		400	_		400	ps
Duty cycle	_	45	_	55	45	_	55	%
Peak-to-peak differential input voltage	—	200		300 <sup>(25)</sup> / 2000	200	_	300 <sup>(25)</sup> / 2000	mV



<sup>&</sup>lt;sup>(23)</sup> Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

REFCLK performance requires to meet transmitter REFCLK phase noise specification. (24)

<sup>&</sup>lt;sup>(25)</sup> The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

Symbol/Description	Condition	Tran	sceiver Speed Gra	de 3	Unit	
Symbol/Description	Condition	Min	Тур	Max	Ont	
	85- $\Omega$ setting	—	85	—	Ω	
Differential on-chip termination	100- $\Omega$ setting	—	100	—	Ω	
resistors	120-Ω setting	—	120	—	Ω	
	150-Ω setting		150	_	Ω	
Intra-differential pair skew	TX $V_{CM}$ = 0.65 V (AC coupled) and slew rate of 15 ps			15	ps	
Intra-transceiver block transmitter channel-to-channel skew	×6 PMA bonded mode			180	ps	
Inter-transceiver block transmitter channel-to-channel skew <sup>(55)</sup>	× <i>N</i> PMA bonded mode			500	ps	

## Table 1-30: CMU PLL Specifications for Arria V GT and ST Devices

Symbol/Description	Transceiver S	peed Grade 3	Unit
Symbol Description	Min	Max	onit
Supported data range	0.611	10.3125	Gbps
fPLL supported data range	611	3125	Mbps

<sup>(55)</sup> This specification is only applicable to channels on one side of the device across two transceiver banks.



Symbol	V <sub>OD</sub> Setting <sup>(58)</sup>	V <sub>OD</sub> Value (mV)	V <sub>OD</sub> Setting <sup>(58)</sup>	V <sub>OD</sub> Value (mV)
	25	500	53	1060
	26	520	54	1080
	27	540	55	1100
	28	560	56	1120
	29	580	57	1140
	30	600	58	1160
	31	620	59	1180
	32	640	60	1200
	33	660		

### **Transmitter Pre-Emphasis Levels**

The following table lists the simulation data on the transmitter pre-emphasis levels in dB for the first post tap under the following conditions:

- Low-frequency data pattern—five 1s and five 0s
- Data rate—2.5 Gbps

The levels listed are a representation of possible pre-emphasis levels under the specified conditions only and the pre-emphasis levels may change with data pattern and data rate.

Arria V devices only support 1st post tap pre-emphasis with the following conditions:

- The 1st post tap pre-emphasis settings must satisfy  $|B| + |C| \le 60$  where  $|B| = V_{OD}$  setting with termination value,  $R_{TERM} = 100 \Omega$  and |C| = 1st post tap pre-emphasis setting.
- |B| |C| > 5 for data rates < 5 Gbps and |B| |C| > 8.25 for data rates > 5 Gbps.
- $(V_{MAX}/V_{MIN} 1)\% < 600\%$ , where  $V_{MAX} = |B| + |C|$  and  $V_{MIN} = |B| |C|$ .

Exception for PCIe Gen2 design:  $V_{OD}$  setting = 43 and pre-emphasis setting = 19 are allowed for PCIe Gen2 design with transmit de-emphasis – 6dB setting (pipe\_txdeemp = 1'b0) using Altera PCIe Hard IP and PIPE IP cores.



<sup>&</sup>lt;sup>(58)</sup> Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.



Arria V GX, GT, SX, and ST Device Datasheet

**Altera Corporation** 



Date	Version	Changes
Date December 2015	Version 2015.12.16	<ul> <li>Updated Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices table.</li> <li>Updated F<sub>clk</sub>, T<sub>dutycycle</sub>, and T<sub>dssfrst</sub> specifications.</li> <li>Added T<sub>qspi_clk</sub>, T<sub>din_starb</sub>, and T<sub>din_end</sub> specifications.</li> <li>Removed T<sub>dinmax</sub> specifications.</li> <li>Updated the minimum specification for T<sub>clk</sub> to 16.67 ns and removed the maximum specification in SPI Master Timing Requirements for Arria V Devices table.</li> <li>Updated Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices table.</li> <li>Updated T<sub>clk</sub> to T<sub>sdmmc_clk_out</sub> symbol.</li> <li>Updated T<sub>sdmmc_clk_out</sub> and T<sub>d</sub> specifications.</li> <li>Added T<sub>sdmmc_clk</sub>, T<sub>su</sub>, and T<sub>h</sub> specifications.</li> <li>Removed T<sub>dinmax</sub> specifications.</li> <li>Updated the following diagrams:</li> <li>Quad SPI Flash Timing Diagram</li> <li>SD/MMC Timing Diagram</li> </ul>
		<ul> <li>Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.</li> </ul>



Symbol	Description	Minimum	Maximum	Unit
V <sub>I</sub>	DC input voltage	-0.5	3.8	V
T <sub>J</sub>	Operating junction temperature	-55	125	°C
T <sub>STG</sub>	Storage temperature (No bias)	-65	150	°C
I <sub>OUT</sub>	DC output current per pin	-25	40	mA

### Table 2-3: Transceiver Power Supply Absolute Conditions for Arria V GZ Devices

Symbol	Description	Minimum	Maximum	Unit
V <sub>CCA_GXBL</sub>	Transceiver channel PLL power supply (left side)	-0.5	3.75	V
V <sub>CCA_GXBR</sub>	Transceiver channel PLL power supply (right side)	-0.5	3.75	V
V <sub>CCHIP_L</sub>	Transceiver hard IP power supply (left side)	-0.5	1.35	V
V <sub>CCHSSI_L</sub>	Transceiver PCS power supply (left side)	-0.5	1.35	V
V <sub>CCHSSI_R</sub>	Transceiver PCS power supply (right side)	-0.5	1.35	V
V <sub>CCR_GXBL</sub>	Receiver analog power supply (left side)	-0.5	1.35	V
V <sub>CCR_GXBR</sub>	Receiver analog power supply (right side)	-0.5	1.35	V
V <sub>CCT_GXBL</sub>	Transmitter analog power supply (left side)	-0.5	1.35	V
V <sub>CCT_GXBR</sub>	Transmitter analog power supply (right side)	-0.5	1.35	V
V <sub>CCH_GXBL</sub>	Transmitter output buffer power supply (left side)	-0.5	1.8	V
V <sub>CCH_GXBR</sub>	Transmitter output buffer power supply (right side)	-0.5	1.8	V

## Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in the following table. They may also undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.



Sumbol	Description	Conditions	Calibration Ac	Unit	
Symbol	Description	Conditions	C3, I3L	C4, I4	Onit
25-Ω R <sub>S</sub>	Internal series termination with calibration (25- $\Omega$ setting)	V <sub>CCIO</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%
50-Ω R <sub>S</sub>	Internal series termination with calibration (50- $\Omega$ setting)	V <sub>CCIO</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%
34- $\Omega$ and 40- $\Omega$ $R_S$	Internal series termination with calibration (34- $\Omega$ and 40- $\Omega$ setting)	V <sub>CCIO</sub> = 1.5, 1.35, 1.25, 1.2 V	±15	±15	%
48-Ω, 60-Ω, 80-Ω, and 240-Ω R <sub>S</sub>	Internal series termination with calibration (48- $\Omega$ , 60- $\Omega$ , 80- $\Omega$ , and 240- $\Omega$ setting)	$V_{CCIO} = 1.2 V$	±15	±15	%
50- $\Omega$ R <sub>T</sub>	Internal parallel termination with calibration (50- $\Omega$ setting)	V <sub>CCIO</sub> = 2.5, 1.8, 1.5, 1.2 V	-10 to +40	-10 to +40	%
20- $\Omega$ , 30- $\Omega$ , 40- $\Omega$ , 60- $\Omega$ , and 120- $\Omega$ R <sub>T</sub>	Internal parallel termination with calibration ( $20-\Omega$ , $30-\Omega$ , $40-\Omega$ , $60-\Omega$ , and $120-\Omega$ setting)	V <sub>CCIO</sub> = 1.5, 1.35, 1.25 V	-10 to +40	-10 to +40	%
60- $\Omega$ and 120- $\Omega$ R <sub>T</sub>	Internal parallel termination with calibration (60- $\Omega$ and 120- $\Omega$ setting)	$V_{CCIO} = 1.2$	-10 to +40	-10 to +40	%
25- $\Omega R_{S\_left\_shift}$	Internal left shift series termination with calibration (25- $\Omega$ R <sub>S_left_shift</sub> setting)	V <sub>CCIO</sub> = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%

### Table 2-11: OCT Without Calibration Resistance Tolerance Specifications for Arria V GZ Devices

Symbol	Description	Conditions	Resistance	Unit	
Symbol	Description	Conditions	C3, I3L	C4, I4	Unit
25-Ω R, 50-Ω R <sub>S</sub>	Internal series termination without calibration (25- $\Omega$ setting)	V <sub>CCIO</sub> = 3.0 and 2.5 V	±40	±40	%



#### Table 2-19: Differential SSTL I/O Standards for Arria V GZ Devices

I/O Standard		$V_{CCIO}(V)$		V <sub>SWING</sub>	<sub>G(DC)</sub> (V)	V <sub>X(AC)</sub> (V)		/ <sub>X(AC)</sub> (V)		V <sub>SWING(AC)</sub> (V)
	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V <sub>CCIO</sub> + 0.6	V <sub>CCIO</sub> /2 - 0.2		V <sub>CCIO</sub> /2 + 0.2	0.62	$V_{CCIO} + 0.6$
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V <sub>CCIO</sub> + 0.6	V <sub>CCIO</sub> /2 - 0.175	_	V <sub>CCIO</sub> /2 + 0.175	0.5	$V_{CCIO} + 0.6$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(127)	V <sub>CCIO</sub> /2 - 0.15		V <sub>CCIO</sub> /2 + 0.15	0.35	_
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	(127)	V <sub>CCIO</sub> /2 - 0.15	V <sub>CCIO</sub> /2	V <sub>CCIO</sub> /2 + 0.15	2(V <sub>IH(AC)</sub> - V <sub>REF</sub> )	$2(V_{IL(AC)} - V_{REF})$
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(127)	V <sub>CCIO</sub> /2 - 0.15	V <sub>CCIO</sub> /2	V <sub>CCIO</sub> /2 + 0.15	2(V <sub>IH(AC)</sub> - V <sub>REF</sub> )	_
SSTL-12 Class I, II	1.14	1.2	1.26	0.18		V <sub>REF</sub> -0.15	V <sub>CCIO</sub> /2	V <sub>REF</sub> + 0.15	-0.30	0.30

## Table 2-20: Differential HSTL and HSUL I/O Standards for Arria V GZ Devices

V <sub>CCI</sub>		۷ <sub>ccio</sub> (۱	/)	V <sub>DIF(DC)</sub> (V)		V <sub>X(AC)</sub> (V)			V <sub>CM(DC)</sub> (V)			V <sub>DIF(AC)</sub> (V)	
	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Мах
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	_	0.78		1.12	0.78	_	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	_	0.68		0.9	0.68		0.9	0.4	—



 $<sup>^{(127)}</sup>$  The maximum value for  $V_{SWING(DC)}$  is not defined. However, each single-ended signal needs to be within the respective single-ended limits ( $V_{IH(DC)}$  and  $V_{IL(DC)}$ ).

Sumbol/Description	Conditions	Trans	ceiver Spee	d Grade 2	Transo	Unit		
Symbol/Description	Conditions	Min	Тур	Max	Min	Тур	Max	
fixedclk clock frequency	PCIe Receiver Detect	_	100 or 125	_	_	100 or 125	_	MHz
Reconfiguration clock (mgmt_clk_ clk) frequency	—	100		125	100	_	125	MHz

#### Arria V Device Overview

For more information about device ordering codes.

#### Receiver

#### Table 2-24: Receiver Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Trans	ceiver Spee	d Grade 2	Transc	Unit		
Symbol Description	Conditions	Min	Тур	Max	Min	Тур	Max	Onic
Supported I/O Standards	1.4-V PCML, 1.5-V PCML, 2.5	-V PCML,	LVPECL, a	and LVDS				
Data rate (Standard PCS) (143), (144)	—	600		9900	600	_	8800	Mbps
Data rate (10G PCS) (143), (144)	_	600		12500	600	_	10312.5	Mbps
Absolute $\mathrm{V}_{\mathrm{MAX}}$ for a receiver pin $^{(145)}$	—			1.2			1.2	V
Absolute $V_{MIN}$ for a receiver pin	_	-0.4	_		-0.4	_	_	V

<sup>&</sup>lt;sup>(143)</sup> The line data rate may be limited by PCS-FPGA interface speed grade.

<sup>(144)</sup> To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.



<sup>&</sup>lt;sup>(145)</sup> The device cannot tolerate prolonged operation at this absolute maximum.

Symbol	V <sub>OD</sub> Setting	V <sub>OD</sub> Value (mV)	V <sub>OD</sub> Setting	V <sub>OD</sub> Value (mV)
	15	300	47	940
	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
$\mathrm{V}_{\mathrm{OD}}$ differential peak to peak typical	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260



## **Core Performance Specifications**

## **Clock Tree Specifications**

### Table 2-33: Clock Tree Performance for Arria V GZ Devices

Symbol	Perfo	llait	
зульог	C3, I3L	C4, I4	
Global and Regional Clock	650	580	MHz
Periphery Clock	500	500	MHz

## **PLL Specifications**

### Table 2-34: PLL Specifications for Arria V GZ Devices

Symbol	Parameter	Min	Тур	Мах	Unit
$f_{\rm IN}^{~(167)}$	Input clock frequency (C3, I3L speed grade)	5	—	800	MHz
	Input clock frequency (C4, I4 speed grade)	5	—	650	MHz
f <sub>INPFD</sub>	Input frequency to the PFD	5	_	325	MHz
f <sub>FINPFD</sub>	Fractional Input clock frequency to the PFD	50	_	160	MHz
f <sub>VCO</sub> (168)	PLL VCO operating range (C3, I3L speed grade)	600	_	1600	MHz
	PLL VCO operating range (C4, I4 speed grade)	600	—	1300	MHz
t <sub>EINDUTY</sub>	Input clock or external feedback clock input duty cycle	40	_	60	%

<sup>(167)</sup> This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

<sup>(168)</sup> The VCO frequency reported by the Quartus II software in the **PLL Usage Summary** section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f<sub>VCO</sub> specification.

Arria V GZ Device Datasheet



t<sub>ARESET</sub>

Symbol	Parameter	Min	Тур	Max	Unit
f <sub>out</sub> (169)	Output frequency for an internal global or regional clock (C3, I3L speed grade)	_	_	650	MHz
	Output frequency for an internal global or regional clock (C4, I4 speed grade)	_		580	MHz
c (160)	Output frequency for an external clock output (C3, I3L speed grade)	_	_	667	MHz
LOUT_EXT	Output frequency for an external clock output (C4, I4 speed grade)	_	_	533	MHz
toutduty	Duty cycle for a dedicated external clock output (when set to 50%)	45	50	55	%
t <sub>FCOMP</sub>	External feedback clock compensation time	—		10	ns
f <sub>DYCONFIGCLK</sub>	Dynamic configuration clock for mgmt_clk and scanclk	_	_	100	MHz
t <sub>LOCK</sub>	Time required to lock from the end-of-device configuration or deassertion of areset		_	1	ms
t <sub>DLOCK</sub>	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/ delays)	_	—	1	ms
f <sub>CLBW</sub>	PLL closed-loop low bandwidth	_	0.3		MHz
	PLL closed-loop medium bandwidth	—	1.5		MHz
	PLL closed-loop high bandwidth (170)	_	4		MHz
t <sub>PLL_PSERR</sub>	Accuracy of PLL phase shift	_	_	±50	ps

10

\_\_\_\_

\_

Minimum pulse width on the areset signal





ns

 $<sup>^{(169)}</sup>$  This specification is limited by the lower of the two: I/O  $f_{MAX}$  or  $f_{OUT}$  of the PLL.

<sup>&</sup>lt;sup>(170)</sup> High bandwidth PLL settings are not supported in external feedback mode.

Symbol	Parameter	Min	Тур	Max	Unit
k <sub>VALUE</sub>	Numerator of Fraction	128	8388608	2147483648	—
f <sub>RES</sub>	Resolution of VCO frequency ( $f_{INPFD} = 100 \text{ MHz}$ )	390625	5.96	0.023	Hz

- Duty Cycle Distortion (DCD) Specifications on page 2-56
- DLL Range Specifications on page 2-53

## **DSP Block Specifications**

## Table 2-35: DSP Block Performance Specifications for Arria V GZ Devices

Mada	Performar	nce		Unit
Mode	C3, I3L	C4 I4		onic
Modes using One DSP Block				
Three 9 × 9	480	420		MHz
One 18 × 18	480	420	400	MHz
Two partial $18 \times 18$ (or $16 \times 16$ )	480	420 400		MHz
One 27 × 27	400	350		MHz
One 36 × 18	400	35	350	
One sum of two $18 \times 18$ (One sum of two $16 \times 16$ )	400	350		MHz
One sum of square	400	350		MHz
One $18 \times 18$ plus $36 (a \times b) + c$	400	350		MHz
Modes using Two DSP Blocks				
Three 18 × 18	400 350		MHz	
One sum of four $18 \times 18$	380	300		MHz



#### 2-44 Periphery Performance

Description	Min	Тур	Мах	Unit
Diode ideality factor	1.006	1.008	1.010	—

## **Periphery Performance**

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

**Note:** The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

#### High-Speed I/O Specification

**High-Speed Clock Specifications** 

#### Table 2-39: High-Speed Clock Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

Arria V GZ devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 230 Mbps
- True mini-LVDS output standard with data rates of up to 340 Mbps



Symbol	Conditions	C3, I3L			C4, I4			Unit
Symbol	Conditions	Min	Тур	Мах	Min	Тур	Max	
True Differential I/O Standards - f <sub>HSDRDPA</sub> (data rate)	SERDES factor J = 3 to 10 (192), (193), (194), (195), (196), (197)	150	_	1250	150	—	1050	Mbps
	SERDES factor $J \ge 4$ LVDS RX with DPA (193), (195), (196), (197)	150	_	1600	150		1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(198)	_	(199)	(198)		(199)	Mbps
	SERDES factor J = 1, uses SDR Register	(198)	_	(199)	(198)		(199)	Mbps
f <sub>HSDR</sub> (data rate)	SERDES factor $J = 3$ to 10	(198)	—	(200)	(198)	—	(200)	Mbps
	SERDES factor J = 2, uses DDR Registers	(198)	—	(199)	(198)		(199)	Mbps
	SERDES factor J = 1, uses SDR Register	(198)	—	(199)	(198)	_	(199)	Mbps

 $^{(192)}$  The  $F_{MAX}$  specification is based on the fast clock used for serial data. The interface  $F_{MAX}$  is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

<sup>(193)</sup> Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.

<sup>(194)</sup> Arria V GZ LVDS serialization and de-serialization factor needs to be x4 and above.

<sup>(195)</sup> Requires package skew compensation with PCB trace length.

<sup>(196)</sup> Do not mix single-ended I/O buffer within LVDS I/O bank.

<sup>(197)</sup> Chip-to-chip communication only with a maximum load of 5 pF.

<sup>(198)</sup> The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

<sup>(199)</sup> The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.

<sup>(200)</sup> You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.



Symbol	Parameter	Minimum	Maximum	Unit
t <sub>CD2CU</sub>	CONF_DONE high to CLKUSR enabled	$4 \times maximum$	—	_
		DCLK period		
t <sub>CD2UM</sub> C	CONF_DONE high to user mode with CLKUSR option on	t <sub>CD2CU</sub> + (8576 × CLKUSR period) (209)		_

- DCLK-to-DATA[] Ratio (r) for FPP Configuration on page 2-57 ٠
- Configuration, Design Security, and Remote System Upgrades in Arria V Devices

Arria V GZ Device Datasheet

**Altera Corporation** 



<sup>&</sup>lt;sup>(208)</sup> The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

<sup>&</sup>lt;sup>(209)</sup> To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.