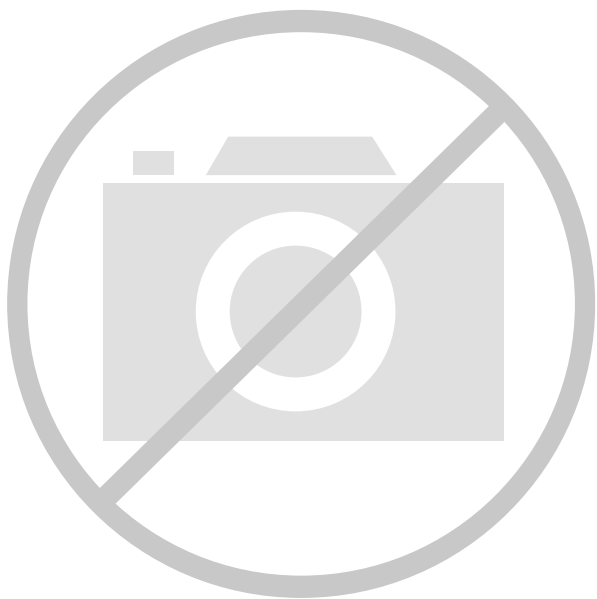




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	14151
Number of Logic Elements/Cells	300000
Total RAM Bits	17358848
Number of I/O	704
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxmb1g4f40c4n

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Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
Vi (AC)	AC input voltage	3.8	100	%
		3.85	68	%
		3.9	45	%
		3.95	28	%
		4	15	%
		4.05	13	%
		4.1	11	%
		4.15	9	%
		4.2	8	%
		4.25	7	%
		4.3	5.4	%
		4.35	3.2	%
		4.4	1.9	%
		4.45	1.1	%
		4.5	0.6	%
		4.55	0.4	%
		4.6	0.2	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Arria V devices.

Recommended Operating Conditions

Table 1-3: Recommended Operating Conditions for Arria V Devices

This table lists the steady-state voltage values expected from Arria V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	V _{CCIO} (V)	Value	Unit
dR/dT	OCT variation with temperature without recalibration	3.0	0.189	%/°C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.35	0.200	
		1.25	0.200	
		1.2	0.317	

Pin Capacitance

Table 1-11: Pin Capacitance for Arria V Devices

Symbol	Description	Maximum	Unit
C _{IOTB}	Input capacitance on top/bottom I/O pins	6	pF
C _{IOLR}	Input capacitance on left/right I/O pins	6	pF
C _{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins	6	pF
C _{IOVREF}	Input capacitance on V _{REF} pins	48	pF

Hot Socketing

Table 1-12: Hot Socketing Specifications for Arria V Devices

Symbol	Description	Maximum	Unit
I _{IOPIN} (DC)	DC current per I/O pin	300	μA
I _{IOPIN} (AC)	AC current per I/O pin	8 ⁽¹⁰⁾	mA
I _{XCVR-TX} (DC)	DC current per transceiver transmitter (TX) pin	100	mA

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-125	1.19	1.25	1.31	0.18	⁽¹⁵⁾	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$

Differential HSTL and HSUL I/O Standards

Table 1-18: Differential HSTL and HSUL I/O Standards for Arria V Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	$V_{CCIO} + 0.3$	—	$0.5 \times V_{CCIO}$	—	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$	0.3	$V_{CCIO} + 0.48$
HSUL-12	1.14	1.2	1.3	0.26	0.26	$0.5 \times V_{CCIO} - 0.12$	$0.5 \times V_{CCIO}$	$0.5 \times V_{CCIO} + 0.12$	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$	0.44	0.44

Differential I/O Standard Specifications

Table 1-19: Differential I/O Standard Specifications for Arria V Devices

Differential inputs are powered by V_{CCPD} which requires 2.5 V.

Table 1-31: Transceiver-FPGA Fabric Interface Specifications for Arria V GT and ST Devices

Symbol/Description	Transceiver Speed Grade 3		Unit
	Min	Max	
Interface speed (PMA direct mode)	50	153.6 ⁽⁵⁶⁾ , 161 ⁽⁵⁷⁾	MHz
Interface speed (single-width mode)	25	187.5	MHz
Interface speed (double-width mode)	25	163.84	MHz

Related Information

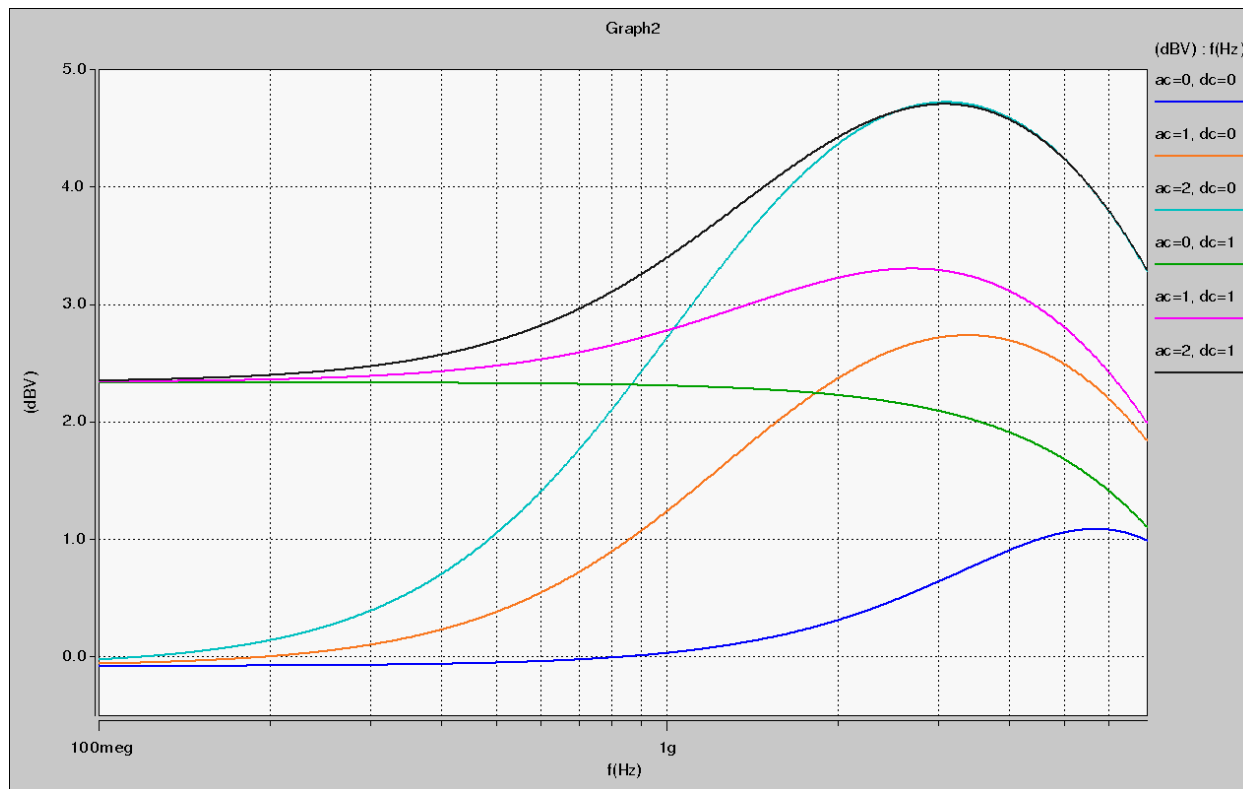
- [CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain](#) on page 1-35
- [CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain](#) on page 1-36

⁽⁵⁶⁾ The maximum frequency when core transceiver local routing is selected.

⁽⁵⁷⁾ The maximum frequency when core transceiver network routing (GCLK, RCLK, or PCLK) is selected.

CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain

Figure 1-2: Continuous Time-Linear Equalizer (CTLE) Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices



For example, when $V_{OD} = 800$ mV, the corresponding V_{OD} value setting is 40. The following conditions show that the 1st post tap pre-emphasis setting = 2 is valid:

- $|B| + |C| \leq 60 \rightarrow 40 + 2 = 42$
- $|B| - |C| > 5 \rightarrow 40 - 2 = 38$
- $(V_{MAX}/V_{MIN} - 1)\% < 600\% \rightarrow (42/38 - 1)\% = 10.52\%$

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Arria V HSSI HSPICE models.

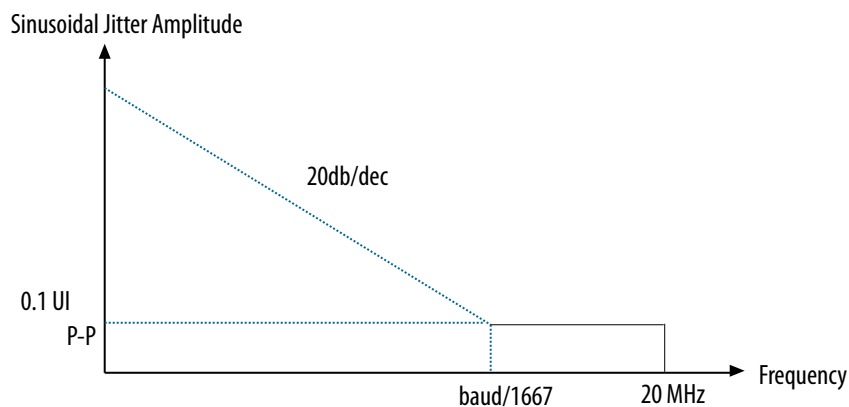
Table 1-33: Transmitter Pre-Emphasis Levels for Arria V Devices

Quartus Prime 1st Post Tap Pre-Emphasis Setting	Quartus Prime V_{OD} Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
0	0	0	0	0	0	0	0	dB
1	1.97	0.88	0.43	0.32	0.24	0.19	0.13	dB
2	3.58	1.67	0.95	0.76	0.61	0.5	0.41	dB
3	5.35	2.48	1.49	1.2	1	0.83	0.69	dB
4	7.27	3.31	2	1.63	1.36	1.14	0.96	dB
5	—	4.19	2.55	2.1	1.76	1.49	1.26	dB
6	—	5.08	3.11	2.56	2.17	1.83	1.56	dB
7	—	5.99	3.71	3.06	2.58	2.18	1.87	dB
8	—	6.92	4.22	3.47	2.93	2.48	2.11	dB
9	—	7.92	4.86	4	3.38	2.87	2.46	dB
10	—	9.04	5.46	4.51	3.79	3.23	2.77	dB
11	—	10.2	6.09	5.01	4.23	3.61	—	dB
12	—	11.56	6.74	5.51	4.68	3.97	—	dB
13	—	12.9	7.44	6.1	5.12	4.36	—	dB
14	—	14.44	8.12	6.64	5.57	4.76	—	dB
15	—	—	8.87	7.21	6.06	5.14	—	dB

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{\text{OUT_EXT}}$	Output frequency for external clock output	–3 speed grade	—	—	670 ⁽⁶³⁾	MHz
		–4 speed grade	—	—	670 ⁽⁶³⁾	MHz
		–5 speed grade	—	—	622 ⁽⁶³⁾	MHz
		–6 speed grade	—	—	500 ⁽⁶³⁾	MHz
t_{OUTDUTY}	Duty cycle for external clock output (when set to 50%)	—	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	—	10	ns
$t_{\text{DYCONFIGCLK}}$	Dynamic configuration clock for mgmt_clk and scan_clk	—	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of areset	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
f_{CLBW}	PLL closed-loop bandwidth	Low	—	0.3	—	MHz
		Medium	—	1.5	—	MHz
		High ⁽⁶⁴⁾	—	4	—	MHz
$t_{\text{PLL_PSERR}}$	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the areset signal	—	10	—	—	ns
$t_{\text{INCCJ}}^{(65)(66)}$	Input clock cycle-to-cycle jitter	$F_{\text{REF}} \geq 100 \text{ MHz}$	—	—	0.15	UI (p-p)
		$F_{\text{REF}} < 100 \text{ MHz}$	—	—	±750	ps (p-p)

⁽⁶⁴⁾ High bandwidth PLL settings are not supported in external feedback mode.⁽⁶⁵⁾ A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.⁽⁶⁶⁾ F_{REF} is f_{IN}/N , specification applies when $N = 1$.

Figure 1-6: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Less than 1.25 Gbps



DLL Frequency Range Specifications

Table 1-43: DLL Frequency Range Specifications for Arria V Devices

Parameter	-I3, -C4	-I5, -C5	-C6	Unit
DLL operating frequency range	200 – 667	200 – 667	200 – 667	MHz

DQS Logic Block Specifications

Table 1-44: DQS Phase Shift Error Specifications for DLL-Delayed Clock ($t_{\text{DQS_PSERR}}$) for Arria V Devices

This error specification is the absolute maximum and minimum error.

Number of DQS Delay Buffer	-I3, -C4	-I5, -C5	-C6	Unit
2	40	80	80	ps

Memory Output Clock Jitter Specifications

Table 1-45: Memory Output Clock Jitter Specifications for Arria V Devices

The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

The memory output clock jitter is applicable when an input jitter of 30 ps (p-p) is applied with bit error rate (BER) 10^{-12} , equivalent to 14 sigma.

Altera recommends using the UniPHY intellectual property (IP) with PHYCLK connections for better jitter performance.

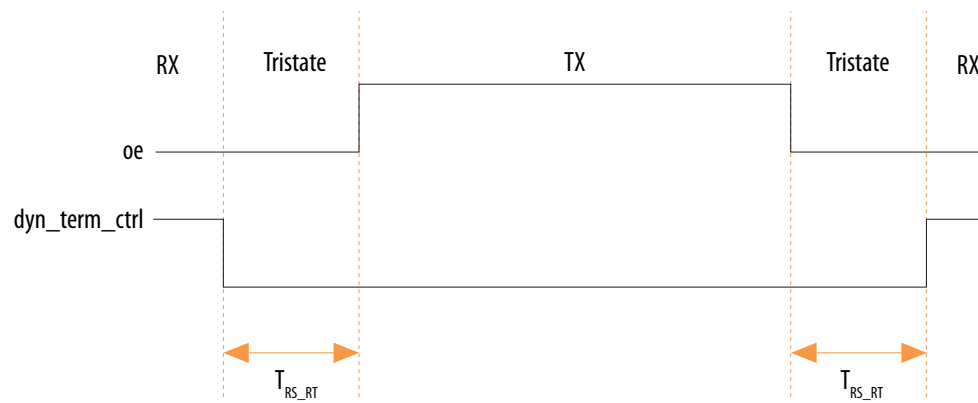
Parameter	Clock Network	Symbol	-I3, -C4		-I5, -C5		-C6		Unit
			Min	Max	Min	Max	Min	Max	
Clock period jitter	PHYCLK	$t_{JIT(per)}$	-41	41	-50	50	-55	55	ps
Cycle-to-cycle period jitter	PHYCLK	$t_{JIT(cc)}$	63		90		94		ps

OCT Calibration Block Specifications

Table 1-46: OCT Calibration Block Specifications for Arria V Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for R_S OCT/ R_T OCT calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the <code>dyn_term_ctrl</code> and <code>oe</code> signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	—	2.5	—	ns

Figure 1-7: Timing Diagram for oe and dyn_term_ctrl Signals



Duty Cycle Distortion (DCD) Specifications

Table 1-47: Worst-Case DCD on Arria V I/O Pins

The output DCD cycle only applies to the I/O buffer. It does not cover the system DCD.

Symbol	-I3, -C4		-C5, -I5		-C6		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	%

HPS Specifications

This section provides HPS specifications and timing for Arria V devices.

For HPS reset, the minimum reset pulse widths for the HPS cold and warm reset signals (HPS_nRST and HPS_nPOR) are six clock cycles of HPS_CLK1.

HPS PLL Input Jitter

Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate. The divide value (N) is the value programmed into the denominator field of the VCO register for each PLL. The PLL input reference clock is divided by this value. The range of the denominator is 1 to 64.

$$\text{Maximum input jitter} = \text{Input clock period} \times \text{Divide value (N)} \times 0.02$$

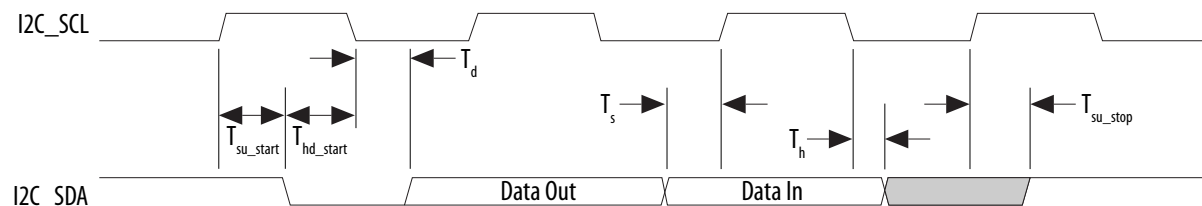
Table 1-50: Examples of Maximum Input Jitter

Input Reference Clock Period	Divide Value (N)	Maximum Jitter	Unit
40 ns	1	0.8	ns
40 ns	2	1.6	ns
40 ns	4	3.2	ns

Quad SPI Flash Timing Characteristics

Table 1-51: Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices

Symbol	Description	Min	Typ	Max	Unit
F _{clk}	SCLK_OUT clock frequency (External clock)	—	—	108	MHz
T _{qspi_clk}	QSPI_CLK clock period (Internal reference clock)	2.32	—	—	ns
T _{dutycycle}	SCLK_OUT duty cycle	45	—	55	%
T _{dssfrst}	Output delay QSPI_SS valid before first clock edge	—	1/2 cycle of SCLK_OUT	—	ns
T _{dsslst}	Output delay QSPI_SS valid after last clock edge	–1	—	1	ns
T _{dio}	I/O data output delay	–1	—	1	ns
T _{din_start}	Input data valid start	—	—	$(2 + R_{\text{delay}}) \times T_{\text{qspi_clk}} - 7.52^{(85)}$	ns

Figure 1-16: I²C Timing Diagram

NAND Timing Characteristics

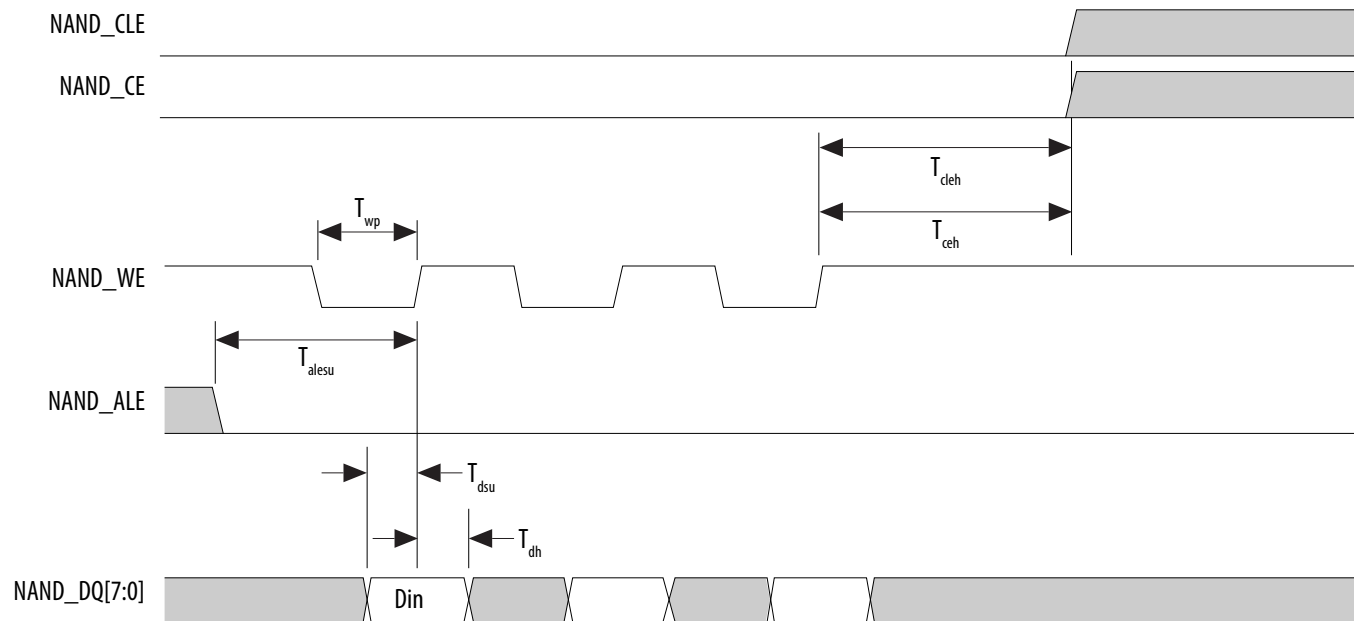
Table 1-60: NAND ONFI 1.0 Timing Requirements for Arria V Devices

The NAND controller supports Open NAND FLASH Interface (ONFI) 1.0 Mode 5 timing as well as legacy NAND devices. This table lists the requirements for ONFI 1.0 mode 5 timing. The HPS NAND controller can meet this timing by programming the C4 output of the main HPS PLL and timing registers provided in the NAND controller.

Symbol	Description	Min	Max	Unit
$T_{wp}^{(89)}$	Write enable pulse width	10	—	ns
$T_{wh}^{(89)}$	Write enable hold time	7	—	ns
$T_{rp}^{(89)}$	Read enable pulse width	10	—	ns
$T_{reh}^{(89)}$	Read enable hold time	7	—	ns
$T_{clesu}^{(89)}$	Command latch enable to write enable setup time	10	—	ns
$T_{cleh}^{(89)}$	Command latch enable to write enable hold time	5	—	ns
$T_{cesu}^{(89)}$	Chip enable to write enable setup time	15	—	ns
$T_{ceh}^{(89)}$	Chip enable to write enable hold time	5	—	ns
$T_{alesu}^{(89)}$	Address latch enable to write enable setup time	10	—	ns
$T_{aleh}^{(89)}$	Address latch enable to write enable hold time	5	—	ns
$T_{dsu}^{(89)}$	Data to write enable setup time	10	—	ns

⁽⁸⁹⁾ Timing of the NAND interface is controlled through the NAND configuration registers.

Figure 1-19: NAND Data Write Timing Diagram



Related Information

- [PowerPlay Early Power Estimator User Guide](#)
For more information about the EPE tool.
- [PowerPlay Power Analysis](#)
For more information about PowerPlay power analysis.

Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus II PowerPlay Power Analyzer feature.

Note: You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

Related Information

- [PowerPlay Early Power Estimator User Guide](#)
For more information about the EPE tool.
- [PowerPlay Power Analysis](#)
For more information about PowerPlay power analysis.

I/O Pin Leakage Current**Table 2-8: I/O Pin Leakage Current for Arria V GZ Devices**

If $V_O = V_{CCIO}$ to $V_{CCIO_{MAX}}$, 100 μA of leakage current per I/O is expected.

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_I	Input pin	$V_I = 0\text{ V to }V_{CCIO_{MAX}}$	-30	—	30	μA
I_{OZ}	Tri-stated I/O pin	$V_O = 0\text{ V to }V_{CCIO_{MAX}}$	-30	—	30	μA

I/O Standard	V _{CCIO} (V)			V _{DIF(DC)} (V)		V _{X(AC)} (V)			V _{CM(DC)} (V)			V _{DIF(AC)} (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V _{CCIO} + 0.3	—	0.5 × V _{CCIO}	—	0.4 × V _{CCIO}	0.5 × V _{CCIO}	0.6 × V _{CCIO}	0.3	V _{CCIO} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5 × V _{CCIO} - 0.12	0.5 × V _{CCIO}	0.5 × V _{CCIO} + 0.12	0.4 × V _{CCIO}	0.5 × V _{CCIO}	0.6 × V _{CCIO}	0.44	0.44

Table 2-21: Differential I/O Standard Specifications for Arria V GZ Devices

I/O Standard	V _{CCIO} (V) ⁽¹²⁸⁾			V _{ID} (mV) ⁽¹²⁹⁾			V _{ICM(DC)} (V)			V _{OD} (V) ⁽¹³⁰⁾			V _{OCM} (V) ⁽¹³⁰⁾		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to the "Transceiver Performance Specifications" section.														
2.5 V LVDS ⁽¹³¹⁾	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.05	D _{MAX} ≤ 700 Mbps	1.8	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	D _{MAX} > 700 Mbps	1.55	0.247	—	0.6	1.125	1.25	1.375
BLVDS ⁽¹³²⁾	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—	—

⁽¹²⁸⁾ Differential inputs are powered by VCCPD which requires 2.5 V.⁽¹²⁹⁾ The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.⁽¹³⁰⁾ RL range: 90 ≤ RL ≤ 110 Ω.⁽¹³¹⁾ For optimized LVDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.⁽¹³²⁾ There are no fixed V_{ICM}, V_{OD}, and V_{OCM} specifications for BLVDS. They depend on the system topology.

Core Performance Specifications

Clock Tree Specifications

Table 2-33: Clock Tree Performance for Arria V GZ Devices

Symbol	Performance		Unit
	C3, I3L	C4, I4	
Global and Regional Clock	650	580	MHz
Periphery Clock	500	500	MHz

PLL Specifications

Table 2-34: PLL Specifications for Arria V GZ Devices

Symbol	Parameter	Min	Typ	Max	Unit
$f_{IN}^{(167)}$	Input clock frequency (C3, I3L speed grade)	5	—	800	MHz
	Input clock frequency (C4, I4 speed grade)	5	—	650	MHz
f_{INPFD}	Input frequency to the PFD	5	—	325	MHz
f_{FINPFD}	Fractional Input clock frequency to the PFD	50	—	160	MHz
$f_{VCO}^{(168)}$	PLL VCO operating range (C3, I3L speed grade)	600	—	1600	MHz
	PLL VCO operating range (C4, I4 speed grade)	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%

⁽¹⁶⁷⁾ This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

⁽¹⁶⁸⁾ The VCO frequency reported by the Quartus II software in the **PLL Usage Summary** section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

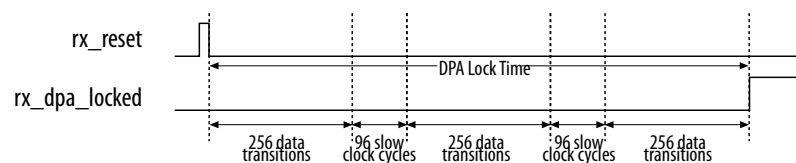
DPA Mode High-Speed I/O Specifications

Table 2-42: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
DPA run length	—	—	—	10000	—	—	10000	UI

Figure 2-3: DPA Lock Time Specification with DPA PLL Calibration Enabled**Table 2-43: DPA Lock Time Specifications for Arria V GZ Devices**

The DPA lock time is for one channel.

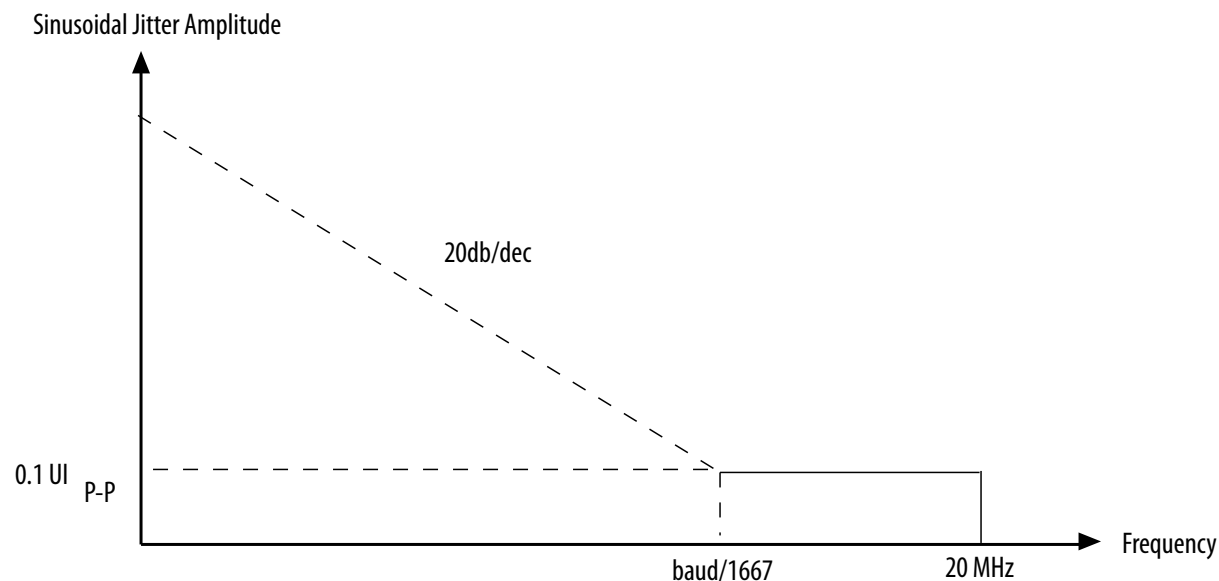
One data transition is defined as a 0-to-1 or 1-to-0 transition.

The DPA lock time stated in this table applies to both commercial and industrial grade.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽²⁰¹⁾	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions

⁽²⁰¹⁾ This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 2-5: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate < 1.25 Gbps



Non DPA Mode High-Speed I/O Specifications

Table 2-46: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Sampling Window	—	—	—	300	—	—	300	ps

Table 2-62: Uncompressed .rbf Sizes for Arria V GZ Devices

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ⁽²²³⁾
Arria V GZ	E1	137,598,880	562,208
	E3	137,598,880	562,208
	E5	213,798,880	561,760
	E7	213,798,880	561,760

Table 2-63: Minimum Configuration Time Estimation for Arria V GZ Devices

Variant	Member Code	Active Serial ⁽²²⁴⁾			Fast Passive Parallel ⁽²²⁵⁾		
		Width	DCLK (MHz)	Min Config Time (ms)	Width	DCLK (MHz)	Min Config Time (ms)
Arria V GZ	E1	4	100	344	32	100	43
	E3	4	100	344	32	100	43
	E5	4	100	534	32	100	67
	E7	4	100	534	32	100	67

Remote System Upgrades Circuitry Timing Specification

Table 2-64: Remote System Upgrade Circuitry Timing Specifications

Parameter	Minimum	Maximum	Unit
$t_{RU_nCONFIG}$ ⁽²²⁶⁾	250	—	ns
$t_{RU_nRSTIMER}$ ⁽²²⁷⁾	250	—	ns

⁽²²³⁾ The IOCSR .rbf size is specifically for the Configuration via Protocol (CvP) feature.

⁽²²⁴⁾ DCLK frequency of 100 MHz using external CLKUSR.

⁽²²⁵⁾ Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.