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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	14151
Number of Logic Elements/Cells	300000
Total RAM Bits	17358848
Number of I/O	704
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxmb1g4f40i5n

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL}[14] (mA)	I_{OH}[14] (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO}+ 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1 × V_{CCIO}	0.9 × V_{CCIO}	—	—

Differential SSTL I/O Standards

Table 1-17: Differential SSTL I/O Standards for Arria V Devices

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.2	—	$V_{CCIO}/2$ + 0.2	0.62	V_{CCIO} + 0.6
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.175	—	$V_{CCIO}/2$ + 0.175	0.5	V_{CCIO} + 0.6
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	[15]	$V_{CCIO}/2$ – 0.15	—	$V_{CCIO}/2$ + 0.15	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$
SSTL-135	1.283	1.35	1.45	0.18	[15]	$V_{CCIO}/2$ – 0.15	$V_{CCIO}/2$	$V_{CCIO}/2$ + 0.15	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$

(14) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

(15) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

- **Transceiver Specifications for Arria V GT and ST Devices** on page 1-29
  Provides the specifications for transmitter, receiver, and reference clock I/O pin.

Switching Characteristics

This section provides performance characteristics of Arria V core and periphery blocks.

Transceiver Performance Specifications

Transceiver Specifications for Arria V GX and SX Devices

Table 1-20: Reference Clock Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported I/O standards	1.2 V PCML, 1.4 V PCML,1.5 V PCML, 2.5 V PCML, Differential LVPECL[23], HCSL, and LVDS							
Input frequency from REFCLK input pins	—	27	—	710	27	—	710	MHz
Rise time	Measure at ±60 mV of differential signal[24]	—	—	400	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal[24]	—	—	400	—	—	400	ps
Duty cycle	—	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	300[25]/ 2000	200	—	300[25]/ 2000	mV

(23) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.
(24) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
(25) The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

Transceiver Specifications for Arria V GT and ST Devices

Table 1-26: Reference Clock Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O standards	1.2 V PCML, 1.4 VPCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL(40), HCSL, and LVDS				
Input frequency from REFCLK input pins	—	27	—	710	MHz
Rise time	Measure at ±60 mV of differential signal(41)	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal(41)	—	—	400	ps
Duty cycle	—	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	300(42)/2000	mV
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	Ω
V_{ICM} (AC coupled)	—	—	1.2	—	V
V_{ICM} (DC coupled)	HCSL I/O standard for the PCIe reference clock	250	—	550	mV

(40) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.
(41) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
(42) The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{CASC\_OUTPJ\_DC}$ (67)(71)	Period jitter for dedicated clock output in cascaded PLLs	$F_{OUT} \geq 100$ MHz	—	—	175	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	17.5	mUI (p-p)
t_{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 µs	—	—	—	±10	%
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	8	24	32	bits
k_{VALUE}	Numerator of fraction	—	128	8388608	2147483648	—
f_{RES}	Resolution of VCO frequency	f_{INPFD} = 100 MHz	390625	5.96	0.023	Hz

Related Information

Memory Output Clock Jitter Specifications on page 1-57
Provides more information about the external memory interface clock output jitter specifications.

(71) The cascaded PLL specification is only applicable with the following conditions:
- Upstream PLL: 0.59 MHz ≤ Upstream PLL BW < 1 MHz
- Downstream PLL: Downstream PLL BW > 2 MHz

DSP Block Performance Specifications

Table 1-37: DSP Block Performance Specifications for Arria V Devices

Mode		Performance			Unit
		–I3, –C4	–I5, –C5	–C6	
Modes using One DSP Block	Independent 9 × 9 multiplication	370	310	220	MHz
	Independent 18 × 19 multiplication	370	310	220	MHz
	Independent 18 × 25 multiplication	370	310	220	MHz
	Independent 20 × 24 multiplication	370	310	220	MHz
	Independent 27 × 27 multiplication	310	250	200	MHz
	Two 18 × 19 multiplier adder mode	370	310	220	MHz
	18 × 18 multiplier added summed with 36-bit input	370	310	220	MHz
Modes using Two DSP Blocks	Complex 18 × 19 multiplication	370	310	220	MHz

Memory Block Performance Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to 50% output duty cycle. Use the Quartus Prime software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX}.

Symbol	Condition	–I3, –C4			–I5, –C5			–C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	SERDES factor J ≥ 8[76][78], LVDS TX with RX DPA	[77]	—	1600	[77]	—	1500	[77]	—	1250	Mbps
	SERDES factor J = 1 to 2, Uses DDR Registers	[77]	—	[79]	[77]	—	[79]	[77]	—	[79]	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Network - f_{HSDR} (data rate)[80]	SERDES factor J = 4 to 10[81]	[77]	—	945	[77]	—	945	[77]	—	945	Mbps
Emulated Differential I/O Standards with One External Output Resistor Network - f_{HSDR} (data rate)[80]	SERDES factor J = 4 to 10[81]	[77]	—	200	[77]	—	200	[77]	—	200	Mbps
$t_{x\ Jitter}$ -True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps – 1.25 Gbps	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	UI

(78) The V_{CC} and V_{CCP} must be on a separate power layer and a maximum load of 5 pF for chip-to-chip interface.
(79) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}), provided you can close the design timing and the signal integrity simulation is clean.
(80) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.
(81) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

HPS PLL Input Jitter

Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate. The divide value (N) is the value programmed into the denominator field of the VCO register for each PLL. The PLL input reference clock is divided by this value. The range of the denominator is 1 to 64.

Maximum input jitter = Input clock period × Divide value (N) × 0.02

Table 1-50: Examples of Maximum Input Jitter

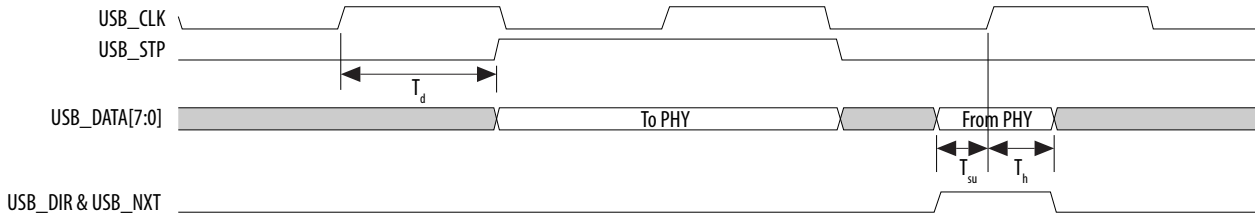
Input Reference Clock Period	Divide Value (N)	Maximum Jitter	Unit
40 ns	1	0.8	ns
40 ns	2	1.6	ns
40 ns	4	3.2	ns

Quad SPI Flash Timing Characteristics

Table 1-51: Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices

Symbol	Description	Min	Typ	Max	Unit
F_{clk}	SCLK_OUT clock frequency (External clock)	—	—	108	MHz
T_{qspi_clk}	QSPI_CLK clock period (Internal reference clock)	2.32	—	—	ns
$T_{dutycycle}$	SCLK_OUT duty cycle	45	—	55	%
$T_{dssfrst}$	Output delay QSPI_SS valid before first clock edge	—	1/2 cycle of SCLK_OUT	—	ns
T_{dsslst}	Output delay QSPI_SS valid after last clock edge	–1	—	1	ns
T_{dio}	I/O data output delay	–1	—	1	ns
T_{din_start}	Input data valid start	—	—	$(2 + R_{delay}) \times T_{qspi\_clk} - 7.52$ (85)	ns

Figure 1-12: USB Timing Diagram

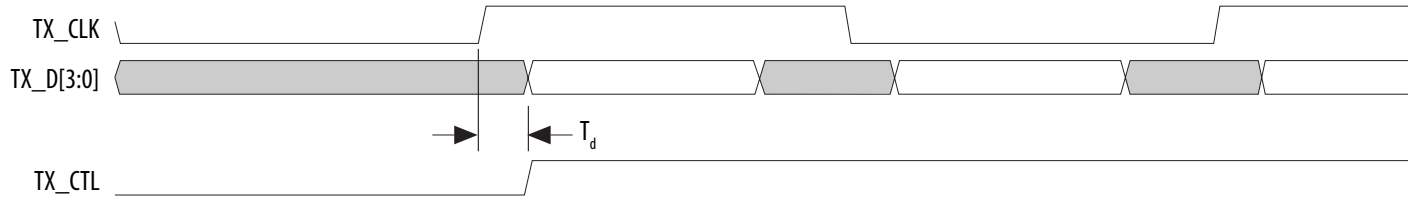


Ethernet Media Access Controller (EMAC) Timing Characteristics

Table 1-56: Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements for Arria V Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	TX_CLK clock period	—	8	—	ns
T_{clk} (100Base-T)	TX_CLK clock period	—	40	—	ns
T_{clk} (10Base-T)	TX_CLK clock period	—	400	—	ns
$T_{dutycycle}$	TX_CLK duty cycle	45	—	55	%
T_d	TX_CLK to TXD/TX_CTL output data delay	–0.85	—	0.15	ns

Figure 1-13: RGMII TX Timing Diagram



FPP Configuration Timing when DCLK-to-DATA[] >1

Table 1-67: FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506(98)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506(99)	µs
t_{CF2CK}(100)	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}(100)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N - 1/f_{DCLK}$(101)	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/ ×16)	—	125	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode(102)	175	437	µs

(98) This value can be obtained if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(99) This value can be obtained if you do not delay configuration by externally holding nSTATUS low.
(100) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.
(101) N is the DCLK-to-DATA[] ratio and f_{DCLK} is the DCLK frequency of the system.
(102) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Date	Version	Changes

January 2015	2015.01.30	• Updated the description for $V_{CC\_AUX\_SHARED}$ to "HPS auxiliary power supply" in the following tables:
		  • Absolute Maximum Ratings for Arria V Devices
		  • HPS Power Supply Operating Conditions for Arria V SX and ST Devices
		• Added statement in I/O Standard Specifications: You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.
		• Updated the conditions for transceiver reference clock rise time and fall time: Measure at ±60 mV of differential signal. Added a note to the conditions: `REFCLK` performance requires to meet transmitter `REFCLK` phase noise specification.
		• Updated the description in Periphery Performance Specifications to mention that proper timing closure is required in design.
		• Updated HPS Clock Performance main_base_clk specifications from 525 MHz (for –I3 speed grade) and 462 MHz (for –C4 speed grade) to 400 MHz.
		• Updated HPS PLL VCO maximum frequency to 1,600 MHz (for –C5, –I5, and –C6 speed grades), 1,850 MHz (for –C4 speed grade), and 2,100 MHz (for –I3 speed grade).
		• Changed the symbol for HPS PLL input jitter divide value from NR to N.
		• Removed "Slave select pulse width (Texas Instruments SSP mode)" parameter from the following tables:
		  • SPI Master Timing Requirements for Arria V Devices
		  • SPI Slave Timing Requirements for Arria V Devices
		• Added descriptions to USB Timing Characteristics section in HPS Specifications: PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board.
		• Added HPS JTAG timing specifications.
		• Updated FPGA JTAG timing specifications note as follows: A 1-ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, t_{JPCO} = 13 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.
		• Updated the value in the V_{ICM} (AC Coupled) row and in note 6 from 650 mV to 750 mV in the Transceiver Specifications for Arria V GT and ST Devices table.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle.

For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

Table 2-4: Maximum Allowed Overshoot During Transitions for Arria V GZ Devices

Symbol	Description	Condition (V)	Overshoot Duration as % @ T_J = 100°C	Unit
Vi (AC)	AC input voltage	3.8	100	%
		3.85	64	%
		3.9	36	%
		3.95	21	%
		4	12	%
		4.05	7	%
		4.1	4	%
		4.15	2	%
		4.2	1	%

Recommended Operating Conditions

Table 2-5: Recommended Operating Conditions for Arria V GZ Devices

Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum(114)	Typical	Maximum (114)	Unit
V_{CC}	Core voltage and periphery circuitry power supply (115)	—	0.82	0.85	0.88	V

(114) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(115) The V_{CC} core supply must be set to 0.9 V if the Partial Reconfiguration (PR) feature is used.

Symbol	V_{OD} Setting	V_{OD} Value (mV)	V_{OD} Setting	V_{OD} Value (mV)
V_{OD} **differential peak to peak typical**	15	300	47	940
	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260

Mode	Performance			Unit
	C3, I3L	C4	I4	
One sum of two 27 × 27	380	300	290	MHz
One sum of two 36 × 18	380	300		MHz
One complex 18 × 18	400	350		MHz
One 36 × 36	380	300		MHz
Modes using Three DSP Blocks				
One complex 18 × 25	340	275	265	MHz
Modes using Four DSP Blocks				
One complex 27 × 27	350	310		MHz

Memory Block Specifications

Table 2-36: Memory Block Performance Specifications for Arria V GZ Devices

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.

Memory	Mode	Resources Used		Performance				Unit
		ALUTs	Memory	C3	C4	I3L	I4	
MLAB	Single port, all supported widths	0	1	400	315	400	315	MHz
	Simple dual-port, x32/x64 depth	0	1	400	315	400	315	MHz
	Simple dual-port, x16 depth (178)	0	1	533	400	533	400	MHz
	ROM, all supported widths	0	1	500	450	500	450	MHz

(178) The F_{MAX} specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

DPA Mode High-Speed I/O Specifications

Table 2-42: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
DPA run length	—	—	—	10000	—	—	10000	UI

Figure 2-3: DPA Lock Time Specification with DPA PLL Calibration Enabled

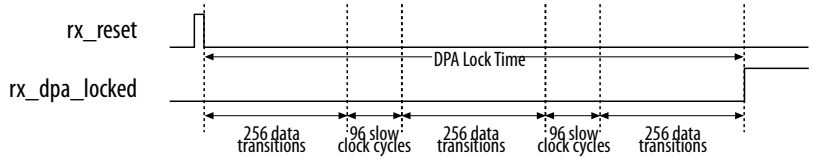


Table 2-43: DPA Lock Time Specifications for Arria V GZ Devices

The DPA lock time is for one channel.

One data transition is defined as a 0-to-1 or 1-to-0 transition.

The DPA lock time stated in this table applies to both commercial and industrial grade.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions (201)	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions

(201) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

DLL Range Specifications

Table 2-47: DLL Range Specifications for Arria V GZ Devices

Arria V GZ devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Parameter	C3, I3L	C4, I4	Unit
DLL operating frequency range	300 – 890	300 – 890	MHz

DQS Logic Block Specifications

Table 2-48: DQS Phase Offset Delay Per Setting for Arria V GZ Devices

The typical value equals the average of the minimum and maximum values.

The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a –3 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 11 ps) ± 20 ps] = 735 ps ± 20 ps.

Speed Grade	Min	Max	Unit
C3, I3L	8	15	ps
C4, I4	8	16	ps

Table 2-49: DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria V GZ Devices

This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a –3 speed grade is ±84 ps or ±42 ps.

Number of DQS Delay Buffers	C3, I3L	C4, I4	Unit
1	30	32	ps
2	60	64	ps
3	90	96	ps

Number of DQS Delay Buffers	C3, I3L	C4, I4	Unit
4	120	128	ps

Memory Output Clock Jitter Specifications

Table 2-50: Memory Output Clock Jitter Specification for Arria V GZ Devices

The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

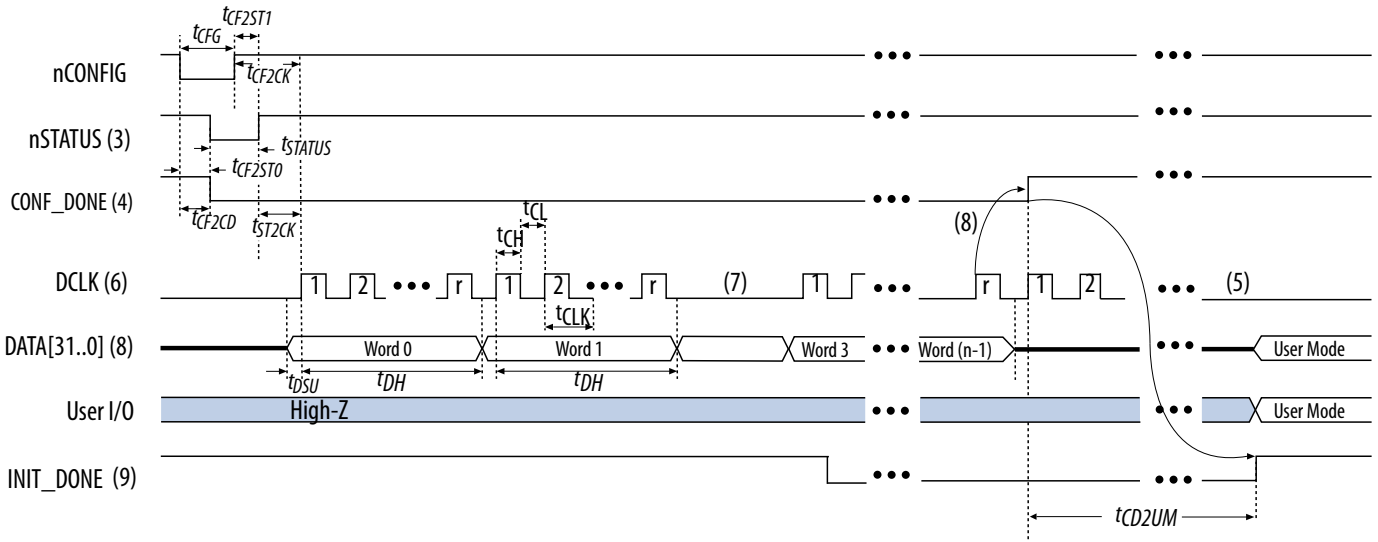
The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

Clock Network	Parameter	Symbol	C3, I3L		C4, I4		Unit
			Min	Max	Min	Max	
Regional	Clock period jitter	$t_{JIT(per)}$	–55	55	–55	55	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	–110	110	–110	110	ps
	Duty cycle jitter	$t_{JIT(duty)}$	–82.5	82.5	–82.5	82.5	ps
Global	Clock period jitter	$t_{JIT(per)}$	–82.5	82.5	–82.5	82.5	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	–165	165	–165	165	ps
	Duty cycle jitter	$t_{JIT(duty)}$	–90	90	–90	90	ps
PHY Clock	Clock period jitter	$t_{JIT(per)}$	–30	30	–35	35	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	–60	60	–70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	–45	45	–56	56	ps

FPP Configuration Timing when DCLK to DATA[] > 1

Figure 2-8: FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 ,

Timing when using a MAX II device, MAX V device, or microprocessor as an external host.



Notes:

1. To find out the DCLK-to-DATA[] ratio for your system, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
2. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
3. After power-up, the Arria V GZ device holds nSTATUS low for the time as specified by the POR delay.
4. After power-up, before and during configuration, CONF_DONE is low.
5. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
6. "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
7. If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31..0] pins prior to sending the first DCLK rising edge.
8. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
9. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 2-57: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1

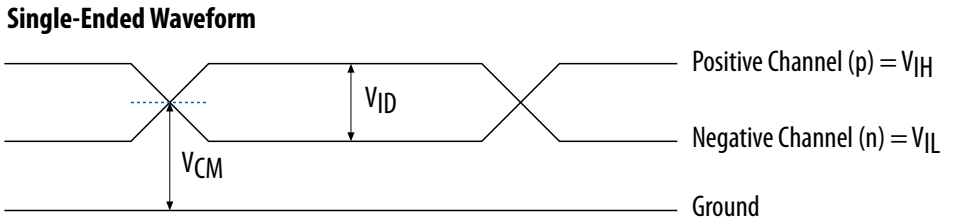
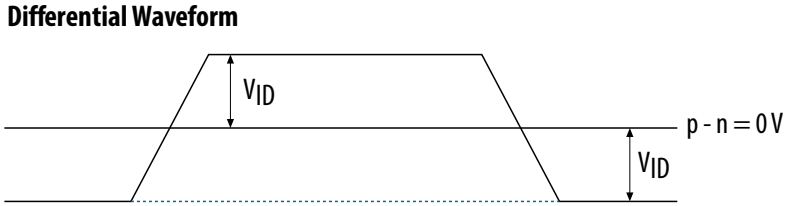
Use these timing parameters when you use the decompression and design security features.

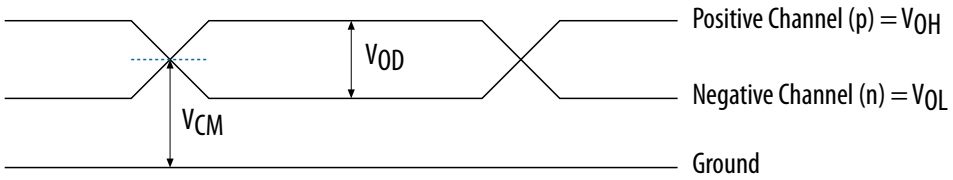
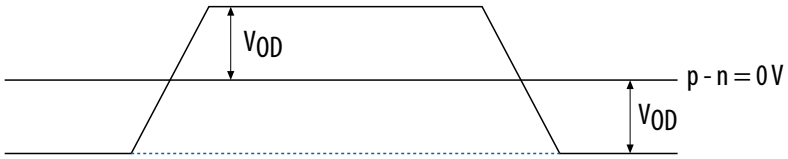
Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1,506 (210)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 (211)	µs
t_{CF2CK} (212)	nCONFIG high to first rising edge on DCLK	1,506	—	µs
t_{ST2CK} (212)	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N-1/f_{DCLK}$ (213)	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16)	—	125	MHz
	DCLK frequency (FPP ×32)	—	100	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode (214)	175	437	µs

(210) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(211) You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.
(212) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.
(213) N is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.
(214) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

Glossary

Table 2-68: Glossary

Term	Definition
Differential I/O Standards	Receiver Input Waveforms   Transmitter Output Waveforms

Term	Definition
	Single-Ended Waveform  **Differential Waveform** 
f_{HSCLK}	Left and right PLL input clock frequency.
f_{HSDR}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	High-speed I/O block—Maximum and minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
J	High-speed I/O block—Deserialization factor (width of parallel data bus).