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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	14151
Number of Logic Elements/Cells	300000
Total RAM Bits	17358848
Number of I/O	384
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxmb1g6f31c6n

Symbol	Description	Condition	Minimum ⁽¹⁾	Typical	Maximum ⁽¹⁾	Unit
V_{CC}	Core voltage power supply	–C4, –I5, –C5, –C6	1.07	1.1	1.13	V
		–I3	1.12	1.15	1.18	V
V_{CCP}	Periphery circuitry, PCIe hard IP block, and transceiver PCS power supply	–C4, –I5, –C5, –C6	1.07	1.1	1.13	V
		–I3	1.12	1.15	1.18	V
V_{CCPGM}	Configuration pins power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
V_{CC_AUX}	Auxiliary supply	—	2.375	2.5	2.625	V
$V_{CCBAT}^{(2)}$	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V
$V_{CCPD}^{(3)}$	I/O pre-driver power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V

⁽¹⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽²⁾ If you do not use the design security feature in Arria V devices, connect V_{CCBAT} to a 1.5-V, 2.5-V, or 3.0-V power supply. Arria V power-on reset (POR) circuitry monitors V_{CCBAT} . Arria V devices do not exit POR if V_{CCBAT} is not powered up.

⁽³⁾ V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25, or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V. V_{CCPD} must be 3.3 V when V_{CCIO} is 3.3 V.

Symbol	Description	V _{CCIO} (V)	Value	Unit
dR/dT	OCT variation with temperature without recalibration	3.0	0.189	%/ ^o C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.35	0.200	
		1.25	0.200	
		1.2	0.317	

Pin Capacitance

Table 1-11: Pin Capacitance for Arria V Devices

Symbol	Description	Maximum	Unit
C _{IOTB}	Input capacitance on top/bottom I/O pins	6	pF
C _{IOLR}	Input capacitance on left/right I/O pins	6	pF
C _{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins	6	pF
C _{IOVREF}	Input capacitance on V _{REF} pins	48	pF

Hot Socketing

Table 1-12: Hot Socketing Specifications for Arria V Devices

Symbol	Description	Maximum	Unit
I _{IOPIN} (DC)	DC current per I/O pin	300	μA
I _{IOPIN} (AC)	AC current per I/O pin	8 ⁽¹⁰⁾	mA
I _{XCVR-TX} (DC)	DC current per transceiver transmitter (TX) pin	100	mA

Protocol	Sub-protocol	Data Rate (Mbps)
Common Public Radio Interface (CPRI)	CPRI E6LV	614.4
	CPRI E6HV	614.4
	CPRI E6LVII	614.4
	CPRI E12LV	1,228.8
	CPRI E12HV	1,228.8
	CPRI E12LVII	1,228.8
	CPRI E24LV	2,457.6
	CPRI E24LVII	2,457.6
	CPRI E30LV	3,072
	CPRI E30LVII	3,072
	CPRI E48LVII	4,915.2
	CPRI E60LVII	6,144
	CPRI E96LVIII ⁽⁶⁰⁾	9,830.4
Gbps Ethernet (GbE)	GbE 1250	1,250
OBSAI	OBSAI 768	768
	OBSAI 1536	1,536
	OBSAI 3072	3,072
	OBSAI 6144	6,144
Serial digital interface (SDI)	SDI 270 SD	270
	SDI 1485 HD	1,485
	SDI 2970 3G	2,970

⁽⁶⁰⁾ You can achieve compliance with TX channel restriction of one HSSI channel per six-channel transceiver bank.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{\text{OUTPJ_DC}}^{(67)}$	Period jitter for dedicated clock output in integer PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	175	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	17.5	mUI (p-p)
$t_{\text{FOUTPJ_DC}}^{(67)}$	Period jitter for dedicated clock output in fractional PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	250 ⁽⁶⁸⁾ , 175 ⁽⁶⁹⁾	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	25 ⁽⁶⁸⁾ , 17.5 ⁽⁶⁹⁾	mUI (p-p)
$t_{\text{OUTCCJ_DC}}^{(67)}$	Cycle-to-cycle jitter for dedicated clock output in integer PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	175	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	17.5	mUI (p-p)
$t_{\text{FOUTCCJ_DC}}^{(67)}$	Cycle-to-cycle jitter for dedicated clock output in fractional PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	250 ⁽⁶⁸⁾ , 175 ⁽⁶⁹⁾	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	25 ⁽⁶⁸⁾ , 17.5 ⁽⁶⁹⁾	mUI (p-p)
$t_{\text{OUTPJ_IO}}^{(67)(70)}$	Period jitter for clock output on a regular I/O in integer PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	600	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	60	mUI (p-p)
$t_{\text{FOUTPJ_IO}}^{(67)(68)(70)}$	Period jitter for clock output on a regular I/O in fractional PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	600	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	60	mUI (p-p)
$t_{\text{OUTCCJ_IO}}^{(67)(70)}$	Cycle-to-cycle jitter for clock output on a regular I/O in integer PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	600	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	60	mUI (p-p)
$t_{\text{FOUTCCJ_IO}}^{(67)(68)(70)}$	Cycle-to-cycle jitter for clock output on a regular I/O in fractional PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	600	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	60	mUI (p-p)

⁽⁶⁷⁾ Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Memory Output Clock Jitter Specification for Arria V Devices table.

⁽⁶⁸⁾ This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05–0.95 must be $\geq 1000 \text{ MHz}$.

⁽⁶⁹⁾ This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.20–0.80 must be $\geq 1200 \text{ MHz}$.

⁽⁷⁰⁾ External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Arria V Devices table.

Symbol		Condition	-I3, -C4			-I5, -C5			-C6			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	TCCS	True Differential I/O Standards	—	—	150	—	—	150	—	—	150	ps
		Emulated Differential I/O Standards	—	—	300	—	—	300	—	—	300	ps
Receiver	True Differential I/O Standards - f_{HSDRDPA} (data rate)	SERDES factor J = 3 to 10 ⁽⁷⁶⁾	150	—	1250	150	—	1250	150	—	1050	Mbps
		SERDES factor J ≥ 8 with DPA ⁽⁷⁶⁾⁽⁷⁸⁾	150	—	1600	150	—	1500	150	—	1250	Mbps
	f_{HSDR} (data rate)	SERDES factor J = 3 to 10	⁽⁷⁷⁾	—	⁽⁸³⁾	⁽⁷⁷⁾	—	⁽⁸³⁾	⁽⁷⁷⁾	—	⁽⁸³⁾	Mbps
		SERDES factor J = 1 to 2, uses DDR registers	⁽⁷⁷⁾	—	⁽⁷⁹⁾	⁽⁷⁷⁾	—	⁽⁷⁹⁾	⁽⁷⁷⁾	—	⁽⁷⁹⁾	Mbps
DPA Mode	DPA run length	—	—	—	10000	—	—	10000	—	—	10000	UI
Soft-CDR Mode	Soft-CDR ppm tolerance	—	—	—	300	—	—	300	—	—	300	±ppm
Non-DPA Mode	Sampling Window	—	—	—	300	—	—	300	—	—	300	ps

⁽⁸³⁾ You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

DPA Lock Time Specifications

Figure 1-4: Dynamic Phase Alignment (DPA) Lock Time Specifications with DPA PLL Calibration Enabled

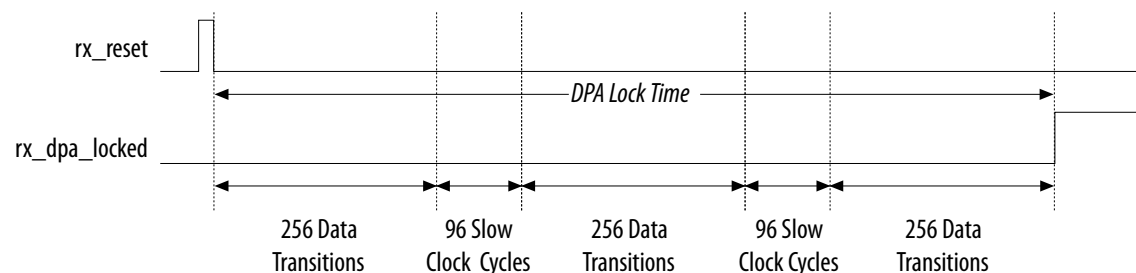


Table 1-41: DPA Lock Time Specifications for Arria V Devices

The specifications are applicable to both commercial and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽⁸⁴⁾	Maximum Data Transition
SPI-4	00000000001111111111	2	128	640
Parallel Rapid I/O	00001111	2	128	640
	10010000	4	64	640
Miscellaneous	10101010	8	32	640
	01010101	8	32	640

⁽⁸⁴⁾ This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

HPS PLL Input Jitter

Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate. The divide value (N) is the value programmed into the denominator field of the VCO register for each PLL. The PLL input reference clock is divided by this value. The range of the denominator is 1 to 64.

$$\text{Maximum input jitter} = \text{Input clock period} \times \text{Divide value (N)} \times 0.02$$

Table 1-50: Examples of Maximum Input Jitter

Input Reference Clock Period	Divide Value (N)	Maximum Jitter	Unit
40 ns	1	0.8	ns
40 ns	2	1.6	ns
40 ns	4	3.2	ns

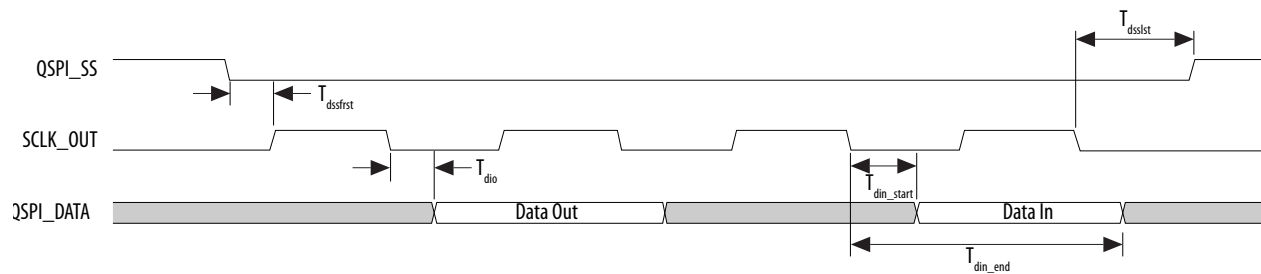
Quad SPI Flash Timing Characteristics**Table 1-51: Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices**

Symbol	Description	Min	Typ	Max	Unit
F _{clk}	SCLK_OUT clock frequency (External clock)	—	—	108	MHz
T _{qspi_clk}	QSPI_CLK clock period (Internal reference clock)	2.32	—	—	ns
T _{dutycycle}	SCLK_OUT duty cycle	45	—	55	%
T _{dssfst}	Output delay QSPI_SS valid before first clock edge	—	1/2 cycle of SCLK_OUT	—	ns
T _{dsslst}	Output delay QSPI_SS valid after last clock edge	–1	—	1	ns
T _{dio}	I/O data output delay	–1	—	1	ns
T _{din_start}	Input data valid start	—	—	$(2 + R_{\text{delay}}) \times T_{\text{qspi_clk}} - 7.52^{(85)}$	ns

Symbol	Description	Min	Typ	Max	Unit
T_{din_end}	Input data valid end	$(2 + R_{delay}) \times T_{qspi_clk} - 1.21^{(85)}$	—	—	ns

Figure 1-8: Quad SPI Flash Timing Diagram

This timing diagram illustrates clock polarity mode 0 and clock phase mode 0.



Related Information

[Quad SPI Flash Controller Chapter, Arria V Hard Processor System Technical Reference Manual](#)

Provides more information about Rdelay.

SPI Timing Characteristics

Table 1-52: SPI Master Timing Requirements for Arria V Devices

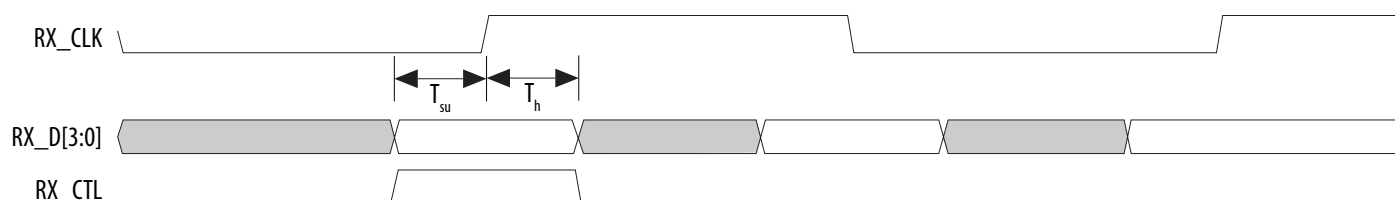
The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

Symbol	Description	Min	Max	Unit
T_{clk}	CLK clock period	16.67	—	ns
T_{su}	SPI Master-in slave-out (MISO) setup time	8.35 ⁽⁸⁶⁾	—	ns

⁽⁸⁵⁾ R_{delay} is set by programming the register `qspiregs.rddatacap`. For the SoC EDS software version 13.1 and later, Altera provides automatic Quad SPI calibration in the preloader. For more information about R_{delay} , refer to the Quad SPI Flash Controller chapter in the Arria V Hard Processor System Technical Reference Manual.

Table 1-57: RGMII RX Timing Requirements for Arria V Devices

Symbol	Description	Min	Typ	Unit
T_{clk} (1000Base-T)	RX_CLK clock period	—	8	ns
T_{clk} (100Base-T)	RX_CLK clock period	—	40	ns
T_{clk} (10Base-T)	RX_CLK clock period	—	400	ns
T_{su}	RX_D/RX_CTL setup time	1	—	ns
T_h	RX_D/RX_CTL hold time	1	—	ns

Figure 1-14: RGMII RX Timing Diagram**Table 1-58: Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices**

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	MDC clock period	—	400	—	ns
T_d	MDC to MDIO output data delay	10	—	20	ns
T_s	Setup time for MDIO data	10	—	—	ns
T_h	Hold time for MDIO data	0	—	—	ns

POR Delay	Minimum	Maximum	Unit
Standard	100	300	ms

Related Information**MSEL Pin Settings**

Provides more information about POR delay based on MSEL pin settings for each configuration scheme.

FPGA JTAG Configuration Timing

Table 1-64: FPGA JTAG Timing Parameters and Values for Arria V Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30, 167 ⁽⁹²⁾	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
t_{JPSU} (TDI)	TDI JTAG port setup time	2	—	ns
t_{JPSU} (TMS)	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	12 ⁽⁹³⁾	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 ⁽⁹³⁾	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 ⁽⁹³⁾	ns

⁽⁹²⁾ The minimum TCK clock period is 167 ns if V_{CCBAT} is within the range 1.2 V – 1.5 V when you perform the volatile key programming.

⁽⁹³⁾ A 1-ns adder is required for each VCCIO voltage step down from 3.0 V. For example, t_{JPCO} = 13 ns if VCCIO of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

FPP Configuration Timing

DCLK-to-DATA[] Ratio (r) for FPP Configuration

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP $\times 16$ where the r is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

Table 1-65: DCLK-to-DATA[] Ratio for Arria V Devices

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
FPP (8-bit wide)	Off	Off	1
	On	Off	1
	Off	On	2
	On	On	2
FPP (16-bit wide)	Off	Off	1
	On	Off	2
	Off	On	4
	On	On	4

FPP Configuration Timing when DCLK-to-DATA[] = 1

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP $\times 8$ and FPP $\times 16$. For the respective DCLK-to-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Arria V Devices table.

Table 1-66: FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Arria V Devices

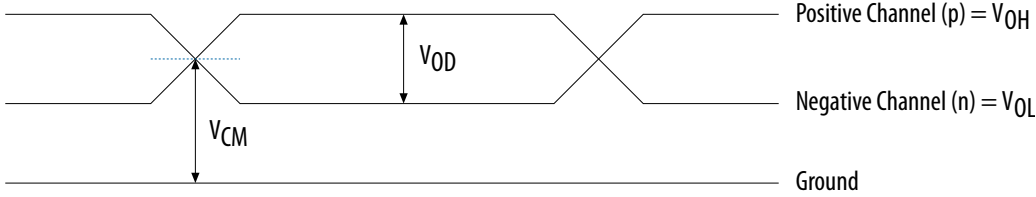
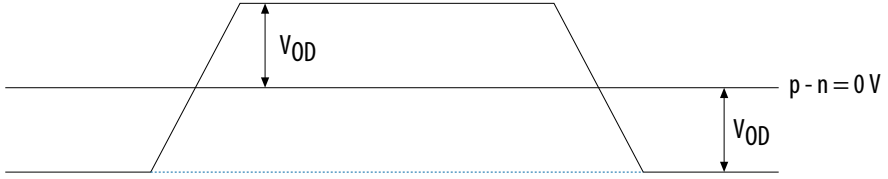
Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	μ s

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)
Arria V GX	A1	71,015,712	439,960
	A3	71,015,712	439,960
	A5	101,740,800	446,360
	A7	101,740,800	446,360
	B1	137,785,088	457,368
	B3	137,785,088	457,368
	B5	185,915,808	463,128
	B7	185,915,808	463,128
Arria V GT	C3	71,015,712	439,960
	C7	101,740,800	446,360
	D3	137,785,088	457,368
	D7	185,915,808	463,128
Arria V SX	B3	185,903,680	450,968
	B5	185,903,680	450,968
Arria V ST	D3	185,903,680	450,968
	D5	185,903,680	450,968

Minimum Configuration Time Estimation

Table 1-73: Minimum Configuration Time Estimation for Arria V Devices

The estimated values are based on the configuration .rbf sizes in Uncompressed .rbf Sizes for Arria V Devices table.

Term	Definition
	Transmitter Output Waveforms Single-Ended Waveform  Positive Channel (p) = V_{OH} Negative Channel (n) = V_{OL} Ground Differential Waveform  V_{OD} $p - n = 0\text{ V}$
f_{HCLK}	Left/right PLL input clock frequency.
f_{HSDR}	High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDR} = 1/TUI$), non-DPA.
$f_{HSDRDPA}$	High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA} = 1/TUI$), DPA.
J	High-speed I/O block—Deserialization factor (width of parallel data bus).

Symbol	Description	Minimum	Maximum	Unit
V_I	DC input voltage	-0.5	3.8	V
T_J	Operating junction temperature	-55	125	°C
T_{STG}	Storage temperature (No bias)	-65	150	°C
I_{OUT}	DC output current per pin	-25	40	mA

Table 2-3: Transceiver Power Supply Absolute Conditions for Arria V GZ Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CCA_GXBL}	Transceiver channel PLL power supply (left side)	-0.5	3.75	V
V_{CCA_GXBR}	Transceiver channel PLL power supply (right side)	-0.5	3.75	V
V_{CCHIP_L}	Transceiver hard IP power supply (left side)	-0.5	1.35	V
V_{CCHSSI_L}	Transceiver PCS power supply (left side)	-0.5	1.35	V
V_{CCHSSI_R}	Transceiver PCS power supply (right side)	-0.5	1.35	V
V_{CCR_GXBL}	Receiver analog power supply (left side)	-0.5	1.35	V
V_{CCR_GXBR}	Receiver analog power supply (right side)	-0.5	1.35	V
V_{CCT_GXBL}	Transmitter analog power supply (left side)	-0.5	1.35	V
V_{CCT_GXBR}	Transmitter analog power supply (right side)	-0.5	1.35	V
V_{CCH_GXBL}	Transmitter output buffer power supply (left side)	-0.5	1.8	V
V_{CCH_GXBR}	Transmitter output buffer power supply (right side)	-0.5	1.8	V

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in the following table. They may also undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{ICM} (AC and DC coupled)	$V_{CCR_GXB} = 0.85\text{ V}$ full bandwidth	—	600	—	—	600	—	mV
	$V_{CCR_GXB} = 0.85\text{ V}$ half bandwidth	—	600	—	—	600	—	mV
	$V_{CCR_GXB} = 1.0\text{ V}$ full bandwidth	—	700	—	—	700	—	mV
	$V_{CCR_GXB} = 1.0\text{ V}$ half bandwidth	—	700	—	—	700	—	mV
$t_{LTR}^{(149)}$	—	—	—	10	—	—	10	μs
$t_{LTD}^{(150)}$	—	4	—	—	4	—	—	μs
$t_{LTD_manual}^{(151)}$	—	4	—	—	4	—	—	μs
$t_{LTR_LTD_manual}^{(152)}$	—	15	—	—	15	—	—	μs
Programmable equalization (AC Gain)	Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz)	—	—	16	—	—	16	dB

⁽¹⁴⁹⁾ t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

⁽¹⁵⁰⁾ t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedto data` signal goes high.

⁽¹⁵¹⁾ t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedto data` signal goes high when the CDR is functioning in the manual mode.

⁽¹⁵²⁾ $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedto ref` signal goes high when the CDR is functioning in the manual mode.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{\text{OUTPJ_IO}}^{(173), (175)}$	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{\text{FOUTPJ_IO}}^{(173), (175), (176)}$	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{\text{OUTCCJ_IO}}^{(173), (175)}$	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{\text{FOUTCCJ_IO}}^{(173), (175), (176)}$	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{\text{CASC_OUTPJ_DC}}^{(173), (177)}$	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{\text{OUT}} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{\text{OUT}} < 100$ MHz)	—	—	17.5	mUI (p-p)
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits

⁽¹⁷⁵⁾ The external memory interface clock output jitter specifications use a different measurement method, which is available in the "Memory Output Clock Jitter Specification for Arria V GZ Devices" table.

⁽¹⁷⁶⁾ This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05–0.95 must be ≥ 1000 MHz.

⁽¹⁷⁷⁾ The cascaded PLL specification is only applicable with the following condition:

- Upstream PLL: $0.59\text{MHz} \leq \text{Upstream PLL BW} < 1$ MHz
- Downstream PLL: $\text{Downstream PLL BW} > 2$ MHz

Figure 2-4: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate ≥ 1.25 Gbps

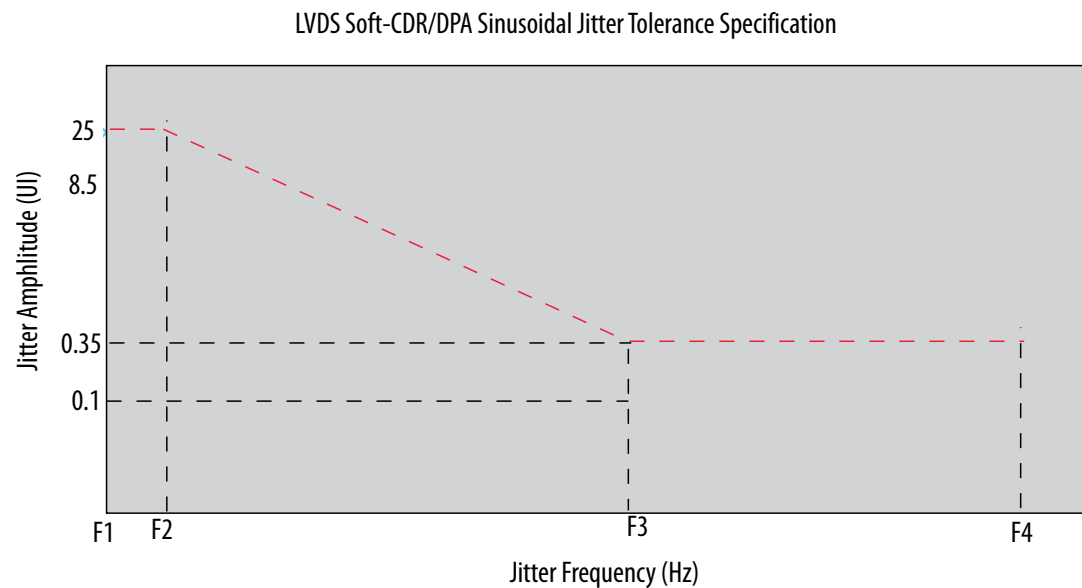


Table 2-45: LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate ≥ 1.25 Gbps

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Note: When you enable the decompression or design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8, FPP ×16, and FPP ×32. For the respective DCLK-to-DATA[] ratio, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.

Table 2-56: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1

Use these timing parameters when the decompression and design security features are disabled.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	μs
t_{STATUS}	nSTATUS low pulse width	268	1,506 ⁽²⁰⁵⁾	μs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽²⁰⁶⁾	μs
t_{CF2CK} (207)	nCONFIG high to first rising edge on DCLK	1,506	—	μs
t_{ST2CK} ⁽²⁰⁷⁾	nSTATUS high to first rising edge of DCLK	2	—	μs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16)	—	125	MHz
	DCLK frequency (FPP ×32)	—	100	MHz
t_{CD2UM}	CONF_DONE high to user mode ⁽²⁰⁸⁾	175	437	μs

⁽²⁰⁵⁾ This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

⁽²⁰⁶⁾ This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

⁽²⁰⁷⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Symbol	Parameter	Minimum	Maximum	Unit
t _{CO}	DCLK falling edge to AS_DATA0/ASDO output	—	4	ns
t _{SU}	Data setup time before falling edge on DCLK	1.5	—	ns
t _H	Data hold time after falling edge on DCLK	0	—	ns
t _{CD2UM}	CONF_DONE high to user mode ⁽²¹⁶⁾	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (8576 × CLKUSR period)	—	—

Table 2-59: DCLK Frequency Specification in the AS Configuration Scheme

This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

Related Information

- [Passive Serial Configuration Timing](#) on page 2-67
- [Configuration, Design Security, and Remote System Upgrades in Arria V Devices](#)

⁽²¹⁶⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the “Initialization” section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Programmable IOE Delay

Table 2-66: IOE Programmable Delay for Arria V GZ Devices

Parameter ⁽²²⁸⁾	Available Settings	Min Offset ⁽²²⁹⁾	Fast Model		Slow Model				Unit
			Industrial	Commercial	C3	C4	I3L	I4	
D1	64	0	0.464	0.493	0.924	1.011	0.921	1.006	ns
D2	32	0	0.230	0.244	0.459	0.503	0.456	0.500	ns
D3	8	0	1.587	1.699	2.992	3.192	3.047	3.257	ns
D4	64	0	0.464	0.492	0.924	1.011	0.920	1.006	ns
D5	64	0	0.464	0.493	0.924	1.011	0.921	1.006	ns
D6	32	0	0.229	0.244	0.458	0.503	0.456	0.499	ns

Programmable Output Buffer Delay

Table 2-67: Programmable Output Buffer Delay for Arria V GZ Devices

You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

Symbol	Parameter	Typical	Unit
D _{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

⁽²²⁸⁾ You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D4**, **D5**, and **D6** in the **Assignment Name** column of **Assignment Editor**.

⁽²²⁹⁾ Minimum offset does not include the intrinsic delay.