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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	17110
Number of Logic Elements/Cells	362000
Total RAM Bits	19822592
Number of I/O	384
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxmb3g4f31i5n

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1-1: Absolute Maximum Ratings for Arria V Devices

Symbol	Description	Minimum	Maximum	Unit
V _{CC}	Core voltage power supply	-0.50	1.43	V
V _{CCP}	Periphery circuitry, PCIe [®] hardIP block, and transceiver physical coding sublayer (PCS) power supply	-0.50	1.43	V
V _{CCPGM}	Configuration pins power supply	-0.50	3.90	V
V _{CC_AUX}	Auxiliary supply	-0.50	3.25	V
V _{CCBAT}	Battery back-up power supply for design security volatile key register	-0.50	3.90	V
V _{CCPD}	I/O pre-driver power supply	-0.50	3.90	V
V _{CCIO}	I/O power supply	-0.50	3.90	V
V _{CCD_FPLL}	Phase-locked loop (PLL) digital power supply	-0.50	1.80	V
V _{CCA_FPLL}	PLL analog power supply	-0.50	3.25	V
V _{CCA_GXB}	Transceiver high voltage power	-0.50	3.25	V
V _{CCH_GXB}	Transmitter output buffer power	-0.50	1.80	V
V _{CCR_GXB}	Receiver power	-0.50	1.50	V
V _{CCT_GXB}	Transmitter power	-0.50	1.50	V
V _{CCL_GXB}	Transceiver clock network power	-0.50	1.50	V
VI	DC input voltage	-0.50	3.80	V
V _{CC_HPS}	HPS core voltage and periphery circuitry power supply	-0.50	1.43	V
V _{CCPD_HPS}	HPS I/O pre-driver power supply	-0.50	3.90	V
V _{CCIO_HPS}	HPS I/O power supply	-0.50	3.90	V
V _{CCRSTCLK_HPS}	HPS reset and clock input pins power supply	-0.50	3.90	V



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Symbol	Description	Condition	Minimum ⁽¹⁾	Typical	Maximum ⁽¹⁾	Unit
V	Coro voltago powor supply	-C4, -I5, -C5, -C6	1.07	1.1	1.13	V
V CC	Core voltage power suppry	-I3	1.12	1.15	1.18	V
V	Periphery circuitry, PCIe hard IP block,	-C4, -I5, -C5, -C6	1.07	1.1	1.13	V
V CCP	and transceiver PCS power supply	-I3	1.12	1.15	1.18	V
		3.3 V	3.135	3.3	3.465	V
V	Configuration pine power supply	3.0 V	2.85	3.0	3.15	V
V CCPGM	Configuration plus power supply	2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
V _{CC_AUX}	Auxiliary supply	_	2.375	2.5	2.625	V
V _{CCBAT} ⁽²⁾	Battery back-up power supply	_	1.2	—	3.0	V
	(For design security volatile key register)					
		3.3 V	3.135	3.3	3.465	V
V _{CCPD} ⁽³⁾	I/O pre-driver power supply	3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V

⁽¹⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(2) If you do not use the design security feature in Arria V devices, connect V_{CCBAT} to a 1.5-V, 2.5-V, or 3.0-V power supply. Arria V power-on reset (POR) circuitry monitors V_{CCBAT}. Arria V devices do not exit POR if V_{CCBAT} is not powered up.



⁽³⁾ V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25, or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V. V_{CCPD} must be 3.3 V when V_{CCIO} is 3.3 V.

Transceiver Power Supply Operating Conditions

Table '	1-4:	Transceiver	Power S	upply	Operating	Conditions	for Arria V Devices	j
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Symbol	Description	Minimum ⁽⁵⁾	Typical	Maximum ⁽⁵⁾	Unit	
V _{CCA_GXBL}	Transceiver high voltage power (left side)	2 275	2 500	2 625	V	
V _{CCA_GXBR}	Transceiver high voltage power (right side)	2.575	2.300	2.025	v	
V _{CCR_GXBL}	GX and SX speed grades—receiver power (left side)	1.08/1.12	1 1/1 15(6)	1 14/1 18	V	
V _{CCR_GXBR}	GX and SX speed grades—receiver power (right side)	1.00/1.12	1.1/1.13	1.14/1.10	v	
V _{CCR_GXBL}	GT and ST speed grades—receiver power (left side)	1 17	1 20	1 23	V	
V _{CCR_GXBR}	GT and ST speed grades—receiver power (right side)		1.20	1.23	v	
V _{CCT_GXBL}	GX and SX speed grades—transmitter power (left side)	1.08/1.12	1 1/1 15(6)	1 14/1 18	V	
V _{CCT_GXBR}	GX and SX speed grades—transmitter power (right side)	1.00/1.12	1.1/1.15	1.14/1.10	V	
V _{CCT_GXBL}	GT and ST speed grades—transmitter power (left side)	1 17	1 20	1 23	V	
V _{CCT_GXBR}	GT and ST speed grades—transmitter power (right side)	1.17	1.20	1.23	V	
V _{CCH_GXBL}	Transmitter output buffer power (left side)	1 /25	1 500	1 575	V	
V _{CCH_GXBR}	Transmitter output buffer power (right side)	1.423	1.300	1.375	V	

⁽⁵⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁶⁾ For data rate <=3.2 Gbps, connect V_{CCR_GXBL/R}, V_{CCT_GXBL/R}, or V_{CCL_GXBL/R} to either 1.1-V or 1.15-V power supply. For data rate >3.2 Gbps, connect V_{CCR_GXBL/R}, V_{CCT_GXBL/R}, or V_{CCL_GXBL/R} to a 1.15-V power supply. For details, refer to the Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines.



1/O Standard	V _{CCIO} (V)			V _{SWING(DC)} (V)			$V_{X(AC)}(V)$		V _{SWING(AC)} (V)		
	Min	Тур	Max	Min	Мах	Min	Тур	Max	Min	Max	
SSTL-125	1.19	1.25	1.31	0.18	(15)	V _{CCIO} /2 – 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} – V _{REF})	$2(V_{IL(AC)} - V_{REF})$	

Differential HSTL and HSUL I/O Standards

Table 1-18: Differential HSTL and HSUL I/O Standards for Arria V Devices

I/O Standard	V _{CCIO} (V)		V _{DIF(DC)} (V)		V _{X(AC)} (V)			V _{CM(DC)} (V)			V _{DIF(AC)} (V)		
	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Мах
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	_	0.78	_	1.12	0.78	_	1.12	0.4	_
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V _{CCIO} + 0.3	_	$0.5 imes V_{ m CCIO}$		$0.4 \times V_{ m CCIO}$	$0.5 imes V_{ m CCIO}$	$0.6 \times V_{ m CCIO}$	0.3	V _{CCIO} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	$\begin{array}{c} 0.5 \times \\ V_{\rm CCIO} - \\ 0.12 \end{array}$	0.5 × V _{CCIO}	$\begin{array}{c} 0.5 \times \\ \mathrm{V}_{\mathrm{CCIO}} \\ + \ 0.12 \end{array}$	$0.4 \times V_{\rm CCIO}$	0.5 × V _{CCIO}	0.6 × V _{CCIO}	0.44	0.44

Differential I/O Standard Specifications

Table 1-19: Differential I/O Standard Specifications for Arria V Devices

Differential inputs are powered by V_{CCPD} which requires 2.5 V.



I/O Standard	V _{CCIO} (V)			V _{ID} (mV) ⁽¹⁶⁾		V _{ICM(DC)} (V)		V _{OD} (V) ⁽¹⁷⁾			V _{OCM} (V) ⁽¹⁷⁾⁽¹⁸⁾				
	Min	Тур	Мах	Min	Condition	Max	Min	Condition	Max	Min	Тур	Max	Min	Тур	Max
PCML	Transmitter, receiver, and input reference clock pins of high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Transceiver Specifications for Arria V GX and SX Devices and Transceiver Specifications for Arria V GT and ST Devices tables.														
2.5 V	2 375	2.5	2 625	100	V _{CM} =		0.05	D _{MAX} ≤ 1.25 Gbps	1.80	0.247		0.6	1 125	1 25	1 375
LVDS ⁽¹⁹⁾	LVDS ⁽¹⁹⁾ 2.375 2.5 2.625	100	1.25 V	1.05	D _{MAX} > 1.25 Gbps	1.55	5.217		0.0	1.125	1.25	1.575			
RSDS (HIO) ⁽²⁰⁾	2.375	2.5	2.625	100	V _{CM} = 1.25 V	_	0.25		1.45	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO) ⁽²¹⁾	2.375	2.5	2.625	200		600	0.300	_	1.425	0.25	_	0.6	1	1.2	1.4
				200			0.60	D _{MAX} ≤ 700 Mbps	1.80						
LVPECL ⁽²²⁾			500			1.00	D _{MAX} > 700 Mbps	1.60							

Related Information

- Transceiver Specifications for Arria V GX and SX Devices on page 1-23 Provides the specifications for transmitter, receiver, and reference clock I/O pin.
- $^{(16)}$ The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.
- ⁽¹⁷⁾ $R_{\rm L}$ range: $90 \le R_{\rm L} \le 110 \ \Omega$.
- ⁽¹⁸⁾ This applies to default pre-emphasis setting only.
- ⁽¹⁹⁾ For optimized LVDS receiver performance, the receiver voltage input range must be within 1.0 V to 1.6 V for data rates above 1.25 Gbps and 0 V to 1.85 V for data rates below 1.25 Gbps.
- ⁽²⁰⁾ For optimized RSDS receiver performance, the receiver voltage input range must be within 0.25 V to 1.45 V.
- ⁽²¹⁾ For optimized Mini-LVDS receiver performance, the receiver voltage input range must be within 0.3 V to 1.425 V.
- ⁽²²⁾ For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rates above 700 Mbps and 0.45 V to 1.95 V for data rates below 700 Mbps.



Symbol/Description	Condition	Tran	sceiver Speed Gra	Unit	
Symbol/Description	Condition	Min	Тур	Max	Ont
	85- Ω setting	—	85	—	Ω
Differential on-chip termination	100- Ω setting	—	100	—	Ω
resistors	120-Ω setting	—	120	—	Ω
	150-Ω setting		150	_	Ω
Intra-differential pair skew	TX V_{CM} = 0.65 V (AC coupled) and slew rate of 15 ps			15	ps
Intra-transceiver block transmitter channel-to-channel skew	×6 PMA bonded mode			180	ps
Inter-transceiver block transmitter channel-to-channel skew ⁽⁵⁵⁾	× <i>N</i> PMA bonded mode			500	ps

Table 1-30: CMU PLL Specifications for Arria V GT and ST Devices

Symbol/Description	Transceiver S	peed Grade 3	Unit
Symbol Description	Min	Max	onit
Supported data range	0.611	10.3125	Gbps
fPLL supported data range	611	3125	Mbps

⁽⁵⁵⁾ This specification is only applicable to channels on one side of the device across two transceiver banks.



Table 1-31: Transceiver-FPGA Fabric Interface Specifications for Arria V GT and ST Devices

Symbol/Description	Transceiver S	peed Grade 3	Unit
Symbol Description	Min		ont
Interface speed (PMA direct mode)	50	153.6 ⁽⁵⁶⁾ , 161 ⁽⁵⁷⁾	MHz
Interface speed (single-width mode)	25	187.5	MHz
Interface speed (double-width mode)	25	163.84	MHz

Related Information

- CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain on page 1-35
- CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain on page 1-36



⁽⁵⁶⁾ The maximum frequency when core transceiver local routing is selected.

⁽⁵⁷⁾ The maximum frequency when core transceiver network routing (GCLK, RCLK, or PCLK) is selected.

Table 1-38: Memory Block Performance Specifications for Arria V Devices

Momory	Mada	Resourc	es Used		Unit		
Memory	Mode	ALUTs	Memory	-I3, -C4	-I5, -C5	-C6	Ont
	Single port, all supported widths	0	1	500	450	400	MHz
	Simple dual-port, all supported widths	0	1	500	450	400	MHz
MLAB	Simple dual-port with read and write at the same address	0	1	400	350	300	MHz
	ROM, all supported width	_		500	450	400	MHz
	Single-port, all supported widths	0	1	400	350	285	MHz
	Simple dual-port, all supported widths	0	1	400	350	285	MHz
M10K Block	Simple dual-port with the read-during- write option set to Old Data , all supported widths	0	1	315	275	240	MHz
	True dual port, all supported widths	0	1	400	350	285	MHz
	ROM, all supported widths	0	1	400	350	285	MHz

Internal Temperature Sensing Diode Specifications

Table 1-39: Internal Temperature Sensing Diode Specifications for Arria V Devices

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
-40 to 100°C	±8°C	No	1 MHz	< 100 ms	8 bits	8 bits

Periphery Performance

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.



Figure 1-10: SPI Slave Timing Diagram



Related Information

SPI Controller, Arria V Hard Processor System Technical Reference Manual

Provides more information about rx_sample_delay.

SD/MMC Timing Characteristics

Table 1-54: Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices

After power up or cold reset, the Boot ROM uses drvsel = 3 and smplsel = 0 to execute the code. At the same time, the SD/MMC controller enters the Identification Phase followed by the Data Phase. During this time, the value of interface output clock SDMMC_CLK_OUT changes from a maximum of 400 kHz (Identification Phase) up to a maximum of 12.5 MHz (Data Phase), depending on the internal reference clock SDMMC_CLK and the CSEL setting. The value of SDMMC_CLK is based on the external oscillator frequency and has a maximum value of 50 MHz.



After the Boot ROM code exits and control is passed to the preloader, software can adjust the value of drvsel and smplsel via the system manager. drvsel can be set from 1 to 7 and smplsel can be set from 0 to 7. While the preloader is executing, the values for SDMMC_CLK and SDMMC_CLK_OUT increase to a maximum of 200 MHz and 50 MHz respectively.

The SD/MMC interface calibration support will be available in a future release of the preloader through the SoC EDS software update.

Symbol	Description	Min	Мах	Unit
	SDMMC_CLK clock period (Identification mode)	20	_	ns
T _{sdmmc_clk} (internal reference clock)	SDMMC_CLK clock period (Default speed mode)	5	—	ns
	SDMMC_CLK clock period (High speed mode)	5	_	ns
	SDMMC_CLK_OUT clock period (Identification mode)	2500	—	ns
T _{sdmmc_clk_out} (interface output clock)	SDMMC_CLK_OUT clock period (Default speed mode)	40	_	ns
	SDMMC_CLK_OUT clock period (High speed mode)	20	—	ns
T _{dutycycle}	SDMMC_CLK_OUT duty cycle	45	55	%
T _d	SDMMC_CMD/SDMMC_D output delay	$\frac{(T_{sdmmc_clk} \times drvsel)/2}{-1.23}$	$\begin{array}{l}(\mathrm{T}_{sdmmc_clk}\times\texttt{drvsel})/2\\+1.69^{\ (87)}\end{array}$	ns
T _{su}	Input setup time	$1.05 - (T_{sdmmc_clk} \times smplsel)/2^{(88)}$	_	ns
T _h	Input hold time	$\frac{(T_{sdmmc_clk} \times smplsel)}{2^{(88)}}$	_	ns



⁽⁸⁷⁾ drvsel is the drive clock phase shift select value.

⁽⁸⁸⁾ smplsel is the sample clock phase shift select value.

Symbol	Description	Min	Max	Unit
$T_{dh}^{(89)}$	Data to write enable hold time	5	—	ns
T _{cea}	Chip enable to data access time		25	ns
T _{rea}	Read enable to data access time		16	ns
T _{rhz}	Read enable to data high impedance		100	ns
T _{rr}	Ready to read enable low	20	—	ns

Figure 1-17: NAND Command Latch Timing Diagram





FPP Configuration Timing when DCLK-to-DATA[] >1

Table 1-67: FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
t _{CF2CD}	nCONFIG low to CONF_DONE low	_	600	ns
t _{CF2ST0}	nconfig low to nstatus low	—	600	ns
t _{CFG}	nCONFIG low pulse width	2		μs
t _{STATUS}	nSTATUS low pulse width	268	1506 ⁽⁹⁸⁾	μs
t _{CF2ST1}	nCONFIG high to nSTATUS high	_	1506 ⁽⁹⁹⁾	μs
t _{CF2CK} ⁽¹⁰⁰⁾	nCONFIG high to first rising edge on DCLK	1506	_	μs
t _{ST2CK} ⁽¹⁰⁰⁾	nSTATUS high to first rising edge of DCLK	2		μs
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5	_	ns
t _{DH}	DATA[] hold time after rising edge on DCLK	$N - 1/f_{\rm DCLK}^{(101)}$		S
t _{CH}	DCLK high time	$0.45 imes 1/f_{MAX}$	_	S
t _{CL}	DCLK low time	$0.45 imes 1/f_{ m MAX}$		S
t _{CLK}	DCLK period	1/f _{MAX}	_	S
f _{MAX}	DCLK frequency (FPP ×8/ ×16)	_	125	MHz
t _R	Input rise time	_	40	ns
t _F	Input fall time		40	ns
t _{CD2UM}	CONF_DONE high to user mode ⁽¹⁰²⁾	175	437	μs

⁽⁹⁸⁾ This value can be obtained if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.



⁽⁹⁹⁾ This value can be obtained if you do not delay configuration by externally holding nSTATUS low.

 $^{^{(100)}}$ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

⁽¹⁰¹⁾ N is the DCLK-to-DATA[] ratio and f_{DCLK} is the DCLK frequency of the system.

⁽¹⁰²⁾ The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

1-94 Document Revision History

Term	Definition
V _{OX}	Output differential cross point voltage
W	High-speed I/O block—Clock boost factor

Document Revision History

Date	Version	Changes
December 2016	2016.12.09	 Updated V_{ICM} (AC coupled) specifications in Receiver Specifications for Arria V GX and SX Devices table. Added maximum specification for T_d in Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices table. Updated T_{init} specifications in the following tables: FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Arria V Devices FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices PS Timing Parameters for Arria V Devices
June 2016	2016.06.10	 Changed pin capacitance to maximum values. Updated SPI Master Timing Requirements for Arria V Devices table. Added T_{su} and T_h specifications. Removed T_{dinmax} specifications. Updated SPI Master Timing Diagram. Updated T_{clk} spec from maximum to minimum in I²C Timing Requirements for Arria V Devices table.





Date	Version	Changes
Date December 2015	Version 2015.12.16	 Updated Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices table. Updated F_{clk}, T_{dutycycle}, and T_{dssfrst} specifications. Added T_{qspi_clk}, T_{din_starb}, and T_{din_end} specifications. Removed T_{dinmax} specifications. Updated the minimum specification for T_{clk} to 16.67 ns and removed the maximum specification in SPI Master Timing Requirements for Arria V Devices table. Updated Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices table. Updated T_{clk} to T_{sdmmc_clk_out} symbol. Updated T_{sdmmc_clk_out} and T_d specifications. Added T_{sdmmc_clk}, T_{su}, and T_h specifications. Removed T_{dinmax} specifications. Updated the following diagrams: Quad SPI Flash Timing Diagram SD/MMC Timing Diagram
		 Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.



Related Information

- PowerPlay Early Power Estimator User Guide For more information about the EPE tool.
- **PowerPlay Power Analysis** ٠ For more information about PowerPlay power analysis.

Power Consumption

Altera offers two ways to estimate power consumption for a design-the Excel-based Early Power Estimator and the Quartus II PowerPlay Power Analyzer feature.

Note: You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

Related Information

- PowerPlay Early Power Estimator User Guide For more information about the EPE tool.
- PowerPlay Power Analysis For more information about PowerPlay power analysis.

I/O Pin Leakage Current

Table 2-8: I/O Pin Leakage Current for Arria V GZ Devices

If $V_O = V_{CCIO}$ to $V_{CCIOMax}$, 100 µA of leakage current per I/O is expected.

Symbol	Description	Conditions	Min	Тур	Max	Unit
II	Input pin	$V_{I} = 0 V$ to $V_{CCIOMAX}$	-30	—	30	μΑ
I _{OZ}	Tri-stated I/O pin	$V_{O} = 0 V$ to $V_{CCIOMAX}$	-30	_	30	μΑ



Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
Symbol/Description	Conditions	Min	Тур	Мах	Min	Тур	Мах	
Supported data rate range	VCO post-divider L = 2	8000		12500	8000	_	10312.5	Mbps
	L = 4	4000	_	6600	4000	_	6600	Mbps
	$L = 8^{(155)}$	2000	_	3300	2000	_	3300	Mbps
t _{pll_powerdown} ⁽¹⁵⁶⁾	_	1	—	_	1	_		μs
t _{pll_lock} ⁽¹⁵⁷⁾	_	_	_	10		_	10	μs

Related Information

- Arria V Device Overview For more information about device ordering codes.
- Transceiver Clocking in Arria V Devices For more information about clocking ATX PLLs.
- **Dynamic Reconfiguration in Arria V Devices** For more information about reconfiguring ATX PLLs.

Fractional PLL

Table 2-28: Fractional PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.



⁽¹⁵⁵⁾ This clock can be further divided by central or local clock dividers making it possible to use ATX PLL for data rates < 1 Gbps. For more information about ATX PLLs, refer to the Transceiver Clocking in Arria V Devices chapter and the Dynamic Reconfiguration in Arria V Devices chapter.

 $t_{pll_powerdown}$ is the PLL powerdown minimum pulse width.

⁽¹⁵⁷⁾ $t_{pll \ lock}$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

2-42 Memory Block Specifications

Mada	Performar	nce		Unit		
Mode	C3, I3L	C4	14	Onit		
One sum of two 27×27	380	300	MHz			
One sum of two 36×18	380	30	MHz			
One complex 18×18	400	35	MHz			
One 36 × 36	380	30	MHz			
Modes using Three DSP Blocks						
One complex 18×25	340	275 265		MHz		
Modes using Four DSP Blocks						
One complex 27×27	350	310		MHz		

Memory Block Specifications

Table 2-36: Memory Block Performance Specifications for Arria V GZ Devices

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.

Momony	Mode	Resources Used		Performance				Unit
Memory	moue	ALUTs	Memory	C3	C4	I3L	14	
	Single port, all supported widths	0	1	400	315	400	315	MHz
MLAB S R	Simple dual-port, x32/x64 depth	0	1	400	315	400	315	MHz
	Simple dual-port, x16 depth (178)	0	1	533	400	533	400	MHz
	ROM, all supported widths	0	1	500	450	500	450	MHz

⁽¹⁷⁸⁾ The F_{MAX} specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.



DLL Range Specifications

Table 2-47: DLL Range Specifications for Arria V GZ Devices

Arria V GZ devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Parameter	C3, I3L	C4, I4	Unit
DLL operating frequency range	300 - 890	300 - 890	MHz

DQS Logic Block Specifications

Table 2-48: DQS Phase Offset Delay Per Setting for Arria V GZ Devices

The typical value equals the average of the minimum and maximum values.

The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a -3 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is $[625 \text{ ps} + (10 \times 11 \text{ ps}) \pm 20 \text{ ps}] = 735 \text{ ps} \pm 20 \text{ ps}$.

Speed Grade	Min	Мах	Unit
C3, I3L	8	15	ps
C4, I4	8	16	ps

Table 2-49: DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria V GZ Devices

This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a -3 speed grade is ± 84 ps or ± 42 ps.

Number of DQS Delay Buffers	C3, I3L	C4, I4	Unit
1	30	32	ps
2	60	64	ps
3	90	96	ps

Table 2-55: DCLK-to-DATA[] Ratio for Arria V GZ Devices

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the data rate in bytes per second (Bps), or words per second (Wps). For example, in FPP ×16 when the DCLK-to-DATA[] ratio is 2, the DCLK frequency must be 2 times the data rate in Wps. Arria V GZ devices use the additional clock cycles to decrypt and decompress the configuration data.

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
FPP ×8	Disabled	Disabled	1
	Disabled	Enabled	1
	Enabled	Disabled	2
	Enabled	Enabled	2
FPP ×16	Disabled	Disabled	1
	Disabled	Enabled	2
	Enabled	Disabled	4
	Enabled	Enabled	4
FPP ×32	Disabled	Disabled	1
	Disabled	Enabled	4
	Enabled	Disabled	8
	Enabled	Enabled	8





Term	Definition
V _{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
V _{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
V _{SWING}	Differential input voltage
V _X	Input differential cross point voltage
V _{OX}	Output differential cross point voltage
W	High-speed I/O block—clock boost factor

Document Revision History

Date	Version	Changes
February 2017	2017.02.10	 Changed the minimum value for t_{CD2UMC} in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1" table. Changed the minimum value for t_{CD2UMC} in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK to DATA[] Ratio is 1" table.
		 Changed the minimum value for t_{CD2UMC} in the "AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices" table. Changed the minimum value for t_{CD2UMC} in the "PS Timing Parameters for Arria V GZ Devices" table. Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices" table.

