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Intel - 5AGXMB3G4F35C4N Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Details	
Product Status	Obsolete
Number of LABs/CLBs	17110
Number of Logic Elements/Cells	362000
Total RAM Bits	19822592
Number of I/O	544
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxmb3g4f35c4n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 1-21: Transceiver Clocks Specifications for Arria V GX and SX Devices

Sumbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
Symbol/Description	Condition	Min	Тур	Max	Min	Тур	Max	Onit
fixedclk clock frequency	PCIe Receiver Detect	_	125	_	_	125	_	MHz
Transceiver Reconfigura- tion Controller IP (mgmt_ clk_clk) clock frequency	_	75	_	125	75	_	125	MHz

Table 1-22: Receiver Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4		Transceiver Speed Grade 6			llnit	
Symbol/Description	Condition	Min	Тур	Мах	Min	Тур	Max	Onit
Supported I/O standards		1	.5 V PCML,	2.5 V PCML,	LVPECL, an	d LVDS		
Data rate ⁽²⁸⁾		611	—	6553.6	611	—	3125	Mbps
Absolute V_{MAX} for a receiver pin ⁽²⁹⁾	_		_	1.2		—	1.2	V
Absolute V _{MIN} for a receiver pin	_	-0.4	_		-0.4	—	—	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) before device configuration	_	_		1.6		_	1.6	V
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) after device configuration	_	_	_	2.2		_	2.2	V



 ⁽²⁸⁾ To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.
 ⁽²⁹⁾ The device cannot tolerate prolonged operation at this absolute maximum.

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
Symbol/Description	Condition	Min	Тур	Max	Min	Тур	Max	Onic
Minimum differential eye opening at the receiver serial input pins ⁽³⁰⁾	_	100	_	_	100	_	_	mV
V _{ICM} (AC coupled)	—	_	0.7/0.75/ 0.8 ⁽³¹⁾			0.7/0.75/ 0.8 ⁽³¹⁾	—	mV
V _{ICM} (DC coupled)	\leq 3.2Gbps ⁽³²⁾	670	700	730	670	700	730	mV
	85- Ω setting		85			85	—	Ω
Differential on-chip	100- Ω setting		100			100		Ω
termination resistors	120-Ω setting		120			120	—	Ω
	150-Ω setting		150			150	—	Ω
$t_{LTR}^{(33)}$	_			10		—	10	μs
$t_{LTD}^{(34)}$		4	_		4	_	—	μs
t _{LTD_manual} ⁽³⁵⁾		4			4	—	—	μs
$t_{LTR_LTD_manual}^{(36)}$		15			15	—	_	μs
Programmable ppm detector ⁽³⁷⁾	_		±62.5, 10	0, 125, 200, 2	50, 300, 500,	and 1000		ppm

⁽³⁰⁾ The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(31) The AC coupled $V_{ICM} = 700 \text{ mV}$ for Arria V GX and SX in PCIe mode only. The AC coupled $V_{ICM} = 750 \text{ mV}$ for Arria V GT and ST in PCIe mode only.

⁽³²⁾ For standard protocol compliance, use AC coupling.

 $^{(33)}$ t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

 $^{(34)}$ t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.

 $^{(35)}$ t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.

 $t_{\text{LTR_LTD_manual}}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.



Typical TX V_{OD} Setting for Arria V Transceiver Channels with termination of 100 Ω

Table 1-32: Typical TX Vor	Setting for Arria V Tran	sceiver Channels with	termination of 100 Ω

Symbol	V _{OD} Setting ⁽⁵⁸⁾	V _{OD} Value (mV)	V _{OD} Setting ⁽⁵⁸⁾	V _{OD} Value (mV)
	6 ⁽⁵⁹⁾	120	34	680
	7 ⁽⁵⁹⁾	140	35	700
	8(59)	160	36	720
	9	180	37	740
	10	200	38	760
	11	220	39	780
	12	240	40	800
	13	260	41	820
	14	280	42	840
V _{OD} differential peak-to-peak typical	15	300	43	860
7 I	16	320	44	880
	17	340	45	900
	18	360	46	920
	19	380	47	940
	20	400	48	960
	21	420	49	980
	22	440	50	1000
	23	460	51	1020
	24	480	52	1040

⁽⁵⁸⁾ Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

⁽⁵⁹⁾ Only valid for data rates \leq 5 Gbps.



1-40 Transceiver Compliance Specification

Quartus Prime 1st	Quartus Prime V _{OD} Setting							
Post Tap Pre- Emphasis Setting	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	Unit
16	_	_	9.56	7.73	6.49		_	dB
17	_		10.43	8.39	7.02		_	dB
18	_		11.23	9.03	7.52		_	dB
19	_		12.18	9.7	8.02		_	dB
20	_		13.17	10.34	8.59		_	dB
21	_		14.2	11.1			_	dB
22	_		15.38	11.87			_	dB
23	_		_	12.67	_	_	_	dB
24	_		_	13.48			_	dB
25	_		_	14.37			_	dB
26	_						_	dB
27	_						_	dB
28	_	_	_	_	_	_	_	dB
29	_		_				_	dB
30	_						_	dB
31	_		_				_	dB

Related Information

SPICE Models for Altera Devices

Provides the Arria V HSSI HSPICE models.

Transceiver Compliance Specification

The following table lists the physical medium attachment (PMA) specification compliance of all supported protocol for Arria V GX, GT, SX, and ST devices. For more information about the protocol parameter details and compliance specifications, contact your Altera Sales Representative.



Figure 1-7: Timing Diagram for oe and dyn_term_ctrl Signals



Duty Cycle Distortion (DCD) Specifications

Table 1-47: Worst-Case DCD on Arria V I/O Pins

The output DCD cycle only applies to the I/O buffer. It does not cover the system DCD.

Symbol	-I3,	-C4	-C5	-I5 -C6			Unit	
Symbol	Min	Max	Min	Max	Min	Max	Unit	
Output Duty Cycle	45	55	45	55	45	55	%	

HPS Specifications

This section provides HPS specifications and timing for Arria V devices.

For HPS reset, the minimum reset pulse widths for the HPS cold and warm reset signals (HPS_nRST and HPS_nPOR) are six clock cycles of HPS_CLK1.



Figure 1-16: I²C Timing Diagram



NAND Timing Characteristics

Table 1-60: NAND ONFI 1.0 Timing Requirements for Arria V Devices

The NAND controller supports Open NAND FLASH Interface (ONFI) 1.0 Mode 5 timing as well as legacy NAND devices. This table lists the requirements for ONFI 1.0 mode 5 timing. The HPS NAND controller can meet this timing by programming the c4 output of the main HPS PLL and timing registers provided in the NAND controller.

Symbol	Description	Min	Max	Unit
T _{wp} ⁽⁸⁹⁾	Write enable pulse width	10	—	ns
T _{wh} ⁽⁸⁹⁾	Write enable hold time	7		ns
T _{rp} ⁽⁸⁹⁾	Read enable pulse width	10		ns
T _{reh} ⁽⁸⁹⁾	Read enable hold time	7		ns
T _{clesu} ⁽⁸⁹⁾	Command latch enable to write enable setup time	10		ns
T _{cleh} ⁽⁸⁹⁾	Command latch enable to write enable hold time	5		ns
T _{cesu} ⁽⁸⁹⁾	Chip enable to write enable setup time	15		ns
T _{ceh} ⁽⁸⁹⁾	Chip enable to write enable hold time	5		ns
T _{alesu} ⁽⁸⁹⁾	Address latch enable to write enable setup time	10		ns
T _{aleh} ⁽⁸⁹⁾	Address latch enable to write enable hold time	5		ns
T _{dsu} ⁽⁸⁹⁾	Data to write enable setup time	10		ns

⁽⁸⁹⁾ Timing of the NAND interface is controlled through the NAND configuration registers.



1-76 FPGA JTAG Configuration Timing

POR Delay	Minimum	Maximum	Unit
Standard	100	300	ms

Related Information

MSEL Pin Settings

Provides more information about POR delay based on MSEL pin settings for each configuration scheme.

FPGA JTAG Configuration Timing

Table 1-64: FPGA JTAG Timing Parameters and Values for Arria V Devices

Symbol	Description	Min	Max	Unit
t _{JCP}	TCK clock period	30, 167 ⁽⁹²⁾		ns
t _{JCH}	TCK clock high time	14		ns
t _{JCL}	TCK clock low time	14		ns
t _{JPSU (TDI)}	TDI JTAG port setup time	2		ns
t _{JPSU (TMS)}	TMS JTAG port setup time	3		ns
t _{JPH}	JTAG port hold time	5		ns
t _{JPCO}	JTAG port clock to output		12 ⁽⁹³⁾	ns
t _{JPZX}	JTAG port high impedance to valid output		14 ⁽⁹³⁾	ns
t _{JPXZ}	JTAG port valid output to high impedance		14 ⁽⁹³⁾	ns



⁽⁹²⁾ The minimum TCK clock period is 167 ns if V_{CCBAT} is within the range 1.2 V – 1.5 V when you perform the volatile key programming.

⁽⁹³⁾ A 1-ns adder is required for each VCCIO voltage step down from 3.0 V. For example, tJPCO= 13 ns if VCCIO of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

Initialization

Table 1-71: Initialization Clock Source Option and the Maximum Frequency for Arria V Devices

Initialization Clock Source	Configuration Scheme	Maximum Frequency (MHz)	Minimum Number of Clock Cycles
Internal Oscillator	AS, PS, and FPP	12.5	
(107)	PS and FPP	125	Т
CLKOSK	AS	100	- ¹ init
DCLK	PS and FPP	125	

Configuration Files

Table 1-72: Uncompressed .rbf Sizes for Arria V Devices

Use this table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (.hex) or tabular text file (.ttf) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Quartus Prime software. However, for a specific version of the Quartus Prime software, any design targeted for the same device has the same uncompressed configuration file size.

The IOCSR raw binary file (.rbf) size is specifically for the Configuration via Protocol (CvP) feature.

Arria V GX, GT, SX, and ST Device Datasheet



⁽¹⁰⁷⁾ To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus Prime software from the **General** panel of the **Device and Pin Options** dialog box.

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)
	A1	71,015,712	439,960
	A3	71,015,712	439,960
	A5	101,740,800	446,360
Arria V CY	A7	101,740,800	446,360
	B1	137,785,088	457,368
	B3	137,785,088	457,368
	B5	185,915,808	463,128
	B7	185,915,808	463,128
	C3	71,015,712	439,960
Arria V CT	C7	101,740,800	446,360
Allia v GI	D3	137,785,088	457,368
	D7	185,915,808	463,128
Arria V SV	B3	185,903,680	450,968
Arria V SX	B5	185,903,680	450,968
Arria V ST	D3	185,903,680	450,968
Arria V SI	D5	185,903,680	450,968

Minimum Configuration Time Estimation

Table 1-73: Minimum Configuration Time Estimation for Arria V Devices

The estimated values are based on the configuration .rbf sizes in Uncompressed .rbf Sizes for Arria V Devices table.





This document covers the electrical and switching characteristics for Arria V GZ devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, core, and periphery performance. This document also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

Related Information

Arria V Device Overview

For information regarding the densities and packages of devices in the Arria V GZ family.

Electrical Characteristics

Operating Conditions

When you use Arria V GZ devices, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Arria V GZ devices, you must consider the operating requirements described in this datasheet.

Arria V GZ devices are offered in commercial and industrial temperature grades.

Commercial devices are offered in -3 (fastest) and -4 core speed grades. Industrial devices are offered in -3L and -4 core speed grades. Arria V GZ devices are offered in -2 and -3 transceiver speed grades.

Table 2-1: Commercial and Industrial Speed Grade Offering for Arria V GZ Devices

C = Commercial temperature grade; I = Industrial temperature grade.

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Symbol	Description	Condition	Minimum ⁽¹¹⁴⁾	Typical	Maximum ⁽¹¹⁴⁾	Unit
V _{CCPT}	Power supply for programmable power technology	—	1.45	1.50	1.55	V
V _{CC_AUX}	Auxiliary supply for the programmable power technology	_	2.375	2.5	2.625	V
V _{CCPD} (116	I/O pre-driver (3.0 V) power supply	_	2.85	3.0	3.15	V
)	I/O pre-driver (2.5 V) power supply	_	2.375	2.5	2.625	V
	I/O buffers (3.0 V) power supply	_	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	_	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	_	1.71	1.8	1.89	V
V _{CCIO}	I/O buffers (1.5 V) power supply	_	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply	_	1.283	1.35	1.45	V
	I/O buffers (1.25 V) power supply	_	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply		1.14	1.2	1.26	V
	Configuration pins (3.0 V) power supply	_	2.85	3.0	3.15	V
V _{CCPGM}	Configuration pins (2.5 V) power supply	_	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply		1.71	1.8	1.89	V
V _{CCA} _	PLL analog voltage regulator power supply		2.375	2.5	2.625	V
V _{CCD} FPLL	PLL digital voltage regulator power supply	_	1.45	1.5	1.55	V
V _{CCBAT} (117	Battery back-up power supply (For design security volatile key register)		1.2		3.0	V

⁽¹¹⁴⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements.
Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.



⁽¹¹⁶⁾ V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V.

⁽¹¹⁷⁾ If you do not use the design security feature in Arria V GZ devices, connect V_{CCBAT} to a 1.2- to 3.0-V power supply. Arria V GZ power-on-reset (POR) circuitry monitors V_{CCBAT}. Arria V GZ devices do not exit POR if V_{CCBAT} is not powered up.

Transceiver Power Supply Requirements

Table 2-7: Transceiver Power Supply Voltage Requirements for Arria V GZ Devices

Conditions	VCCR_GXB and VCCT_GXB ⁽¹²²⁾	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true:	1.05			
• Data rate > 10.3 Gbps.				
• DFE is used.				
If ANY of the following conditions are true ⁽¹²³⁾ :	1.0	3.0		
• ATX PLL is used.				
• Data rate > 6.5 Gbps.			1.5	V
• DFE (data rate ≤ 10.5 Gbps), AEQ, or EyeQ feature is used.				
If ALL of the following conditions are true:	0.85	2.5		
• ATX PLL is not used.				
• Data rate ≤ 6.5 Gbps.				
• DFE, AEQ, and EyeQ are not used.				

DC Characteristics

Supply Current

Standby current is the current drawn from the respective power rails used for power budgeting.

Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.



Send Feedback

⁽¹²²⁾ If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to 0.85 V, they can be shared with the VCC core supply.

⁽¹²³⁾ Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

Bus Hold Specifications

Table 2-9: Bus Hold Parameters for Arria V GZ Devices

			V _{ccio}										
Parameter	Symbol	Conditions	1.2	2 V	1.5	5 V	1.8	3 V	2.5	5 V	3.0	V	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I _{SUSL}	V _{IN} > V _{IL} (maximum)	22.5	_	25.0	_	30.0		50.0	_	70.0	_	μΑ
High sustaining current	I _{SUSH}	V _{IN} < V _{IH} (minimum)	-22.5	_	-25.0	_	-30.0	_	-50.0	_	-70.0	_	μΑ
Low overdrive current	I _{ODL}	$0V < V_{IN} < V_{CCIO}$	_	120	_	160	_	200	_	300	_	500	μΑ
High overdrive current	I _{ODH}	$0V < V_{IN} < V_{CCIO}$	—	-120	_	-160	_	-200		-300	_	-500	μΑ
Bus-hold trip point	V _{TRIP}		0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block.

Table 2-10: OCT Calibration Accuracy Specifications for Arria V GZ Devices

OCT calibration accuracy is valid at the time of calibration only.





Sumbol	Description	Conditions	Calibration Ac	Unit	
Symbol	Description	Conditions	C3, I3L	C4, I4	Onit
25-Ω R _S	Internal series termination with calibration (25- Ω setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%
50-Ω R _S	Internal series termination with calibration (50- Ω setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%
34- Ω and 40- Ω R_S	Internal series termination with calibration (34- Ω and 40- Ω setting)	V _{CCIO} = 1.5, 1.35, 1.25, 1.2 V	±15	±15	%
48-Ω, 60-Ω, 80-Ω, and 240-Ω R _S	Internal series termination with calibration (48- Ω , 60- Ω , 80- Ω , and 240- Ω setting)	$V_{CCIO} = 1.2 V$	±15	±15	%
50- Ω R _T	Internal parallel termination with calibration (50- Ω setting)	V _{CCIO} = 2.5, 1.8, 1.5, 1.2 V	-10 to +40	-10 to +40	%
20- Ω , 30- Ω , 40- Ω , 60- Ω , and 120- Ω R _T	Internal parallel termination with calibration ($20-\Omega$, $30-\Omega$, $40-\Omega$, $60-\Omega$, and $120-\Omega$ setting)	V _{CCIO} = 1.5, 1.35, 1.25 V	-10 to +40	-10 to +40	%
60- Ω and 120- Ω R _T	Internal parallel termination with calibration (60- Ω and 120- Ω setting)	$V_{CCIO} = 1.2$	-10 to +40	-10 to +40	%
25- $\Omega R_{S_left_shift}$	Internal left shift series termination with calibration (25- Ω R _{S_left_shift} setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%

Table 2-11: OCT Without Calibration Resistance Tolerance Specifications for Arria V GZ Devices

Symbol	Description	Conditions	Resistance	Unit	
Symbol	Description	Conditions	C3, I3L	C4, I4	Onic
25-Ω R, 50-Ω R _S	Internal series termination without calibration (25- Ω setting)	V _{CCIO} = 3.0 and 2.5 V	±40	±40	%



Switching Characteristics

Transceiver Performance Specifications

Reference Clock

Table 2-22: Reference Clock Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
Symbol/Description		Min	Тур	Мах	Min	Тур	Мах	Onit
Reference Clock								
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCM and HCSL	L, 1.4-V PC	ML, 1.5-V P	CML, 2.5-V	PCML, Di	fferential LV	PECL, LVDS,
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS						
Input Reference Clock Frequency (CMU PLL) ⁽¹³⁷⁾	_	40		710	40		710	MHz
Input Reference Clock Frequency (ATX PLL) ⁽¹³⁷⁾	-	100		710	100		710	MHz

⁽¹³⁷⁾ The input reference clock frequency options depend on the data rate and the device speed grade.



Sumbol	Conditions	C3, I3L			C4, I4			Unit
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Onic
True Differential I/O Standards - f _{HSDR} (data rate)	SERDES factor J = 3 to 10 (182), (183)	(184)	_	1250	(184)	_	1050	Mbps
	SERDES factor $J \ge 4$ LVDS TX with DPA (185), (186), (187), (188)	(184)		1600	(184)	_	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(184)	—	(189)	(184)	_	(189)	Mbps
	SERDES factor J = 1, uses SDR Register	(184)	—	(189)	(184)		(189)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f _{HSDR} (data rate) (190)	SERDES factor J = 4 to 10 ⁽¹⁹¹⁾	(184)		840	(184)		840	Mbps

⁽¹⁸²⁾ If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

- ⁽¹⁸⁵⁾ Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.
- Requires package skew compensation with PCB trace length. (186)
- (187)Do not mix single-ended I/O buffer within LVDS I/O bank.
- Chip-to-chip communication only with a maximum load of 5 pF. (188)
- ⁽¹⁸⁹⁾ The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.
- ⁽¹⁹⁰⁾ You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.
- ⁽¹⁹¹⁾ When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.



⁽¹⁸³⁾ The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

⁽¹⁸⁴⁾ The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

Active Serial Configuration Timing

Figure 2-9: AS Configuration Timing



Timing waveform for the active serial (AS) x1 mode and AS x4 mode configuration timing.

Notes:

1. If you are using AS ×4 mode, this signal represents the AS_DATA[3..0] and ERCQ sends in 4-bits of data for each DCLKcycle.

2. The initialization clock can be from internal oscillator or CLKUSR pin

3. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE ges low.

Table 2-58: AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices

The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in the "PS Timing Parameters for Arria V GZ Devices" table.



Symbol	Parameter	Minimum	Maximum	Unit
t _{CO}	DCLK falling edge to AS_DATA0/ASDO output	-	4	ns
t _{SU}	Data setup time before falling edge on DCLK	1.5		ns
t _H	Data hold time after falling edge on DCLK	0	—	ns
t _{CD2UM}	CONF_DONE high to user mode ⁽²¹⁶⁾	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK}$ period	_	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (8576 × clkusr period)	_	_

Table 2-59: DCLK Frequency Specification in the AS Configuration Scheme

This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

The AS multi-device configuration scheme does not support ${\tt DCLK}$ frequency of 100 MHz.

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

Related Information

- Passive Serial Configuration Timing on page 2-67
- Configuration, Design Security, and Remote System Upgrades in Arria V Devices





⁽²¹⁶⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Table 2-60: PS Timing Parameters for Arria V GZ Devices

Symbol	Parameter	Minimum	Maximum	Unit
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	_	600	ns
t _{CFG}	nCONFIG low pulse width	2		μs
t _{STATUS}	nSTATUS low pulse width	268	1,506 (217)	μs
t _{CF2ST1}	nCONFIG high to nSTATUS high		1,506 (218)	μs
t _{CF2CK} (219)	nCONFIG high to first rising edge on DCLK	1,506	—	μs
t _{ST2CK} (219)	nSTATUS high to first rising edge of DCLK	2		μs
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5		ns
t _{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t _{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$		S
t _{CL}	DCLK low time	$0.45 imes 1/f_{ m MAX}$	—	s
t _{CLK}	DCLK period	1/f _{MAX}		S
f _{MAX}	DCLK frequency	_	125	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽²²⁰⁾	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK}$ period	_	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (8576 × CLKUSR period) (221)	—	

⁽²¹⁷⁾ This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.



⁽²¹⁸⁾ This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

⁽²¹⁹⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

⁽²²⁰⁾ The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

Related Information

Configuration, Design Security, and Remote System Upgrades in Arria V Devices

Initialization

Table 2-61: Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices

Initialization Clock Source	Configuration Schemes	Maximum Frequency (MHz)	Minimum Number of Clock Cycles
Internal Oscillator	AS, PS, FPP	12.5	
(222)	PS, FPP	125	9576
CLKUSR	AS	100	8370
DCLK	PS, FPP	125	

Configuration Files

Use the following table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (.hex) or tabular text file (.ttf) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size.

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⁽²²¹⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.

⁽²²²⁾ To enable CLKUSR as the initialization clock source, turn on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software from the General panel of the Device and Pin Options dialog box.