E·XFL

Intel - 5AGXMB3G4F35C5N Datasheet



Welcome to <u>E-XFL.COM</u>

Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Details	
Product Status	Obsolete
Number of LABs/CLBs	17110
Number of Logic Elements/Cells	362000
Total RAM Bits	19822592
Number of I/O	544
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxmb3g4f35c5n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Transceiver Power Supply Operating Conditions

Table '	1-4:	Transceiver	Power S	upply	Operating	Conditions	for Arria V Devices	j
---------	------	-------------	---------	-------	-----------	------------	---------------------	---

Symbol	Description	Minimum ⁽⁵⁾	Typical	Maximum ⁽⁵⁾	Unit
V _{CCA_GXBL}	Transceiver high voltage power (left side)	2 275	2 500	2 625	V
V _{CCA_GXBR}	Transceiver high voltage power (right side)	2.575	2.300	2.025	v
V _{CCR_GXBL}	GX and SX speed grades—receiver power (left side)	1.08/1.12	1 1/1 15(6)	1 14/1 18	V
V _{CCR_GXBR}	GX and SX speed grades—receiver power (right side)	1.00/1.12	1.1/1.13	1.14/1.10	v
V _{CCR_GXBL}	GT and ST speed grades—receiver power (left side)	1 17	1 20	1 23	V
V _{CCR_GXBR}	GT and ST speed grades—receiver power (right side)	1.17 1.20		1.23	v
V _{CCT_GXBL}	GX and SX speed grades—transmitter power (left side)	1.08/1.12	1 1/1 15(6)	1 14/1 18	V
V _{CCT_GXBR}	GX and SX speed grades—transmitter power (right side)	1.00/1.12	1.1/1.15	1.14/1.10	v
V _{CCT_GXBL}	GT and ST speed grades—transmitter power (left side)	1 17	1 20	1 23	V
V _{CCT_GXBR}	GT and ST speed grades—transmitter power (right side)	1.17	1.20	1.23	v
V _{CCH_GXBL}	Transmitter output buffer power (left side)	1 /25	1 500	1 575	V
V _{CCH_GXBR}	Transmitter output buffer power (right side)	1.423	1.300	1.375	v

⁽⁵⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁶⁾ For data rate <=3.2 Gbps, connect V_{CCR_GXBL/R}, V_{CCT_GXBL/R}, or V_{CCL_GXBL/R} to either 1.1-V or 1.15-V power supply. For data rate >3.2 Gbps, connect V_{CCR_GXBL/R}, V_{CCT_GXBL/R}, or V_{CCL_GXBL/R} to a 1.15-V power supply. For details, refer to the Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines.



Figure 1-1: Equation for OCT Variation Without Recalibration

$$R_{OCT} = R_{SCAL} \left(1 + \left(\frac{dR}{dT} \times \Delta T \right) \pm \left(\frac{dR}{dV} \times \Delta V \right) \right)$$

The definitions for the equation are as follows:

- The R_{OCT} value calculated shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
- R_{SCAL} is the OCT resistance value at power-up.
- ΔT is the variation of temperature with respect to the temperature at power up.
- ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
- dR/dT is the percentage change of R_{SCAL} with temperature.
- dR/dV is the percentage change of R_{SCAL} with voltage.

OCT Variation after Power-Up Calibration

Table 1-10: OCT Variation after Power-Up Calibration for Arria V Devices

This table lists OCT variation with temperature and voltage after power-up calibration. The OCT variation is valid for a V_{CCIO} range of $\pm 5\%$ and a temperature range of 0°C to 85°C.

Symbol	Description	V _{CCIO} (V)	Value	Unit
		3.0	0.100	
		2.5	0.100	
	OCT variation with voltage without recalibration	1.8	0.100	
dR/dV		1.5	0.100	%/mV
		1.35	0.150	
		1.25	0.150	
		1.2	0.150	



1/O Standard	V _{IL(DC)} (V)		V _{IH(DC)} (V)		V _{IL(AC)} (V)	V _{IH(AC)} (V)	V _{OL} (V)	V _{OH} (V)	I _{OL} ⁽¹⁴⁾	I_{a} (mA)
	Min	Max	Min	Мах	Max	Min	Мах	Min	(mA)	
HSTL-15 Class II	—	V _{REF} – 0.1	$V_{REF} + 0.1$	_	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	V _{CCIO} – 0.4	16	-16
HSTL-12 Class I	-0.15	V _{REF} – 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	V _{REF} – 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	16	-16
HSUL-12	_	V _{REF} – 0.13	$V_{REF} + 0.13$	_	V _{REF} - 0.22	V _{REF} + 0.22	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	_	_

Differential SSTL I/O Standards

Table 1-17: Differential SSTL I/O Standards for Arria V Devices

I/O Standard	$V_{CCIO}(V) \qquad V_{SWING(DC)}(V) \qquad V_{X(AC)}$		$V_{X(AC)}(V)$	V _{X(AC)} (V)		V _{SWING(AC)} (V)				
	Min	Тур	Max	Min	Мах	Min	Тур	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V _{CCIO} + 0.6	V _{CCIO} /2 – 0.2	—	V _{CCIO} /2 + 0.2	0.62	$V_{CCIO} + 0.6$
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V _{CCIO} + 0.6	V _{CCIO} /2 – 0.175	—	V _{CCIO} /2 + 0.175	0.5	$V_{CCIO} + 0.6$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(15)	V _{CCIO} /2 – 0.15	—	V _{CCIO} /2 + 0.15	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$
SSTL-135	1.283	1.35	1.45	0.18	(15)	V _{CCIO} /2 – 0.15	V _{CCIO} /2	V _{CCIO} /2 + 0.15	2(V _{IH(AC)} – V _{REF})	$2(V_{IL(AC)} - V_{REF})$

⁽¹⁴⁾ To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.



 $^{^{(15)}}$ The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Symbol/Description	Condition	Tran	de 3	Unit	
Symbol/Description	Condition	Min	Тур	Max	Ont
	85- Ω setting	—	85	—	Ω
Differential on-chip termination	100- Ω setting	—	100	—	Ω
resistors	120-Ω setting	—	120	—	Ω
	150-Ω setting		150	_	Ω
Intra-differential pair skew	TX V_{CM} = 0.65 V (AC coupled) and slew rate of 15 ps			15	ps
Intra-transceiver block transmitter channel-to-channel skew	×6 PMA bonded mode			180	ps
Inter-transceiver block transmitter channel-to-channel skew ⁽⁵⁵⁾	× <i>N</i> PMA bonded mode			500	ps

Table 1-30: CMU PLL Specifications for Arria V GT and ST Devices

Symbol/Description	Transceiver S	peed Grade 3	Unit
Symbol Description	Min	Max	onit
Supported data range	0.611	10.3125	Gbps
fPLL supported data range	611	3125	Mbps

⁽⁵⁵⁾ This specification is only applicable to channels on one side of the device across two transceiver banks.



Figure 1-12: USB Timing Diagram



Ethernet Media Access Controller (EMAC) Timing Characteristics

Table 1-56: Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements for Arria V Devices

Symbol	Description	Min	Тур	Мах	Unit
T _{clk} (1000Base-T)	TX_CLK clock period	_	8		ns
T _{clk} (100Base-T)	TX_CLK clock period	_	40		ns
T _{clk} (10Base-T)	TX_CLK clock period		400		ns
T _{dutycycle}	TX_CLK duty cycle	45	—	55	%
T _d	TX_CLK to TXD/TX_CTL output data delay	-0.85	—	0.15	ns

Figure 1-13: RGMII TX Timing Diagram





1-76 FPGA JTAG Configuration Timing

POR Delay	Minimum	Maximum	Unit
Standard	100	300	ms

Related Information

MSEL Pin Settings

Provides more information about POR delay based on MSEL pin settings for each configuration scheme.

FPGA JTAG Configuration Timing

Table 1-64: FPGA JTAG Timing Parameters and Values for Arria V Devices

Symbol	Description	Min	Max	Unit
t _{JCP}	TCK clock period	30, 167 ⁽⁹²⁾		ns
t _{JCH}	TCK clock high time	14		ns
t _{JCL}	TCK clock low time	14		ns
t _{JPSU (TDI)}	TDI JTAG port setup time	2		ns
t _{JPSU (TMS)}	TMS JTAG port setup time	3		ns
t _{JPH}	JTAG port hold time	5		ns
t _{JPCO}	JTAG port clock to output		12 ⁽⁹³⁾	ns
t _{JPZX}	JTAG port high impedance to valid output		14 ⁽⁹³⁾	ns
t _{JPXZ}	JTAG port valid output to high impedance		14 ⁽⁹³⁾	ns



⁽⁹²⁾ The minimum TCK clock period is 167 ns if V_{CCBAT} is within the range 1.2 V – 1.5 V when you perform the volatile key programming.

⁽⁹³⁾ A 1-ns adder is required for each VCCIO voltage step down from 3.0 V. For example, tJPCO= 13 ns if VCCIO of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

FPP Configuration Timing

DCLK-to-DATA[] Ratio (r) for FPP Configuration

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP $\times 16$ where the *r* is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

Table 1-65: DCLK-to-DATA[] Ratio for Arria V Devices

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
	Off	Off	1
EDD (9 bit wide)	On	Off	1
frr (o-bit wide)	Off	On	2
	On	On	2
	Off	Off	1
EDD (16 bit wide)	On	Off	2
FFF (10-bit wide)	Off	On	4
	On	On	4

FPP Configuration Timing when DCLK-to-DATA[] = 1

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8 and FPP ×16. For the respective DCLKto-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Arria V Devices table.

Table 1-66: FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Arria V Devices

Symbol	Parameter	Minimum	Maximum	Unit
t _{CF2CD}	nCONFIG low to CONF_DONE low	_	600	ns
t _{CF2ST0}	nconfig low to nstatus low	_	600	ns
t _{CFG}	nCONFIG low pulse width	2		μs

Arria V GX, GT, SX, and ST Device Datasheet

Altera Corporation



		Active Serial ⁽¹⁰⁸⁾			Fast Passive Parallel ⁽¹⁰⁹⁾			
Variant	Member Code	Width	DCLK (MHz)	Minimum Configura- tion Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)	
	A1	4	100	178	16	125	36	
	A3	4	100	178	16	125	36	
	A5	4	100	255	16	125	51	
Arria V CV	A7	4	100	255	16	125	51	
Allia V GA	B1	4	100	344	16	125	69	
	В3	4	100	344	16	125	69	
	B5	4	100	465	16	125	93	
	B7	4	100	465	16	125	93	
	C3	4	100	178	16	125	36	
Amia V CT	C7	4	100	255	16	125	51	
Allia v GI	D3	4	100	344	16	125	69	
	D7	4	100	465	16	125	93	
Arria V SV	В3	4	100	465	16	125	93	
AIIIa V SA	B5	4	100	465	16	125	93	
Arria V ST	D3	4	100	465	16	125	93	
Arria V SI	D5	4	100	465	16	125	93	

Related Information Configuration Files on page 1-83

(108) DCLK frequency of 100 MHz using external CLKUSR.
 (109) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.





1-94 Document Revision History

Term	Definition
V _{OX}	Output differential cross point voltage
W	High-speed I/O block—Clock boost factor

Document Revision History

Date	Version	Changes
December 2016	2016.12.09	 Updated V_{ICM} (AC coupled) specifications in Receiver Specifications for Arria V GX and SX Devices table. Added maximum specification for T_d in Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices table. Updated T_{init} specifications in the following tables: FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Arria V Devices FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices PS Timing Parameters for Arria V Devices
June 2016	2016.06.10	 Changed pin capacitance to maximum values. Updated SPI Master Timing Requirements for Arria V Devices table. Added T_{su} and T_h specifications. Removed T_{dinmax} specifications. Updated SPI Master Timing Diagram. Updated T_{clk} spec from maximum to minimum in I²C Timing Requirements for Arria V Devices table.





1-98 Document Revision History

Date	Version	Changes
July 2014	3.8	 Added a note in Table 3, Table 4, and Table 5: The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements. Updated V_{CC_HPS} specification in Table 5. Added a note in Table 19: Differential inputs are powered by V_{CCPD} which requires 2.5 V. Updated "Minimum differential eye opening at the receiver serial input pins" specification in Table 20 and Table 21. Updated description in "HPS PLL Specifications" section. Updated VCO range maximum specification in Table 39. Updated T_d and T_h specifications in Table 45. Added T_h specification in Table 47 and Figure 13. Updated a note in Figure 20, Figure 21, and Figure 23 as follows: Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required. Removed "Remote update only in AS mode" specification in Table 58. Added DCLK device initialization clock source specification in Table 60. Added description in "Configuration Files" section: The IOCSR .rbf size is specifically for the Configuration via Protocol (CvP) feature. Removed f_{MAX_RU_CLK} specification in Table 63.
February 2014	3.7	 Updated V_{CCRSTCLK_HPS} maximum specification in Table 1. Added V_{CC_AUX_SHARED} specification in Table 1.
December 2013	3.6	 Added "HPS PLL Specifications". Added Table 24, Table 39, and Table 40. Updated Table 1, Table 3, Table 5, Table 19, Table 20, Table 21, Table 38, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, Table 51, Table 55, Table 56, and Table 59. Updated Figure 7, Figure 13, Figure 15, Figure 16, and Figure 19. Removed table: GPIO Pulse Width for Arria V Devices.



Date	Version	Changes
August 2013	3.5	Removed "Pending silicon characterization" note in Table 29.Updated Table 25.
August 2013	3.4	 Removed Preliminary tags for Table 1, Table 2, Table 3, Table 4, Table 5, Table 6, Table 7, Table 9, Table 12, Table 13, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, Table 21, Table 22, Table 23, Table 24, Table 25, Table 26, Table 27, Table 28, Table 29, Table 30, Table 31, Table 35, Table 36, Table 51, Table 53, Table 54, Table 55, Table 56, Table 57, Table 60, Table 62, and Table 64. Updated Table 1, Table 3, Table 11, Table 19, Table 20, Table 21, Table 22, Table 29.
June 2013	3.3	Updated Table 20, Table 21, Table 25, and Table 38.
May 2013	3.2	 Added Table 37. Updated Figure 8, Figure 9, Figure 20, Figure 22, and Figure 23. Updated Table 1, Table 5, Table 10, Table 13, Table 19, Table 20, Table 21, Table 23, Table 29, Table 39, Table 40, Table 46, Table 56, Table 57, Table 60, and Table 64. Updated industrial junction temperature range for -I3 speed grade in "PLL Specifications" section.
March 2013	3.1	 Added HPS reset information in the "HPS Specifications" section. Added Table 60. Updated Table 1, Table 3, Table 17, Table 20, Table 29, and Table 59. Updated Figure 21.



1-100 Document Revision History

Date	Version	Changes
November 2012	3.0	 Updated Table 2, Table 4, Table 9, Table 14, Table 16, Table 17, Table 20, Table 21, Table 25, Table 29, Table 36, Table 56, Table 57, and Table 60. Removed table: Transceiver Block Jitter Specifications for Arria V Devices. Added HPS information: Added "HPS Specifications" section. Added Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, and Table 50. Added Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19. Updated Table 3 and Table 5.
October 2012	2.4	 Updated Arria V GX V_{CCR_GXBL/R}, V_{CCT_GXBL/R}, and V_{CCL_GXBL/R} minimum and maximum values, and data rate in Table 4. Added receiver V_{ICM} (AC coupled) and V_{ICM} (DC coupled) values, and transmitter V_{OCM} (AC coupled) and V_{OCM} (DC coupled) values in Table 20 and Table 21.
August 2012	2.3	Updated the SERDES factor condition in Table 30.
July 2012	2.2	 Updated the maximum voltage for V_I (DC input voltage) in Table 1. Updated Table 20 to include the Arria V GX -I3 speed grade. Updated the minimum value of the fixedclk clock frequency in Table 20 and Table 21. Updated the SERDES factor condition in Table 30. Updated Table 50 to include the IOE programmable delay settings for the Arria V GX -I3 speed grade.
June 2012	2.1	Updated V _{CCR_GXBL/R} , V _{CCT_GXBL/R} , and V _{CCL_GXBL/R} values in Table 4.



Sumbol	Description	Conditions	Calibration Ac	Unit		
Symbol	Description	Conditions	C3, I3L	C4, I4		
25-Ω R _S	Internal series termination with calibration (25- Ω setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%	
50-Ω R _S	Internal series termination with calibration (50- Ω setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%	
34- Ω and 40- Ω R_S	Internal series termination with calibration (34- Ω and 40- Ω setting)	V _{CCIO} = 1.5, 1.35, 1.25, 1.2 V	±15	±15	%	
48-Ω, 60-Ω, 80-Ω, and 240-Ω R _S	Internal series termination with calibration (48- Ω , 60- Ω , 80- Ω , and 240- Ω setting)	$V_{CCIO} = 1.2 V$	±15	±15	%	
50- Ω R _T	Internal parallel termination with calibration (50- Ω setting)	V _{CCIO} = 2.5, 1.8, 1.5, 1.2 V	-10 to +40	-10 to +40	%	
20- Ω , 30- Ω , 40- Ω , 60- Ω , and 120- Ω R _T	Internal parallel termination with calibration ($20-\Omega$, $30-\Omega$, $40-\Omega$, $60-\Omega$, and $120-\Omega$ setting)	V _{CCIO} = 1.5, 1.35, 1.25 V	-10 to +40	-10 to +40	%	
60- Ω and 120- Ω R _T	Internal parallel termination with calibration (60- Ω and 120- Ω setting)	$V_{CCIO} = 1.2$	-10 to +40	-10 to +40	%	
25- $\Omega R_{S_left_shift}$	Internal left shift series termination with calibration (25- Ω R _{S_left_shift} setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%	

Table 2-11: OCT Without Calibration Resistance Tolerance Specifications for Arria V GZ Devices

Symbol	Description	Conditions	Resistance	Unit	
		Conditions	C3, I3L	C4, I4	Onic
25-Ω R, 50-Ω R _S	Internal series termination without calibration (25- Ω setting)	V _{CCIO} = 3.0 and 2.5 V	±40	±40	%



2-28	Transmitter
------	-------------

Sumbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit	
Symbol/Description	Conditions	Min	Тур	Мах	Min	Тур	Max	Onic	
	85- Ω setting	—	85 ± 20%	_	_	85 ± 20%	—	Ω	
Differential on-chip termination	100- Ω setting		100 ± 20%			100 ± 20%	_	Ω	
resistors	120- Ω setting	—	120 ± 20%			120 ± 20%	_	Ω	
	150-Ω setting	—	150 ± 20%			150 ± 20%	_	Ω	
V _{OCM} (AC coupled)	0.65-V setting	—	650			650	_	mV	
V _{OCM} (DC coupled)	_	—	650			650	—	mV	
Intra-differential pair skew	Tx V _{CM} = 0.5 V and slew rate of 15 ps	—		15	_	_	15	ps	
Intra-transceiver block transmitter channel-to-channel skew	x6 PMA bonded mode			120			120	ps	
Inter-transceiver block transmitter channel-to-channel skew	xN PMA bonded mode			500			500	ps	

Related Information

Arria V Device Overview

For more information about device ordering codes.



Symbol	V _{OD} Setting	V _{OD} Value (mV)	V _{OD} Setting	V _{OD} Value (mV)
	15	300	47	940
	16	320	48	960
	17	340	49	980
	18	360	50	1000
	19	380	51	1020
	20	400	52	1040
	21	420	53	1060
	22	440	54	1080
V_{OD} differential peak to peak typical	23	460	55	1100
	24	480	56	1120
	25	500	57	1140
	26	520	58	1160
	27	540	59	1180
	28	560	60	1200
	29	580	61	1220
	30	600	62	1240
	31	620	63	1260



Symbol	Parameter	Min	Тур	Мах	Unit
t _{OUTPJ_IO} , ⁽¹⁷³⁾ , ⁽¹⁷⁵⁾	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	600	ps (p-p)
	Period Jitter for a clock output on a regular I/O in integer PLL (f _{OUT} < 100 MHz)			60	mUI (p-p)
t _{FOUTPJ_IO} ⁽¹⁷³⁾ , ⁽¹⁷⁵⁾ , ⁽¹⁷⁶⁾	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)			600	ps (p-p)
	Period Jitter for a clock output on a regular I/O in fractional PLL (f _{OUT} < 100 MHz)		_	60	mUI (p-p)
t _{OUTCCJ_IO} ⁽¹⁷³⁾ , ⁽¹⁷⁵⁾	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \ge 100 \text{ MHz}$)		_	600	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL (f _{OUT} < 100 MHz)			60	mUI (p-p)
t _{FOUTCCJ_IO} ⁽¹⁷³⁾ , ⁽¹⁷⁵⁾ , ⁽¹⁷⁶⁾	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)			600	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL (f _{OUT} < 100 MHz)		_	60	mUI (p-p)
t _{CASC_OUTPJ_DC} ⁽¹⁷³⁾ , ⁽¹⁷⁷⁾	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} \ge 100 \text{ MHz}$)			175	ps (p-p)
	Period Jitter for a dedicated clock output in cascaded PLLS (f _{OUT} < 100 MHz)			17.5	mUI (p-p)
dK _{BIT}	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits

⁽¹⁷⁵⁾ The external memory interface clock output jitter specifications use a different measurement method, which is available in the "Memory Output Clock Jitter Specification for Arria V GZ Devices" table.

⁽¹⁷⁶⁾ This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05–0.95 must be \geq 1000 MHz.

⁽¹⁷⁷⁾ The cascaded PLL specification is only applicable with the following condition:



a. Upstream PLL: 0.59Mhz ≤ Upstream PLL BW < 1 MHz

b. Downstream PLL: Downstream PLL BW > 2 MHz

Table 2-52: Worst-Case DCD on Arria V GZ I/O Pins

The DCD numbers do not cover the core clock network.

Symbol	C3, I3L		C4, I4		Unit
Зушьог	Min	Max	Min	Max	ont
Output Duty Cycle	45	55	45	55	%

Configuration Specification

POR Specifications

Table 2-53: Fast and Standard POR Delay Specification for Arria V GZ Devices

Select the POR delay based on the MSEL setting as described in the "Configuration Schemes for Arria V Devices" table in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

POR Delay	Minimum (ms)	Maximum (ms)
Fast	4	12 (202)
Standard	100	300

Related Information

Configuration, Design Security, and Remote System Upgrades in Arria V Devices

Altera Corporation



⁽²⁰²⁾ The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

2-64 FPP Configuration Timing when DCLK to DATA[] > 1

Symbol	Parameter	Minimum	Maximum	Unit
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK}$ period	_	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (8576 × CLKUSR period) ⁽²¹⁵⁾		_

Related Information

- DCLK-to-DATA[] Ratio (r) for FPP Configuration on page 2-57
- Configuration, Design Security, and Remote System Upgrades in Arria V Devices





⁽²¹⁵⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Related Information

Configuration, Design Security, and Remote System Upgrades in Arria V Devices

Initialization

Table 2-61: Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices

Initialization Clock Source	Configuration Schemes	Maximum Frequency (MHz)	Minimum Number of Clock Cycles	
Internal Oscillator	AS, PS, FPP	12.5		
arap (222)	PS, FPP	125	9576	
CLKUSR	AS	100	8370	
DCLK	PS, FPP	125		

Configuration Files

Use the following table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (.hex) or tabular text file (.ttf) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size.

Arria V GZ Device Datasheet

Altera Corporation



⁽²²¹⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.

⁽²²²⁾ To enable CLKUSR as the initialization clock source, turn on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software from the General panel of the Device and Pin Options dialog box.